Design & implementation of FPGA based digital FIR filter

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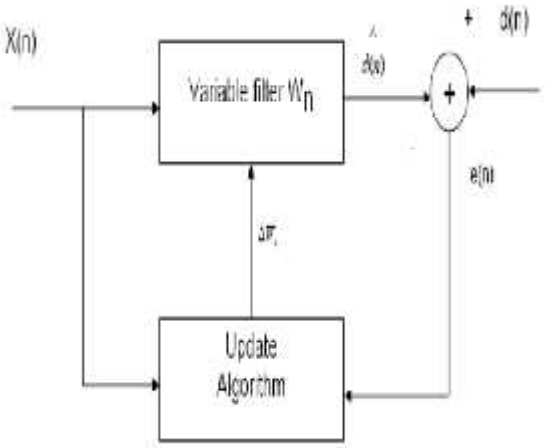
ABSTRACT
Digital filters are used extensively in all areas of electronic industry. This is because Digital filters have the potential to attain much better signal to noise ratios than analog filters and at each intermediate stage the analog filter adds more noise to the signal. Fir filters are commonly used in a wide range of applications such as Echo cancellation, Noise cancellation, Prediction, System modeling or system identification, Radar signal processing, Equalizations of communication channels, Biomedical signal enhancements, Navigational systems, Digital communication Receiver, and many more. Many algorithm transformation techniques are available for optimum implementation of the digital signal processing algorithms. Reducing the area is important for digital FIR filters. By reducing the size device portability will increase and as the number of component reduces the overall noise of the device will reduces. So to achieve this target we have use new approach to design a filter. Field programmable gate arrays are widely used in many areas such as audio and video, Digital signal processing, Image signal Processing, Digital communication systems, mobile communication system and many other embedded applications, because of their high performance, parallel processing ability and flexibility. We used shift register logic and distributed arithmetic based logic for implementation of FIR filter. All architecture implemented using Xilinx Virtex 4 Starter Kit as the target board and Xilinx System Generator (XSG).

Keywords: Multiplier and accumulator, multiple constant multiplication, Fir filter, distributed arithmetic.

INTRODUCTION
Adaptive filters have become vastly popular in the area of digital signal processing. Adaptive direct modeling or system identification and adaptive inverse modeling or channel equalization find extensive applications in telecommunication, control system, instrumentation, power system engineering and geophysics.

Filter adds more noise to the signal; the digital filter performs noiseless mathematical operations at each intermediate step in the transform. As the digital filters have merged as a strong option for removing noise, shaping spectrum, and minimizing inter-symbol interference in communication architectures. These filters have become popular because their precise reproducibility allows design engineers to achieve performance levels that are difficult to obtain with analog filters .

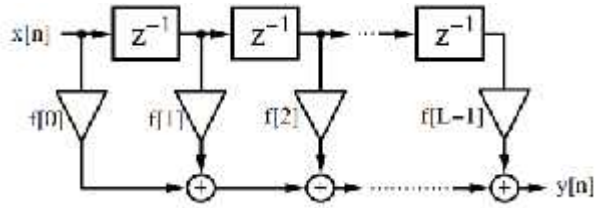
Adaptive Filter
An adaptive filter is a filter that adjusts its transfer function according to an optimizing algorithm. Because of the complexity of the optimizing algorithms, most adaptive filters are digital filters that perform digital signal processing and adapt their performance based on the input signal used.[1]



Adaptive Filter

FIR filter

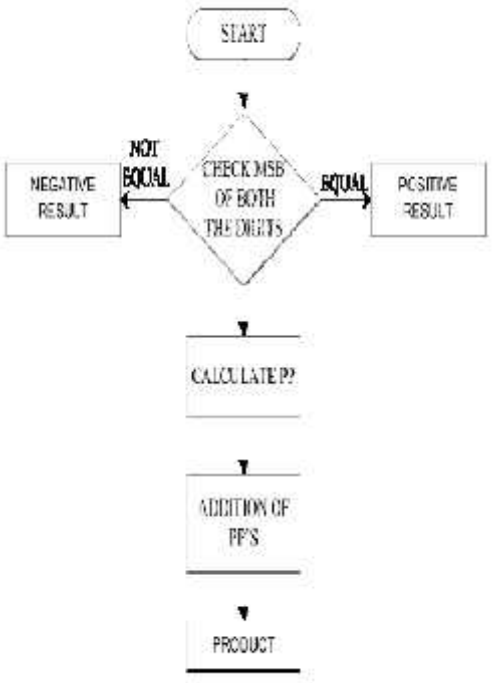
The Lth-order LTI FIR filter is graphically interpreted in Fig.It can be seen to consist of a collection of a "tapped delay line," adders, and multipliers. One of the operands
presented to each multiplier is an FIR coefficient, often referred to as a "tap weight" for obvious reasons. Historically, the FIR filter is also known by the name "transversal filter," suggesting its "tapped delay line" structure [7].



FIR filter

MULTIPLIER AND ACCUMULATOR

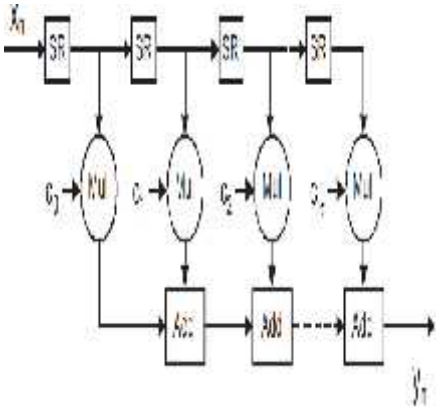
A multiplier can be divided into three operational steps. The first is radix-2 Booth encoding in which partial product is generated from the multiplicand X and the multiplier Y. The second is adder array or partial product compression to add all partial products. The last is the final addition in which the process to accumulate the multiplied results is included.[2]



MULTIPLIER AND ACCUMULATOR

FIR filter using shift register logic

Due to the intensive use of FIR filters in video and communication systems, high performance in speed, area and power consumption is demanded. Basically, digital filters are used to modify the characteristic of signals in time and frequency domain and have been recognized as primary digital signal processing operations In FIR filter design using shift register logic the input is shifted through n number of registers also called "taps". They are multiplied by a number of constant coefficients and added up.



FIR filter using shift register logic block diagram

Where $x_b[n]$ represents the b[th] bit position of the number's binary representation. Many DSP Algorithms like convolution and correlation are formulated in a sum of products (SOP) fashion. The key is to realize that the second summation can be mapped to a Look up Table (LUT). The coefficients c[n] are known .then each SOP is just a combination of the c[n]'s for which a logic cell table can be constructed. Multiplication by a power of 2 is no more that a bit shift, finally, a block diagram for the DA implementation of a FIR filter is shown in figure 3.6.Here look up table is used as a multiplier and accumulator is used as a shifter.

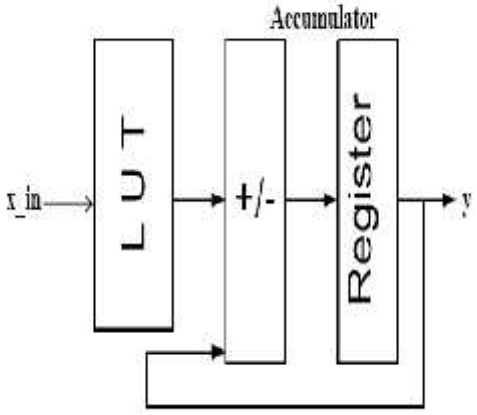
4 FIR filter using distributed arithmetic logic

Distributed Arithmetic (DA) is a different approach for implementing digital filters. The basic idea is to replace all multiplications and additions by a table and a shifter accumulator. DA relies on the fact that the filter coefficients are known, so constant Distributed Arithmetic (DA) can be used to compute sum of products. Consider the following sum of products:

$$y = c[0]x[0]+c[1]x[1]+\cdots+c[N-1]x[N-1] \quad (3.4)$$

Further assume that the coefficients c[n] are known values and that the variable x[n] can be represented by

$$x[n]=\sum_{b=0}^{B-1} x_b[n]\times 2^b \quad \text{With} \quad x_b[n]\in[0,1] \quad (3.5)$$



FIR filter using distributed arithmetic logic block diagram

RESULTS

The device utilization summary of our design is given below .

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of 4 input LUTs	22	[illegible]	[illegible]
Logic Distribution			
Number of occupied Slices	12	[illegible]	[illegible]
Number of Slices containing only related logic	12	[illegible]	100%
Number of Slices containing unrelated logic	0	[illegible]	0%
Total Number of 4 input LUTs	23	[illegible]	[illegible]
Number used as logic	22		
Number used as route-thru	1		
Number of bonded IOBs	17	[illegible]	[illegible]
Number of BUFG/BUFGCTRLs	1	[illegible]	[illegible]
Number used as BUFGs	1		
Number used as BUFGCTRLs	0		
Total equivalent gate count for design	389		
Additional JTAG gate count for IOBs	816		

Design summary by using FIR filter using shift register

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	[illegible]	[illegible]	1%
Number of 4 input LUTs	[illegible]	[illegible]	1%
Logic Distribution			
Number of occupied Slices	[illegible]	[illegible]	1%
Number of Slices containing only related logic	[illegible]	19	100%
Number of Slices containing unrelated logic	[illegible]	19	0%
Total Number of 4 input LUTs	[illegible]	[illegible]	1%
Number of bonded IOBs	[illegible]	240	6%
Number of BUFG/BUFGCTRLs	[illegible]	32	3%
Number used as BUFGs	[illegible]		
Number used as BUFGCTRLs	[illegible]		
Total equivalent gate count for design	[illegible]		
Additional JTAG gate count for IOBs	[illegible]		

Figure Design summary by using FIR filter using shift register

CONCLUSION

(1) In this approach we presented low area FIR filters to reduce area we have use shift register and distributed arithmetic based approach. It demonstrated that our approach is most effective for implementations with the constraints of low area and low power.

(2) It demonstrated that our approach is most effective for implementations with the constraints of low area. The proposed FIR filters have been synthesized and implemented using Xilinx ISE Virtex 4. We presented a low area FIR filter. For reduce area we used shift register and distributed arithmetic based concept architecture. These filters were compared for area with other common implementations.

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