Improving Performance of DVR with High-Frequency Isolated DC-DC Converter

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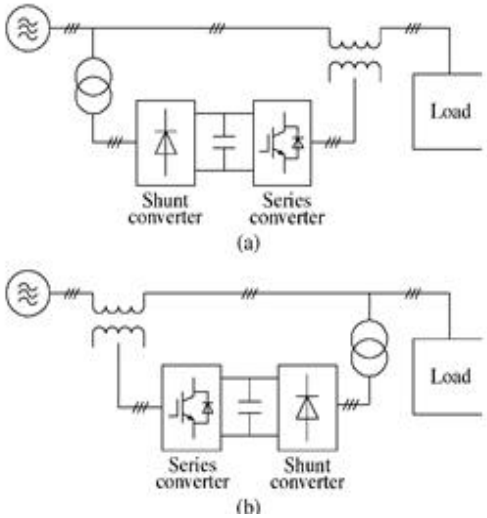
***Abstract*—This paper presents a dynamic voltage restorer(DVR) that is characterized by the use of a high-frequency unidirectional isolated dc-dc converter. A traditional DVR has a large and bulky series transformer even for three-phase low-voltage up to 480-V applications because the transformer operates at the line frequency (50 or 60 Hz). As the increase in the development of power electronics which have a suitable high frequency isolated dc-dc converters. This paper discusses the control and performance of a low-voltage DVR using a high-frequency isolated dc-dc converter. The high-frequency (20-kHz) transformer in the dc-dc converter is much smaller, for example, one-hundredth,in volume thanthe line-frequency transformer. Moreover, connecting the shunt converter to the load side brings a significant reduction in energy storage capacity to the DVR. Experimental results obtained from a three-phase three-wire 200-V 5-kW laboratory system confirm the viability and effectiveness of the system configuration.**

I. INTRODUCTION

RESEARCH has been conducted on a dynamic voltage restorer (DVR) to ride through voltage sags. Fig. 1(a) shows a system configuration of a traditional DVR, whichis characterized by connecting the shunt converter (the diode rectifier) to the supply side. The DVR consists of shunt and series converters connected back to back and a common dc capacitor as an energy-storage device. Fig. 1(b) shows another configuration that is characterized by connecting the shunt converter to the load side [1], [2]. The series converter can maintain the ac terminal voltages of the shunt converter at a nominal voltage even while voltage sags occur. Therefore, the aim of the dc capacitor is not to store the energy required for riding through voltage sags but to smooth the dc voltage. This makes the dc capacitor in Fig. 1(b) 100 times smaller in capacitance value than that in Fig. 1(a). The system in Fig. 1(b) increases the line current during voltage sags because it continuously draws electric power from the supply to maintain the load voltage. The increased line current may cause an impact upon the supply and it's upstream. Thus, the system configuration in Fig. 1(b) would be suitable only for providing emergency power to low-voltage critical loads up to 480 V. However, the series transformer is still heavy, bulky, and costly because it operates at the line frequency. Moreover, the series transformer suffers from a dc magnetic-flux bias during several line cycles after voltage sag occurs and restores.



This requires double the cross-sectional core area of the series transformer in order to avoid magneticflux saturation.

Fig.(1) .System configurations of DVRs. (a) Shunt converter are connected to the supcply side. (b) Shunt converter is connected to the load side

Multilevel topologies such as diode-clamped or cascaded pulse width modulation (PWM) converters can eliminate line frequency transformers from medium-voltage applications [3], [4]. However, both system configurations in Fig. 1 require line frequency transformers to achieve galvanic isolation between the three-phase ac power lines and the ac terminals of the series converter even in three-phase low-voltage applications. Fig. 2 show a system configuration that is prominent in using ac boost choppers [5]. This DVR can boost a decreased or dropped supply voltage directly to the nominal voltage so that neither the energy-storage device nor the line-frequency transformer is required in low voltage applications. However, voltage-sag compensation has a limitation resulting from using the boost choppers. To achieve successful voltage-sag compensation, at least two line-to-neutral voltages must be higher than half the nominal voltage. In addition, the blocking voltage of all the insulated-gate bipolar transistors (IGBTs) used should be higher than the nominal

voltage.

Fig.3 shows another system configuration in which a high-frequency-link cyclo converter is used [6]. Although the high frequency (e.g., 20 kHz) makes the transformer compact, a large energy-storage device is required to ride through voltage sags.

Attention has been paid to high-frequency unidirectional and bidirectional isolated dc-dcconverters based on single-phase and three-phase full-bridge configurations [7]. A main motivation of the isolated dc-dc converters is to replace line-frequency transformers with high-frequency

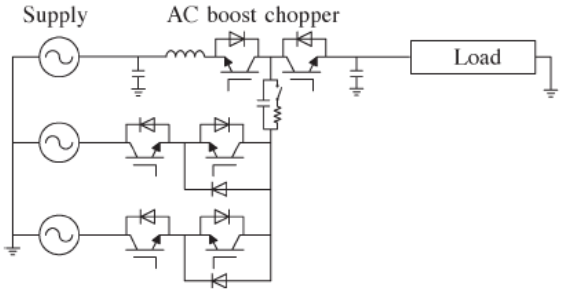


Fig. 2. Three-phase DVR with ac boost choppers [5], where a single-phase load is drawn for simplicity.

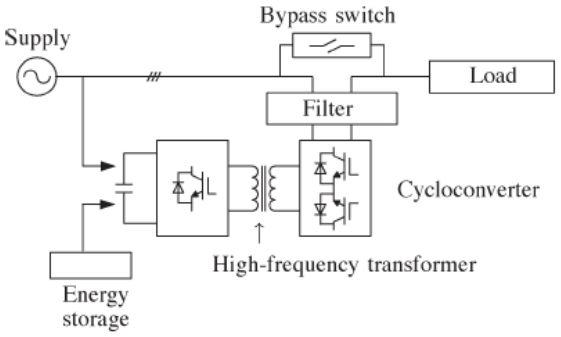


Fig. 3. Three-phase DVR with a high-frequency-link cycloconverter [6].

transformers, in which galvanic isolation is indispensable between the two sets of dc terminals. A Nanocrystalline soft magnetic core (FINEMET) that is available from the market offers high saturation flux density (more than 1.2 T) and high relative permeability (over 10 000 at 100 kHz), leading to an extremely low core loss [8]. The combination of the magnetic core with the latest trench-gate IGBTs and superjunction MOSFETshas made it possible to improve the system efficiency of the dc-dc converters up to 97% or higher [9], [10]. In the near future, the emergence of silicon carbide (SiC) switching devices and a new magnetic core material will allow the system efficiency to reach higher than 99%.

This paper addresses the design and performance of a new DVR, the system configuration of which is characterized by using a high-frequency unidirectional isolated dc-dc converter intended for low-voltage applications. Moreover, connecting the shunt converter to the load side enables one to eliminate an energy-storage device from the DVR. Experimental results obtained by a 200-V 5-kW laboratory system verify the viability and effectiveness of the system configuration.

II. NEW SYSTEM CONFIGURATION

The aim of the three single-phase series transformers inFig. 1 is to achieve galvanic isolation between an ac mains powerline and the corresponding series converter in eachphase. As a result, the DVR is allowed to use a common dc link for the series and the shunt converters.

Fig. 4 shows the single-line circuit diagram of a new DVR, which uses a high-frequency unidirectional isolated dc-dc converter. The circuit parameters are shown in Table I. Figs. 1(b) and Fig. 4 are similar in system configuration and are the same in power flow during the occurrence of voltage sags. However, the following significant difference exists in achieving galvanic isolation among the three single-phase series converters: The high-frequency transformer in the high-frequency dc-dc converter takes the part of the series line-frequency transformer in Fig. 1(b). Thus, the DVR has a common dc capacitor for the shunt converter and other three individual dc capacitors for the three series converters.

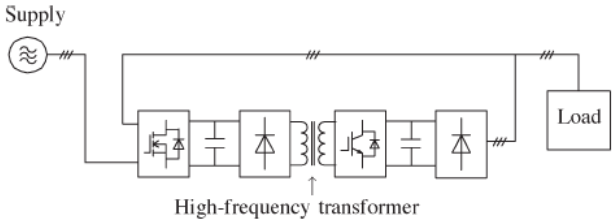


Fig. 4. DVR with a high-frequency unidirectional isolated dc-dc converter.

TABLE I
SYSTEM PARAMETERS

The AC Mains	
Line-to-line rms voltage (V_{nom})	200V
Frequency (f)	50Hz
The Load	
Rating (P_L)	5kW
The DVR	
AC Inductor L_R	1.3mH (5%)*
DC Capacitor C_{dc1}	2,000 F
DC Voltage V_{dc1}	273 V
Unit Capacitance Constant H_1*	15 ms
DC Capacitor C_{dc2}	5,400 F
DC Voltage V_{dc2}	90 V
Unit Capacitance Constant H_2*	13 ms
DC Inductor L_{dc2}	0.18 mH (0.7%)
Switching Frequency f_s	20 kHz
Dead Time T_d	2 s
Switching ripple filter f_C	2.17 kHz
L_f	0.180 mH (0.85%)*
C_f	30 F
R_f	1Ω

* Parameters in () are based on 3ø, 220V, 5kVA, and 50Hz

III. EXPERIMENTAL SYSTEM

A. System Configuration

Fig. 5 shows the experimental circuit configuration of a DVR for a 200-V 5-kW load. A voltage-sag generator is connected to cause single- or three-phase voltage sags intentionally. The DVR consists of the so-called "back-to-back" connection of series and shunt converters via a high-frequency isolated dc-dc converter. The high-frequency transformer operating at 20 kHz has a single winding in the primary and three sets of galvanically isolated windings in the secondary.

The main circuit of the shunt converter uses a three-phase diode rectifier, and the dc link is connected to the primary side of the dc-dc converter. The peak dc voltage of v_{dc1}reaches 284 V ($= \sqrt{2} \times 200$ V) so that the dc-dc converter uses four 600-V IGBTs in the primary full-bridge inverter.

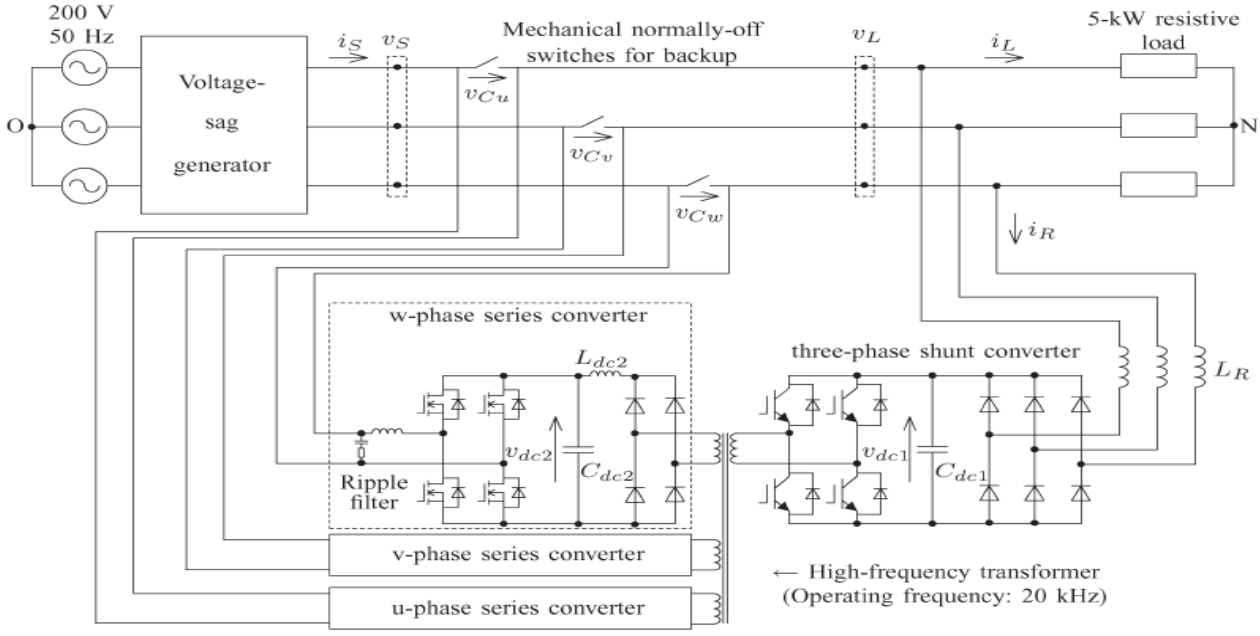


Fig. 5. Experimental circuit configuration of the DVR, including a high-frequency unidirectional isolated dc-dc converter.

On the other hand, the minimum dc input voltage to the series converter V_{dc2} requires a voltage of 82 V ($= \sqrt{2/3} \times 200\ \text{V} \times 50\%$) for voltage-sag compensation of a voltage dip of 50%. This paper designed the dc voltage V_{dc2} to be 90 V so that the dc-dc converter uses four 200-V fast-recovery diodes in the secondary full-bridge rectifier.

Each series converter uses four 200-V MOSFETs. Generally, MOSFETs have a tradeoff or compromise between ON-state resistance and output capacitance. The series converter selects the MOSFETs (Renesas: H5N2008P) with a low ON-state resistance (R_{on} = 20 mΩ, P_{loss} = 4.5 W at 5 kVA) in the two lower arms because the lower arm MOSFETs remain turned on during standby mode. On the other hand, the upper arm MOSFETs (Renesas: RJK2009DPM) have a smaller output capacitance (C_{loss} = 520 pF) than the lower arm MOSFETs. Note that the mechanical switches in Fig. 5 are installed only for backup, which remain normally open in compensation mode, as well as in standby mode. This idea of using the two different types of MOSFETs contributes to reducing the conducting loss during standby mode and to achieving fast voltage-sag compensation.

The mechanical switches are also applicable to bypass the line current until the occurrence of voltage sags. This operation of bypassing enables reducing the conduction loss under a normal operating condition. However, this may cause a compensation delay of 10 ms or more due to the slow response in the mechanical switches, even when a fast voltage detection circuit or control is implemented in the system.

The diode rectifier produces an amount of harmonic current in the supply. Since the voltage sag lasts in a short duration of 100 ms or less, the harmonic current may not cause any problem. It is also possible to replace the diode rectifiers with a PWM rectifier using six IGBTs to eliminate harmonic currents from the shunt device. The PWM rectifier, however, may bring a switching loss to the IGBTs and a core loss to L_R.

Fig. 6 shows a photograph of the handmade high-frequency (20-kHz) transformer used in this experiment, along with one of the three single-phase line-frequency series transformers used in [2]. Table II describes the characteristics of the high frequency transformer. It uses a nano crystalline soft magnetic core (FINEMET) that offers high permeability at high frequencies. The operating frequency is designed to be 20 kHz in consideration of the electrical characteristics of the magnetic core and the IGBTs. The turn number of the high-frequency transformer is designed to be 15 : 3 ($= V_{dc1} : V_{dc2}$). It is desirable that the leakage inductance should be much lower than the magnetizing inductance because a voltage drop causedby the leakage inductance produces a bad effect on regulating the secondary dc voltage v_{dc2}. The handmade high-frequency transformer has the primary and secondary windings lapped together on two magnetic core stacks in order to reduce the leakage inductance. The volume of the high-frequency transformer is 171.6 cm^3 ($= W \times T \times D$ = 6.5 cm× 5.5 cm× 4.8 cm) that is one-hundredth of that of the line-frequency transformer.

TABLE II
CHARACTERISTICS OF THE HIGH-FREQUENCY TRANSFORMER

Core Material	Nano-crystalline soft magnetic core

	(FINEMET™) [8]
Operating Frequency	20kHz
Winding resistance*	160mΩ
Leackage inductance*	10μH
Mutual inductance*	1.86mH
Size	W 6.5×T 5.5×D 4.8 cm (=171.6 cm^3)

Optimal design would bring a further reduction in volume to the high-frequency transformer. Note that the DVR in Fig. 5 devotes itself to voltage-sag compensation. Voltage-swell compensation can be achieved by replacing the unidirectional dc-dc converter and the diode rectifier with a bidirectional dc-dc converter and a PWM rectifier.

B. Control Method

Fig. 7 shows the control block diagram for the series converters [2]. The phase-locked loop circuit detects the three-phase supply voltage v_S and calculates the phase-angle information θ_S. The three-phase supply voltages are transformed into the d- and q-axis voltages, namely, v_d and v_q on the d-q reference frames. The d-axis voltage v_d is equal to the nominal ac mains line-to-line rms voltage V_{nom} (= 200 V), and v_q is equal to zero when the three-phase supply voltages are sinusoidal and balanced in normal conditions. Thus, the d- and q-axis reference voltages can be set as $v^d = V_{nom}$ (= 200 V) and $v^*_q = 0$.

A voltage-sag depth in the three-phase three-wire circuit can be represented by Δv_d and Δv_q on the d-q reference frames, which are obtained by subtracting v_d and v_q from v^d and v^q. Then, three-phase compensating voltages Δv_u, Δv_v, and Δv_w are calculated by applying the inverse d-q transformation to Δv_d and Δv_q. Adding a common zero-sequence voltage v_{C0} to the three-phase compensating voltages produces the three phase compensating voltage references for the series converters, namely v^*_{Cu}, v^*_{Cv} and v^*_{Cw} as follows:

$$\begin{aligned} v^*_{Cu} &= \Delta v_u + v_{Co} \\ v^*_{Cv} &= \Delta v_v + v_{Co} \\ v^*_{Cw} &= \Delta v_w + v_{Co} \end{aligned} \quad (1)$$

Here, the zero-sequence voltage v_{C0} is calculated by

$$v_{Co} = -\frac{\max(\Delta v_u, \Delta v_v, \Delta v_w)}{2} - \frac{\min(\Delta v_u, \Delta v_v, \Delta v_w)}{2} \quad (2)$$

This zero-sequence voltage plays an important role in sharing the compensating voltages among the three series converters [2].

IV. Effect of the Zero-Sequence-Voltage Control

A. Assumptions for Analysis

The dc-dc converter has three single-phase diode rectifiers in the secondary, and three individual floating dc-link capacitorsare installed between the three diode rectifiers and the three series converters. Analysis in this section confirms that the zero-sequence-voltage control defined in (1) and (2) produces a good effect on the DVR during the occurrence of voltage sags.

The following discussion assumes a u-phase voltage sag, the magnitudes of which are given as Δv_{Su}, Δv_{Sv}, and Δv_{Sw}.

$$\begin{cases} \Delta v_{Su} = \sqrt{\frac{2}{3}}\delta V_{nom} \cos\omega t \\ \Delta v_{Sv} = 0 \\ \Delta v_{Sw} = 0 \end{cases} \quad (3)$$

where δ is a ratio of a voltage-sag depthwith respect to the nominal line-to-neutral voltage ($= V_{nom}/\sqrt{3}$). In addition, the three-phase supply currents are assumed to be sinusoidal and balanced with unity power factor as follows:

$$\begin{cases} i_{Su} = \sqrt{2} I_S \cos\omega t \\ i_{Sv} = \sqrt{2} I_S \cos(\omega t - 2\pi/3) \\ i_{Sw} = \sqrt{2} I_S \cos(\omega t + 2\pi/3) \end{cases} \quad (4)$$

where $I_S$is the rms value of i_S.

B. Direct Compensation for Voltage Sag

When the DVR tries to compensate directly for the voltage sag, the compensating voltage v_C is equal to the voltage sag Δv_S as follows:

$$\begin{aligned} v_{Cu} &= \Delta v_{Su} = \frac{\sqrt{2}\delta V_{nom}}{\sqrt{3}} \cos\omega t \\ v_{Cv} &= \Delta v_{Sv} = 0 \\ v_{Cw} &= \Delta v_{Sw} = 0 \end{aligned} \quad (5)$$

Therefore, the instantaneous active power released from the series converter p_C is calculated by

$$\begin{aligned} p_{Cu} &= v_{Cu} \cdot i_{Su} = \frac{\delta V_{nom}}{\sqrt{3}} I_S (1 + \cos 2\omega t) \\ p_{Cv} &= v_{Cv} \cdot i_{Sv} = 0 \\ p_{Cw} &= v_{Cw} \cdot i_{Sw} = 0 \end{aligned} \quad (6)$$

Equation (6) suggests that the active power concentrates onlyon the u-phase. Then, the three dc-voltage ripples Δv_{dc2u},Δv_{dc2v}, and $\Delta v_{dc2w}$are calculated by

$$\begin{aligned} \Delta v_{dc2u} &= \frac{1}{C_{dc2} V_{dc2u}} \int \Delta p_{Cu}\, dt \\ &= \frac{\delta V_{nom}\, I_S}{2\sqrt{3}\omega C_{dc2} V_{dc2u}} \sin 2\omega t \end{aligned} \quad (7)$$

$$\Delta v_{dc2v} = \frac{1}{C_{dc2} V_{dc2v}} \int \Delta p_{Cv} dt = 0$$

$$\Delta v_{dc2w} = \frac{1}{C_{dc2} V_{dc2w}} \int \Delta p_{Cw} dt = 0$$

where $\Delta p_{Cu}, \Delta p_{Cv}\ and\ \Delta p_{Cw}$ are the active-power ripples that correspond to the second terms in (9) and $V_{dc2u}, V_{dc2v}\ and\ V_{dc2w}$ are the mean dc voltages.

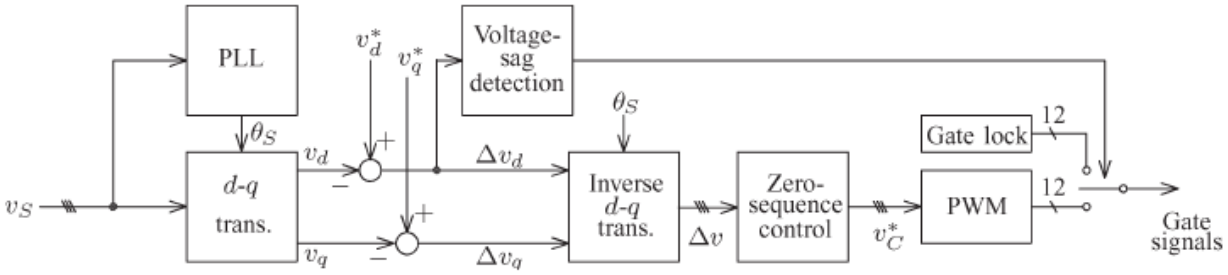


Fig. 6. Control block diagram for the series converters.

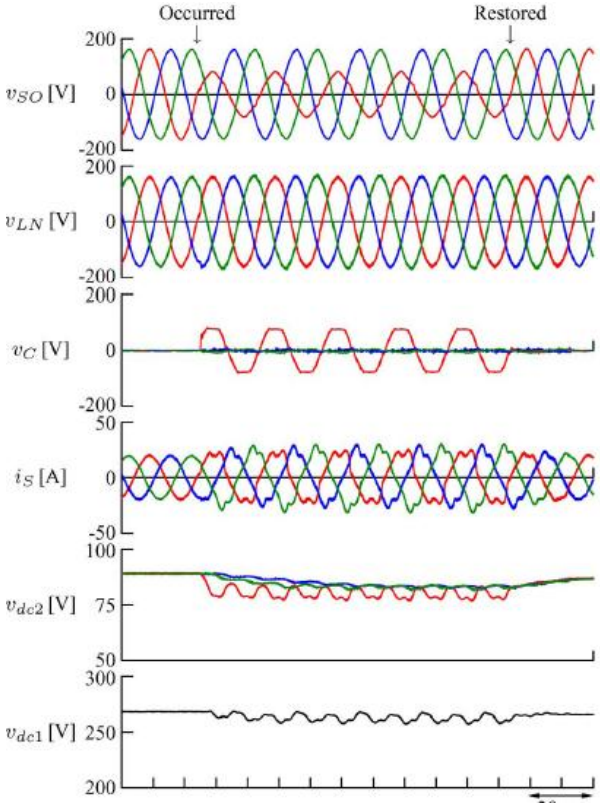


Fig. 7. Experimental waveforms under a single-phase voltage sag when the three-phase compensating voltage references were directly given without zero-sequence-voltage control.

C. Zero-Sequence-Voltage Superimposition

When the zero-sequence-voltage control discussed in the previous section is applied, the zero-sequence voltage is calculated by substituting (3) into (2) as follows:

$$v_{Co} = -\frac{1}{2}\Delta v_{Su} = -\frac{1}{2}\sqrt{\frac{2}{3}}\delta V_{nom}\cos\omega t \quad (7)$$

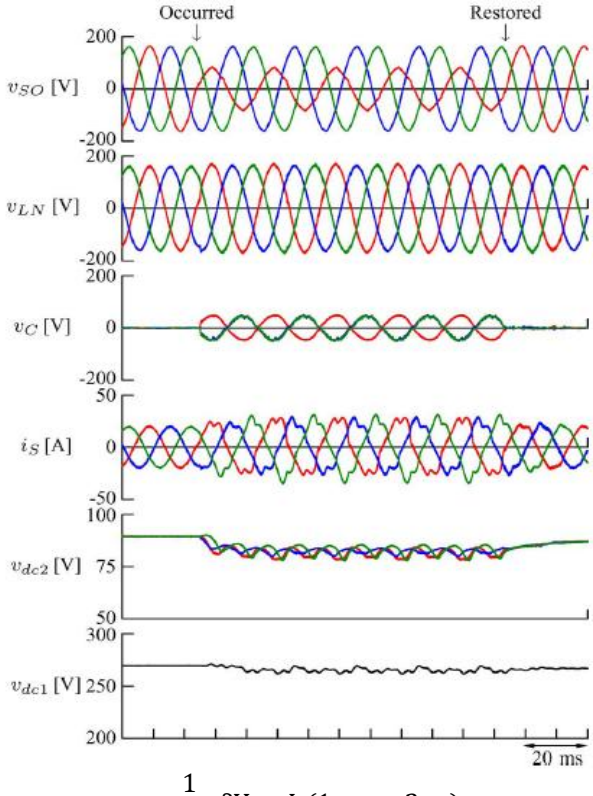
Hence, the three-phase compensating voltages v_{Cu}, v_{Cv}, and v_{Cw} are represented by

$$v_{Cu} = \frac{1}{2}\sqrt{\frac{2}{3}}\delta V_{nom}\cos\omega t \quad (8)$$

$$v_{Cu} = v_{Cw} = -\frac{1}{2}\sqrt{\frac{2}{3}}\delta V_{nom}\cos\omega t$$

The instantaneous active power released from the series converter p_C is obtained by

$$p_{Cu} = v_{Cu}\cdot i_{Su} \quad (9)$$



$$= \frac{1}{2\sqrt{3}}\delta V_{nom} I_S(1+\cos 2\omega t)$$

Fig. 8. Experimental waveforms under a single-phase voltage sag when the zero-sequence voltage v_{C0}, calculated by (2), was superimposed.

$$p_{Cv} = v_{Cv}\cdot i_{Sv} = \frac{1}{2\sqrt{3}}\delta V_{nom} I_S\left\{\frac{1}{2}-\cos(2\omega t - 2\pi/3)\right\}$$

$$p_{Cw} = v_{Cw}\cdot i_{Sw} = \frac{1}{2\sqrt{3}}\delta V_{nom} I_S\left\{\frac{1}{2}-\cos(2\omega t + 2\pi/3)\right\}$$

The first and second terms in the right hand side of (6) and (9) indicate the mean active power and the active-power ripple in each phase, respectively. Comparing (6)-(9) reveals that the zero-sequence-voltage control has the following advantages.

1) The differences in mean active power among the

three phases are mitigated, and the maximal mean active powercan be reduced to half. This has a function of sharing the compensating active powers among the three series converters.

2) The active-power ripples are also reduced to half. This brings a reduction in the capacitance value to the three dc capacitors C_{dc2}.

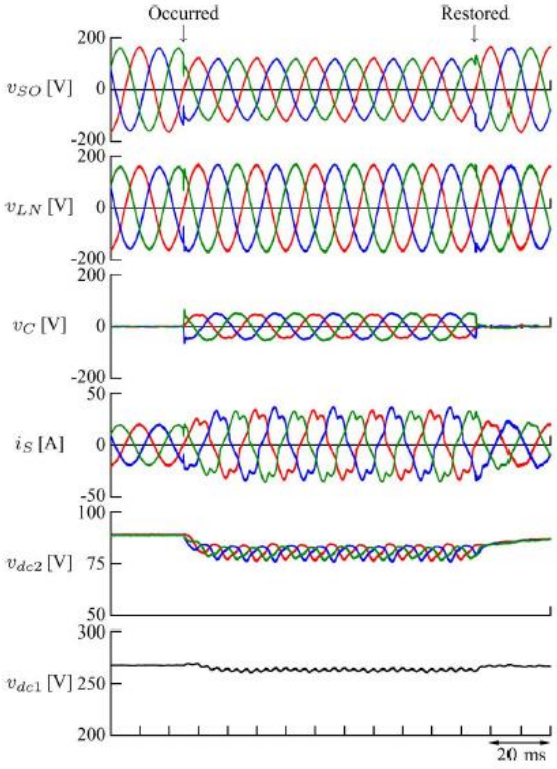


Fig. 9. Experimental waveforms under a three-phase voltage sag when the three-phase compensating voltage references were directly given without zero-sequence-voltage control.

Finally, the dc-voltage ripples Δv_{dc2u} , Δv_{dc2v} , and Δv_{dc2w} are calculated by

$$\Delta v_{dc2u} = \frac{1}{C_{dc2} V_{dc2u}} \int \Delta p_{Cu}\, dt$$

$$= \frac{\delta V_{nom}\, I_S}{4\sqrt{3} C_{dc2} V_{dc2u}} \sin 2\omega t$$

$$\Delta v_{dc2v} = \frac{1}{C_{dc2} V_{dc2v}} \int \Delta p_{Cv}\, dt$$

$$= -\frac{\delta V_{nom}\, I_S}{4\sqrt{3} C_{dc2} V_{dc2v}} \sin(2\omega t - 2\pi/3)$$

$$\Delta v_{dc2w} = \frac{1}{C_{dc2} V_{dc2v}} \int \Delta p_{Cv}\, dt \qquad (10)$$

$$= -\frac{\delta V_{nom}\, I_S}{4\sqrt{3} C_{dc2} V_{dc2w}} \sin(2\omega t + 2\pi/3)$$

Figs. 7 and 8 show the experimental waveforms under single-phase voltage sag. As already shown in Fig. 5, the three-phase resistor rated at 200 V and 5 kW was used as a load, and the voltage-sag generator was employed to intentionally cause the single-phase voltage sag with a depth of 50% and a time interval of 100 ms.In Fig. 8, the three-phase compensating voltage references were directly given from the detected voltage sag without zero-sequence-voltage control. Both the amplitude and phase angle of the load voltage v_{LN}were almost maintained even duringthe occurrence of the voltage sag. However,

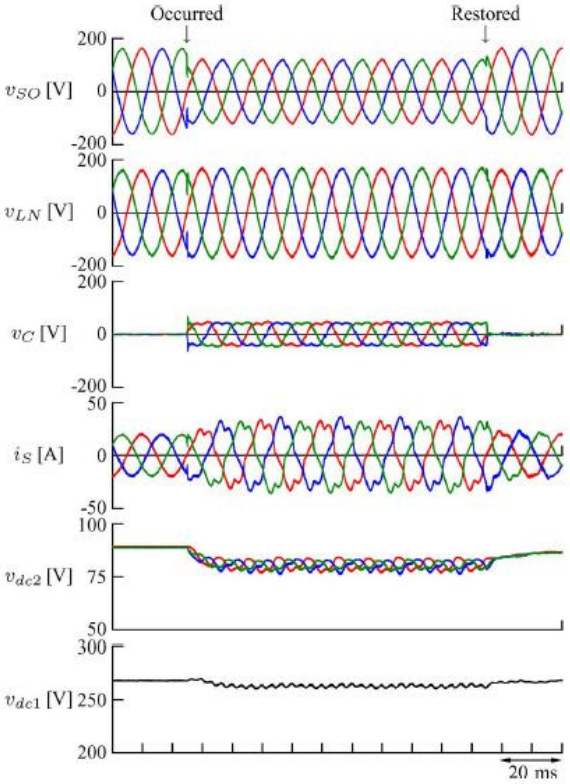


Fig. 10. Experimental waveforms under a three-phase voltage sag when the zero-sequence voltage v_{C0} , calculated by (2), was superimposed.

the waveform of v_C contained the harmonic voltage resulting from the two following reasons. One is that the u-phase compensating voltage reference $v_{Cu}$was equal to the u-phase detected voltage sag, the peak value of which was $\sqrt{2/3} \times 200\, V \times 50\% = 82V$.

The other is that a non negligible voltage drop inside the dc-dc converter makes the dc voltage v_{dc2} decrease. The minimal value of the dc voltage v_{dc2} was 77 V, which is lower by 5 Vthan the required peak voltage of 82 V.

In Fig. 8, the zero-sequence voltage v_{C0} , calculated by (2), was superimposed. As a result, the three-phase compensating voltages v_{Cu} , v_{Cv} , and v_{Cw} were balanced in amplitude, and the peak value was half the voltage sag, i.e., 41 V. Moreover, the minimal value of the dc voltage increased to 79 V by 2 V. Thus, the compensating voltage v_C was more purely sinusoidalthan those in Fig. 7. The rms value of the supply current i_S was 15 A before the occurrence of the voltage sag, and it increased to 18.5 A during the voltage sag. The dc-voltage ripples present in the dc voltage v_{dc2} were observed to be ±2.5 V from Fig. 8, and its theoretical value is obtained by (10) as follows:

$$\pm \frac{50\% \times 200V \times 18.5A}{4\sqrt{3} \times 2\pi \times 50Hz \times 5.4mF \times 81.5F} = \pm 1.9V$$

This theoretical value agrees with the experimental one with an acceptable difference.

Figs. 9 and 10 show the experimental waveforms

under a three-phase voltage sag with a depth of 25%. In Fig. 9, no voltage dip appeared in the three-phase load voltage v_{LN} although no zero-sequence voltage was superimposed, like in Fig. 7. The compensating voltage v_C was the same as the voltages occurring in the supply voltage v_S, and the peak value was $\sqrt{2/3} \times 200\,\text{V} \times 25\% = 41\,\text{V}$.

In Fig. 10, the zero-sequence voltage v_{C0} was superimposed. The compensating voltage v_C had a trapezoidal waveform because a third-order harmonic component was included in the zero-sequence voltage v_{C0}. However, no third-order harmonic component was included in the waveform of v_{LN} because v_{LN} was observed with respect to the load neutral point N. Moreover, it was confirmed by experiment that the third-order harmonic component disappeared from the three-phase line-to-line voltages at the load side, although the waveforms were not included in Fig. 10. The three-phase compensating voltages v_{Cu}, v_{Cv}, and v_{Cw} had the same peak value as 35 V, that was 90% of the voltage sag (= 41 V).

VI. CONCLUSION

This paper has presented a three-phase three-wire lowvoltage DVR that is prominent in using a high-frequency unidirectional isolated dc-dc converter. Using the dc-dc converter makes it possible to remove heavy and bulky line-frequency transformers from the DVR. Moreover, connecting the shunt converter to the load side makes it possible to eliminate expensive energy-storage devices from the DVR. The high-frequency transformer was one hundredth smaller in volume than the corresponding line-frequency transformer.

Experimental results obtained by a 200-V 5-kW laboratory system have verified the viability and effectiveness of the DVR. In the near future, replacing Si devices with SiC devices will bring significant reductions in volume and weight to the dc-dc converter, as well as the series converter.

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