Leakage Reduction in various Logic circuits using VTCMOS technique

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***Abstract*— Using a low supply voltage (V_{DD}) and a low threshold voltage (V_T) in CMOS circuits is an efficient method for reducing the overall power dissipation, while maintaining high-speed performance. Designing the CMOS logic circuits entirely with low V_T transistors will lead to increased sub threshold leakage, and consequently, to higher stand-by power dissipation when the output is not switching. A way to overcome this problem is to adjust the threshold voltages of the transistors in order to avoid leakage in stand-by mode, by changing the substrate bias. To achieve different threshold voltages, a self-substrate bias circuit is used to control the body bias. In the active mode, a nearly zero body bias is applied. While in the standby mode, a deeper reverse body bias is applied to increase the threshold voltage and cut off the leakage current.**

***Keywords*— Variable threshold voltage CMOS, average power consumption, threshold voltage, CMOS**

I. INTRODUCTION

With the rapid progress in semiconductor technology, chip density and operation frequency have increased, making the power consumption in battery operated portable devices a major concern. High power consumption reduces the battery service life. The goal of low power design for battery powered devices is thus to extend the battery service life while meeting performance requirements. Reducing power dissipation is a design goal even for non portable devices since excessive power dissipation results in increased packaging and cooling costs as well as potential reliability problems. IC power dissipation consists of different components depending on the circuit operating mode. First, the switching or dynamic power component dominates during the active mode of operation. Second, there are two primary leakage sources, the active component and the standby leakage component. The standby leakage may be made significantly smaller than the active leakage by changing the body bias conditions.

II. POWER DISSIPATION IN CMOS

Power has a direct impact on the system cost. If an IC is consuming more power, then a better cooling mechanism would be required to keep the circuit in normal conditions. Otherwise, its performance is degraded and on continuous use it may be permanently damaged.

When V_{in} = 0, the NMOST is in cutoff mode and when $V_{in}=V_{DD}$, the PMOST is in cutoff. Hence with the input stable at either 0 or V_{DD}, no current flows from V_{DD} to ground. A very small amount of power dissipation, though takes place. This is due to the leakage current.

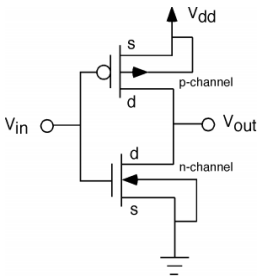

Fig. 1 CMOS inverter

With V_{in} = 0, the PMOST is conducting and NMOST is cutoff. The output capacitor is charged up to V_{DD}. As V_{in} is increased beyond V_T, the NMOST starts to come out of cutoff and enters the saturation region. The output capacitor starts to discharge through the NMOST and V_{out} decrease.

While changing the Vin from 0 to Vdd, current flows consists of a Vdd to ground component and an output capacitor charging component. In either case the two components of current flow give rise to power dissipation, referred to as dynamic power dissipation, as it occurs when the gate output is changing. The component of power dissipation due to flow of current from Vdd direct to ground is called short circuit power dissipation. The power dissipated in charging and discharging the load capacitance is called switching power.

A. Static power dissipation

Static power dissipation in CMOS is due to the leakage current or other current drawn continuously from the power supply. There is some small static dissipation due to reverse bias leakage between diffusion regions and the substrate. In addition, sub threshold conduction can contributes to the static dissipation. Total static power dissipation Ps is obtained from:

Ps = leakage current * supply voltage

B. Dynamic power dissipation

When a transition from either '0' to '1' or alternatively, from '1' to '0', both n and p-transistors switches from their stable states and circuit operates called in active mode. Dynamic power dissipation can be given as:

$$P_d = C_L . V_{DD}^2 . f_{pd}$$

Where C_L is load Capacitance, V_{DD} denotes the supply voltage and f_p is the switching frequency.

C. Short-circuit dissipation

Both n and p transistors are on for a short period of time when transition takes place from '0' to '1' or alternatively '1' to '0'. This results in a short current pulse from V_{DD} to ground. The short circuit dissipation is given by:

$$P_{SC} = I_{SC} . V_{DD}$$

Where I_{SC} is the short circuit current and V_{DD} is supply voltage.

The total power dissipation is given by

$$P_{total} = P_S + P_d + P_{SC}$$

III. Sources of Leakage Power

There are four main sources of leakage current in a CMOS transistor :

1. Reverse biased junction leakage current (IREV)
2. Gate induced drain leakage (IGIDL)
3. Gate direct tunneling leakage (IG)
4. Sub threshold (weak inversion) leakage (ISUB)

A. Junction leakage

The junction leakage occurs from the source or drain to the substrate through the reverse biased diodes when a transistor is OFF. A reverse biased pn junction leakage has two main components: one is minority carrier diffusion/drift near the edge of the depletion region, the other is due to electron hole pair generation in the depletion region of the reverse biased junction. For instance, in the case of an inverter with low input voltage, the NMOS is OFF, the PMOS is ON, and the output voltage is high. Subsequently, the drain to substrate voltage of the OFF NMOS transistor is equal to the supply voltage. This results in a leakage current from the drain to the substrate through the reverse biased diode.

B. Gate induced drain leakage (GIDL)

The gate induced drain leakage (GIDL) is caused by high field effect in the drain junction of MOS transistors. For an NMOS transistor with grounded gate and drain potential at $V_{DD,}$ significant band bending in the drain allows electron hole pair generation through avalanche multiplication and band to band tunneling. A deep depletion condition is created since the holes are rapidly swept out to the substrate. At the same time, electrons are collected by the drain, resulting in GIDL current. Thinner oxide and higher supply voltage increase GIDL current.

C. Gate direct tunneling leakage

The gate leakage flows from the gate through the "leaky" oxide insulation to the substrate. In oxide layers thicker than 3-4nm, this kind of current results from the Fowler Nordheim tunneling of electrons into the conduction band of the oxide layer under a high applied electric field across the oxide layer. For lower oxide thicknesses (which are typically found in 0.15um and lower technology nodes), however, direct tunneling through the silicon oxide layer is the leading effect. The magnitude of the gate directs tunneling current increases exponentially with the gate oxide thickness t_{ox} and supply voltage V_{DD}.

D. Sub threshold leakage

The sub threshold leakage is the drain source current of transistor operating in the weak inversion region. Unlike the strong inversion region in which the drift current dominates, the sub threshold conduction is due to the diffusion current of the minority carriers in the channel for a MOS device. I_{SUB} is calculated by using the following formula:

$$I_{ds} = u_o C_{ox} (W/L) (m-1)(V_t)^2 \; e^{(Vgs - Vth)/ mVt} (1-e^{-Vds/Vt})$$

Where

$$m=1+(C_{dm}/C_{ox}) =1+(3t_{ox} /w_{dm}$$

Where:

V_{th}= The threshold voltage

V_t= The thermal voltage

C_{ox}= Gate oxide capacitance

u_o= zero bias mobility

m=The sub threshold swing coefficient (also called body effect coefficient)

W_{dm}= The maximum depletion layer width

t_{ox}= the gate oxide thickness

C_{dm}= The capacitance of the depletion layer

IV. VTCMOS TECHNIQUE

The threshold voltage V_T of an MOS transistor is a function of its source to substrate voltage $V_{SB.}$ In conventional logic circuits, the substrate terminal of all NMOS transistors are connected to ground potential, while the substrate terminal of all PMOS transistors are connected to V_{DD}. This ensures that the source and drain diffusion regions always remain reverse biased with respect to the substrate, and the threshold voltages of the transistors are not significantly influenced by the body effect. In VTCMOS circuit technique, the transistors are designed inherently with a low threshold voltage, and the substrate bias voltages of NMOS and PMOS transistors are generated by a variable substrate bias control circuit.

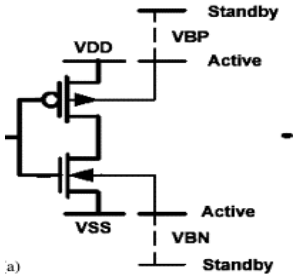

Fig. 2 VTCMOS Structure

When the inverter circuit in Fig. 2 is operating in its active mode, the substrate bias voltage of the NMOS transistor is V_{BN}=0 and the substrate bias voltage of the PMOS transistor is V_{BP}=$V_{DD.}$ Thus, the inverter transistors do not experience any back-gate bias effect. The circuit operates with low V_{DD} and low V_T, benefiting from both low power dissipation (due to low V_{DD}) and switching speed (due to low V_T) [1].

When the inverter circuit is in stand-by mode, however, the substrate bias control circuit generates a lower substrate bias voltage for the NMOS transistor and a higher substrate bias voltage for the PMOS transistor. As a result the magnitudes of the threshold voltages V_{TN} and V_{TP} both increase in the stand-by mode, due to the back-gate bias effect. Since the substrate leakage current drops exponentially with increasing threshold voltage, the leakage power dissipation in the stand-by mode can be significantly reduced with this technique [1].

VTMOS is nothing but an extension of DTMOS in the sense that the substrate voltage differs always by a constant voltage from the gate voltage. As shown in Fig 2(c), by connecting positive bias between gate and substrate for NMOS and negative bias between gate and substrate for PMOS, there is a good reduction of power dissipation in sub-threshold when compared to DTMOS and traditional CMOS. The circuit is named as VTMOS because, we have used the same DTMOS with a biased voltage between gate and substrate .The voltage of each transistor is dynamically adjusted depending on gate voltage, causing the threshold voltage of device to adjust dynamically [2].

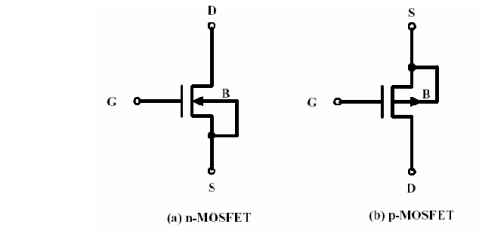

Fig. 3 CMOS Structure

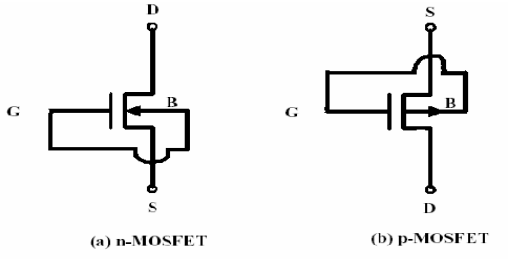

Fig. 4 DTMOS Structure

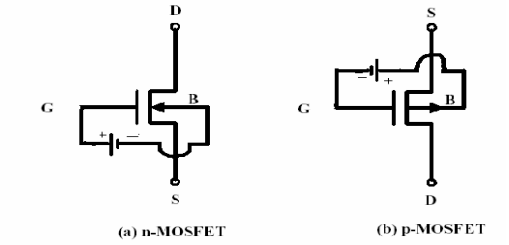

Fig. 5 VTMOS Structure

V. CIRCUIT DESIGN

A. *NAND GATE*

In digital electronics, a NAND gate (Negated AND or NOT AND) is a logic gate which produces an output that is false only if all its inputs are true. A LOW (0) output results only if both the inputs to the gate are HIGH (1); if one or both inputs are LOW (0), a HIGH (1) output results. It is made using transistors.

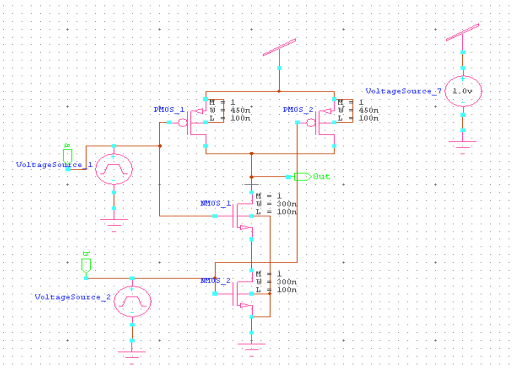

Fig. 6 CMOS NAND GATE

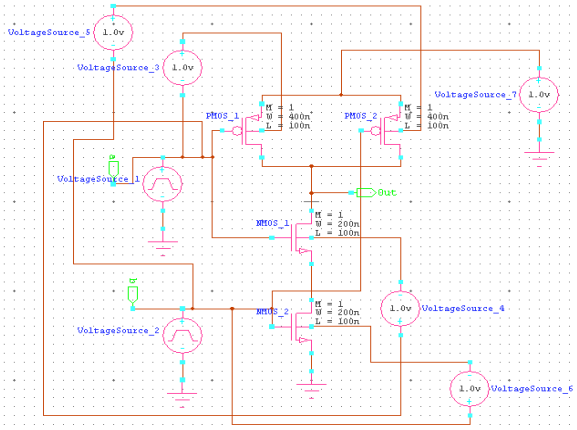

Fig. 7 VTCMOS NAND GATE

B. Even parity genrator

Consider a 3-bit message to be transmitted together with an even parity bit. The three bits, X, Y, and Z, constitute the message and are the inputs to the even parity generator circuit whose output is the parity bit P. For even parity, whenever the message bits(X, Y& Z) have an odd number of 1's, the parity bit P must be 1. Otherwise, P must be0. Therefore, P can be expressed as a three-variable exclusive-OR function:

$$P = X \oplus Y \oplus Z$$

Three-bit Message			Parity bit
X	Y	Z	P
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

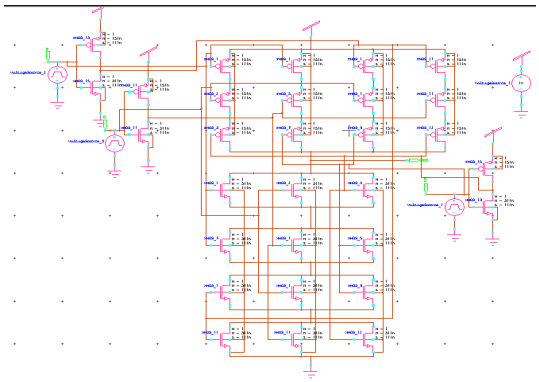

Fig. 8 CMOS EVEN PARITY GENERATOR

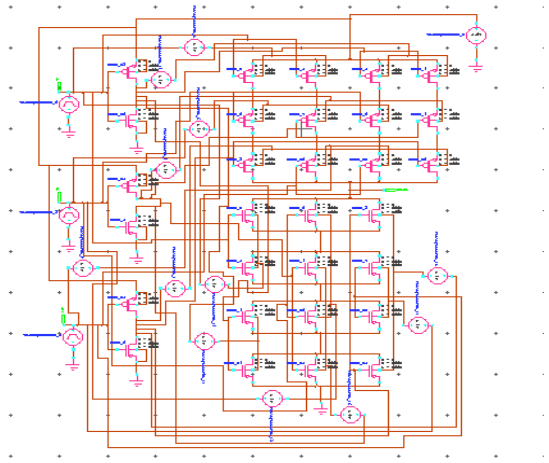

Fig. 9 VTCMOS EVEN PARITY GENERATOR

VI. Result & Simulation

A. Power consumption comparison table and graph for NAND gate:

Technology	CMOS	VTCMOS	%Reduction
180nm	$3.6322e^{-06}$	$1.8110e^{-06}$	50%
130nm	$8.5134e^{-07}$	$3.8695e^{-07}$	55%
100nm	$3.7920e^{-07}$	$1.0313e^{-07}$	73%

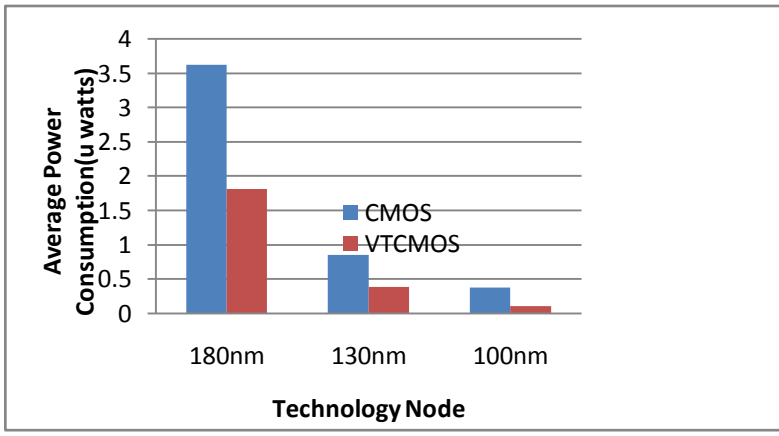

Fig. 10 Comparison of Power Dissipation for NAND Gate

B. Power delay product comparison table and graph for NAND gate:

Technology	CMOS	VTCMOS	%Decrement
180nm	$1.7266e^{-15}$	$1.3650e^{-15}$	21%
130nm	$5.8495e^{-16}$	$1.1002e^{-16}$	81%
100nm	$2.6373e^{-16}$	$2.6834e^{-17}$	90%

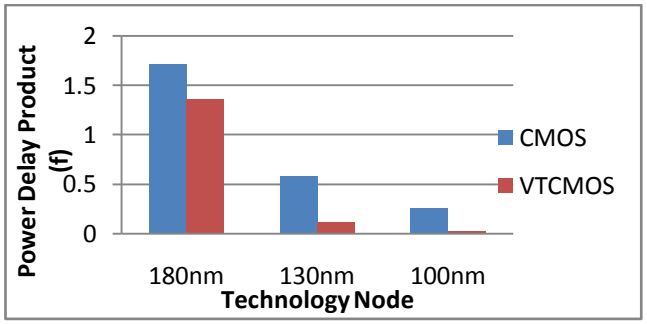

Fig. 11 Comparison of Power Delay Product for NAND GATE

C. Power consumption comparison table and graph for even parity generator:

Technology	CMOS	VTCMOS	%Reduction
180nm	$1.6807e^{-05}$	$1.3156e^{-05}$	22%
130nm	$3.0502e^{-06}$	$2.6965e^{-06}$	12%
100nm	$1.5965e^{-06}$	$1.4495e^{-06}$	9%

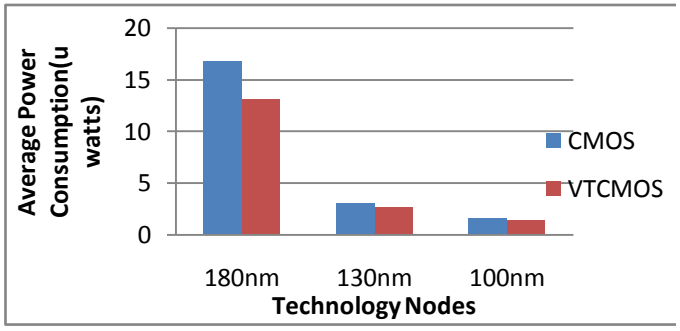

Fig. 12 Comparison of Power Dissipation for Even Parity Generator

D. Power delay product comparison table and graph for even parity generator:

Technology	CMOS	VTCMOS	%Increment
180nm	$1.2965e^{-14}$	$1.1282e^{-14}$	-12%
130nm	$1.5825e^{-15}$	$1.7237e^{-15}$	9%
100nm	$8.2743e^{-16}$	$8.3286e^{-16}$	0.6%

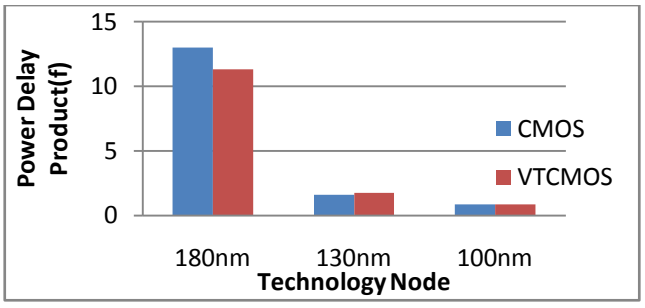

Fig. 13 Comparison of Power Delay Product for Even Parity Generator

VII. Conclusions

Simulation has been done using 180nm, 130nm and 100nm technology node. Average Power Consumption has been reduced with VTCMOS technique. For NAND GATE, it is reduced by 50%, 54% and 73% using 180nm, 130nm and 100nm technology node respectively. For Even Parity Generator, it is reduced by 22%, 12% and 9% using 180nm, 130nm and 100nm technology node respectively.

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