DESIGN AND IMPLEMENTATION OF SINGLE STAGE HIGH POWER FACTOR FULL BRIDGE AC-DC CONVERTER

A.Parthiban, R.Sivakumar, R.Saktheeswaran, Member ISTE, S.Sulthan sikkander badusha
Department of Electrical and Electronics Engineering

ABSTRACT

This paper proposes a novel single-stage high-power-factor ac/dc converter with symmetrical topology. The circuit topology is derived from the integration of two buck-boost power-factor-correction (PFC) converters and a full-bridge series-resonant dc/dc converter. Switch-utilization factor is improved by using two active switches to serve in the PFC circuits. A high power factor at the input line is assured by operating the buck-boost converters at discontinuous conduction mode. With symmetrical operation and elaborately designed circuit parameters, zero-voltage-switching on all the active power switches of the converter can be retained to achieve high circuit efficiency. The operation modes, design equations and design steps for the circuit parameters are proposed. A prototype circuit designed for a 80W dc output was built and tested to verify the analytical predictions. Satisfactory performances are obtained from the experimental results.

I.INTRODUCTION

Traditionally, an ac/dc converter consists of a diode-bridge rectifier followed by a bulky capacitor and a high-frequency dc/dc converter. This kind of converter inevitably introduces highly distorted input current, resulting in a large amount of harmonics and a low power factor. In order to prevent distorting the AC line current, standards of the harmonic regulation such as IEC 61000-3-2 and IEEE 519 are enacted to limit the input current harmonics and to guarantee a power factor of 0.9 at least. With the goal to comply with the more stringent regulations on current harmonics and to improve the power factor, an additional ac/dc conversion stage of power-factor-correction (PFC) is required to cascade in front of the dc/dc converter. It leads to a two-stage approach which includes a PFC stage to shape the input current into a sinusoidal waveform and a dc/dc conversion stage to regulate the output voltage. In spite of its good performance, the two-stage approaches require more circuit components and two power-conversion processes, resulting in higher cost and lower efficiency.

II.ARCHITECTURE & WORKING

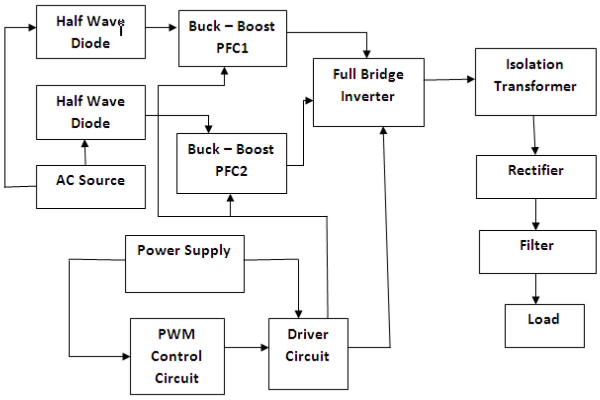

Fig .1 Architecture

The above diagram shows the arrangement of a proposed system. The single phase AC supply is converted into DC and applied to boost converter. The switch is controlled by means of PWM technique. Hence controlled DC voltage is applied to the Load.

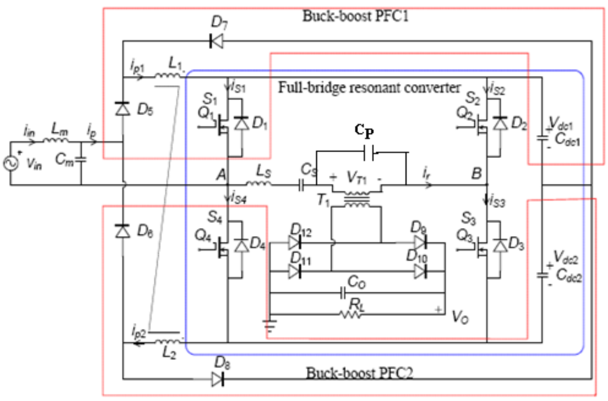

Fig.2 Circuit Diagram

There are six modes of operation in this proposed converter

MODE I

This mode begins at the instant of turning off the transistors (Q2 and Q4). Since the load resonant circuit is designed to represent an inductive load, the load resonant current ir (Resonant Current) is negative at this switching-off instant. The diodes (D1 and D3) are forced to free wheel ir (Resonant Current). The drain-to-source voltages (Vds1 and Vds3) of Q1 and Q3 are both clamped to -0.7V. The voltage across the load resonant circuit (vAB) is nearly equal to the dc-link voltage Vdc, which is the sum of Vds1 and Vds3. After the dead time, the transistors (Q1 and Q3) are activated by the gated signals ($v$gs1 and $v$gs), but they still remain off. The voltage imposes on the inductor L1 is approximately equal to the rectified line voltage. Since the PFC converter is designed to operation at DCM, the inductor current ip1 increases linearly from zero with a rising slope, which is proportional to the line voltage. When the sum of ir (Resonant Current) and ip1 (inductor current) becomes positive, Q1 is turned on approximately at zero voltage.

MODE II

During this mode, ir (Resonant Current) is still negative. Parts of ip1 (inductor current) flow through Q1, while its residual is equal to ir (Resonant Current), which flows through D3 and the line-voltage source. This mode ends when ir (Resonant Current) passes zero and becomes positive. Thereafter, Q3 is turned on approximately at zero voltage to carry ir (Resonant Current)

MODE III

During this mode, Q1 and Q3 are kept at ON state. Since the line voltage keeps applying on L1, ip1 (inductor current) increases continuously and flows through Q1, Current ir (Resonant Current) is positive and flows through Q1 and Q3.

MODE IV

This mode begins when Q1 and Q3 are turned off. At the switching-off instant, ip1 (inductor current) reaches its peak, and ir (Resonant Current) is positive. Current ir (Resonant Current) will freewheel through D2 and D4 to charge Cdc1 and Cdc2. The drain-to-source voltages (Vds2 and Vds4) of (Q2 and Q4) are both clamped to -0.7V. The voltage vAB is nearly equal to –Vdc. After the dead time, the transistors (Q2 and Q4) are activated by the gated signals ($v$gs1 and $v$gs), but they still remain off. In order to make the PFC perform as a buck-boost converter. Vdc1 and Vdc2 are both designed to be higher than the amplitude of the line voltage. Then diode D5 is reversed-biased, and ip1 (inductor current) will flow through diode D7 to charge Cdc1. The voltage across L1 is –Vdc1; therefore, ip1 (inductor current) starts to decrease linearly. Since the peak of ip1 (inductor current) is proportional to the rectified input voltage, the duration for ip1 (inductor current) declining to zero is not a constant but varies with the rectified input voltage. Thus there are two possible modes following *Mode IV*, depending on which current of ip1 (inductor current) or ir (Resonant Current) reaches zero first.

MODE V

When the rectified input voltage is at high level, the peak value of ip1 (inductor current) is high. On this condition, ir (Resonant Current) declines to zero before ip1 (inductor current) does. When ir (Resonant Current) resonates to pass zero, the circuit operation enters *Mode V-a.* At this instant, D2 and D4 turn off naturally, and Q2 and Q4 are turned on at nearly zero voltage to carry ir (Resonant Current). During this mode, ip1 (inductor current) decreases continuously. This mode ends when ip1 (inductor current) decreases to zero.

On the contrary, when the rectified input voltage is at low level. The peak of ip1 (inductor current) is small and declines to zero before ir (Resonant Current) resonates to zero. The circuit operation will enter *Mode V-b* when ip1 decreases to zero. In this mode, D7 is off, and ir (Resonant Current) keeps flowing through D2 and D4 . This mode ends at the time when ir resonates to zero. Then Q2 and Q4 are turned on at zero voltage to carry ir (Resonant Current).

MODE VI

During this mode, ir (Resonant Current) is negative and flows through Q2 and Q4. The capacitors (Cdc1 and Cdc) supply energy to the load resonant circuit. When (ϑgs2 and ϑgs) go to zero, Q2 and Q4 are turned off, and *Mode VI* ends. The circuit operation returns to *Mode I* of the next high-frequency cycle.

III SIMULATION CIRUIT DIAGRAM

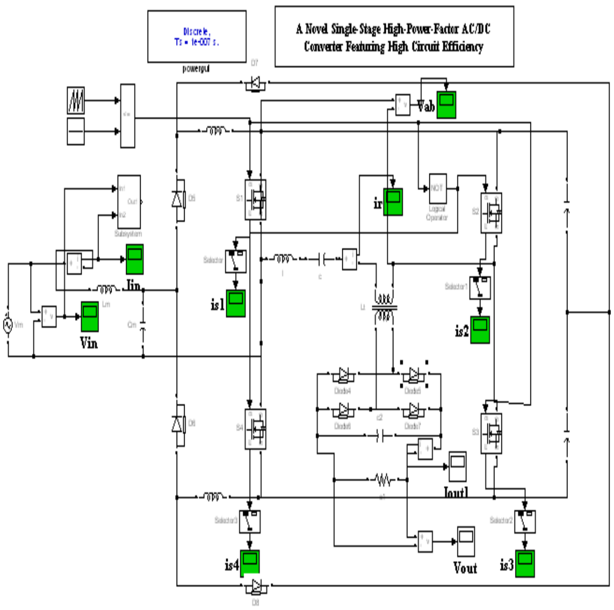

Fig.3 Simulation Circuit Diagram

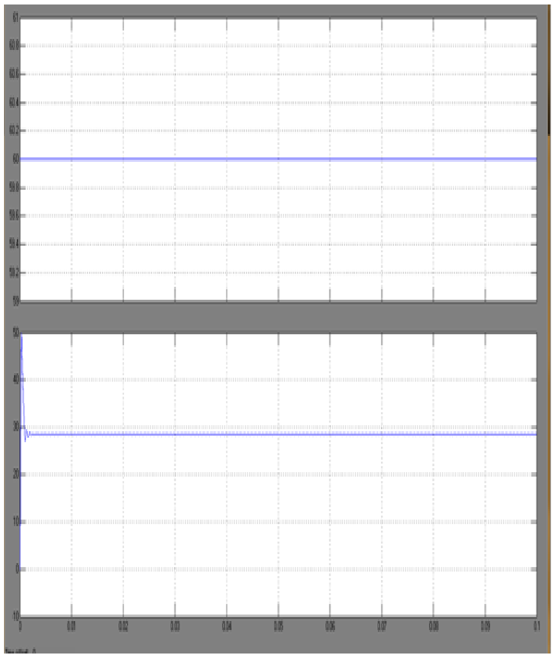

Fig.4 Input and Output Voltages

When a boost converter operates in continuous mode, the current through the inductor (I_L) never falls to zero. The above figure shows the typical waveforms of voltage in a converter operating in this mode. The output voltage can be calculated. During the On-state, the switch Q is closed, which makes the input voltage (V_i) appear across the inductor, which causes a change in current (I_L) flowing through the inductor during a time period (t).

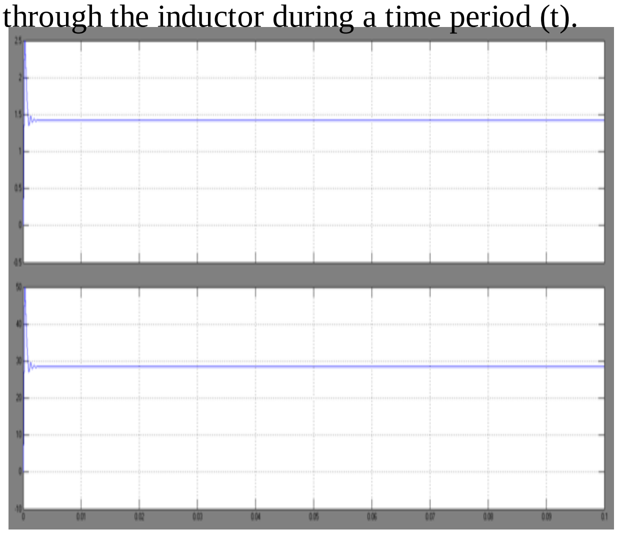

Fig.5 Output Voltage and Output Current

IV CONCLUSION

A new AC-DC single-stage PWM full-bridge converter is proposed in the paper. The outstanding features of the converter are that it can operate with an excellent input power factor, and a DC bus voltage that is always less than 450 V and that has much less variation with line and load change than boost-type single-stage converters. In the paper, the operation of the converter was explained, its design was discussed, and experimental results that confirmed its feasibility were presented.

A novel single-stage ac/dc resonant converter with symmetrical topology has been presented. The proposed circuit was derived by integrating two buck–boost PFCs and a full-bridge series resonant converter. The buck–boost PFC converters operated at DCM to achieve an HPF.

A prototype circuit designed for a 100-W dc load was built and measured to verify the theoretical analyses. ZVS can be retained on all the active power switches to reduce the switching losses. In addition, the conduction losses were also effectively reduced. The experimental results show that the converter performs satisfactorily. A nearly unity power factor and a THD less than 7% can be achieved. The converter has a high circuit efficiency of 0.88 at a rated output power

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A.Parthiban received the B.E degree from Anna University Chennai, in 2006 and the M.E degree from Sathyabama University Chennai, in 2012. He is currently working as Assistant Professor in Sri Venkateshwara Institute of Science and technology under Anna University, Chennai.

R.Sivakumar received the B.E degree from Periyar University Salem, in 2003 and the M.E degree from Anna University Chennai, in 2012. He is currently working as Assistant Professor in S.R.I College of Engg & Tech under Anna University, Chennai and 6 years of Teaching Experience in engineering Discipline.

R.Saktheeswaran received the B.E degree from Anna University Chennai, in 2008 and the M.E degree from Sathyabama University Chennai, in 2012. He is currently working as Assistant Professor in Roever College of Engg & Tech under Anna University, Chennai. He is a life time member of ISTE.

S.Sulthan sikkander badusha received the B.E degree from Anna University Chennai, in 2005 and the M.E degree from Anna University Chennai, in 2008. He is currently working as Assistant Professor in Roever College of Engg & Tech under Anna University, Chennai.