Dual Output Inverter for Minimized Total Harmonic Distortion using SVM

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Abstract- Nowadays Dual output inverter is mostly proposed as nine-switch inverter and nine-switch z-source inverter. This paper deals with minimization of total harmonic distortion using Space Vector Modulation (SVM) of nine-switch inverter and nine-switch z-source inverter. With this proposed method the sum of modulation indices can be increased upto 17% in contrast with the conventional scheme, in which the sum of modulation indices is same or less than unity. The SVM switching pattern proposed here lessen the cost of power devices along with thermal heat effect and also reduces the no.of. semiconductor switching. The extra voltage available for a given input dc voltage translates to a higher torque. The proposed feature will be advantageous for high power inverter applications where cost and efficiency are key design factors. Furthermore a novel SVM is proposed for reducing total harmonic distortion. The proposed SVM's performance for both nine-switch inverter and nine-switch z-source inverter is verified by simulation

Keywords
Space Vector Modulation (SVM), Nine-switch inverter, nine switch Z-source inverter.

I. INTRODUCTION

Inverters are used as power controller for ac load such as motor drivers. In many cases, there are two or more ac loads, which require independent control. The conventional solution is to use separate inverters. This increases cost and volume of system. A dual output inverter has been presented in using only nine semiconductor switches (see Fig. 1). This inverter is known as nine-switch inverter and is also used as an ac/ac converter. The nine-switch inverter is composed of two conventional inverters with three common switches. In nine-switch inverter, sum of modulation index of two outputs must be less than or equal to one. Therefore, voltage amplitude of outputs is smaller, compared with two separate inverters. To remedy this problem, this paper proposes using an impedance source (z-source) network in front of nine-switch inverter as a dc/dc boost converter (see Fig. 2). Z-source network was used as front-end boost converter for a conventional inverter, for the first time. This inverter was called z-source inverter and has been proposed for fuel cell, photovoltaic, and wind turbine systems [6]–[8]. The z-source network also was used in other converters such as three-level inverters.

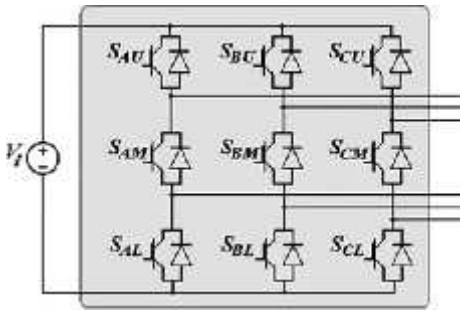

Fig.1.Nine-switch inverter

In [1], carrier-based pulse width modulation (PWM) methods have been proposed for nine-switch inverter. This paper proposes space vector modulation (SVM) methods for the aforementioned nine-switch and nine-switch-z-source inverters. In order to reduce number of semiconductor switching and total distortion harmonic (THD), some specific switching patterns for SVM are proposed. This paper is organized as follows. Section II describes the carrier-based PWM control method for nine-switch inverter. Section III describes the proposed SVM for nine-switch inverter, as well as two special SVMs with minimum switching number and THD. The proposed SVM is developed for nine-switch z-source inverter in Section IV. Section V describes maximum gain. Finally, Section VI presents simulation and experimental results.

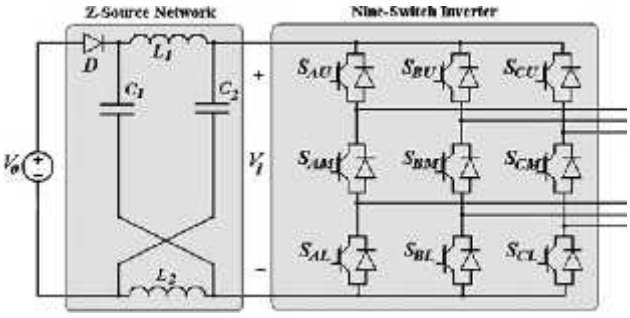

Fig.2. Nine-switch-z-source inverter.

II. CARRIER-BASED PWM METHOD

The carrier-based PWM control method for nine-switch inverter is shown in Fig. 3. There are two reference signals (upper and lower) for each phase. The upper and lower reference signals are related to upper and lower outputs respectively.

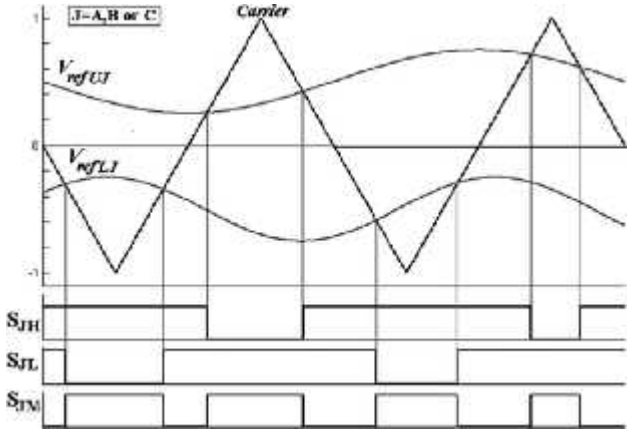

Fig.3. Carrier based PWM method for nine-switch inverter

The gate signal for upper switch of a leg is generated by comparing the carrier signal and upper reference signal of the related phase ($V_{ref\ UJ}$). Similarly, the gate signal for lower switch is generated from the carrier signal and lower reference signal of the related phase ($V_{ref\ LJ}$). The gate signal for mid switch is generated by the logical XOR of the gate signals for upper and lower switches. With this method, always two switches are ON in each leg.

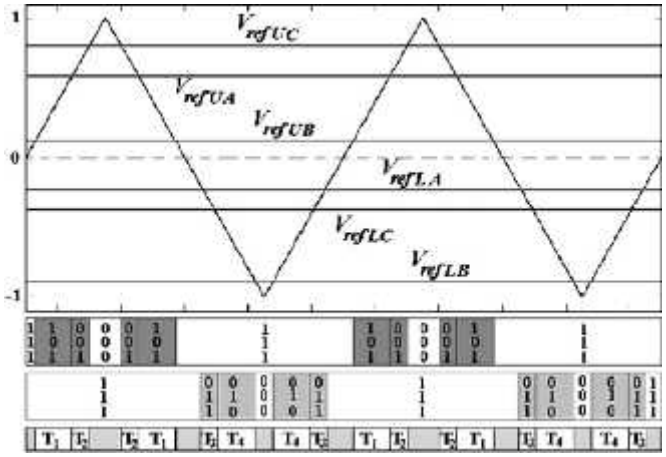

Fig.4. Carrier-based PWM method switching vector

Fig. 4 shows carrier-based PWM method switching vectors. There are six vectors in each switching cycle for both outputs: two nonzero vectors, one zero vector 0 0 0, two non-zero vectors and one zero vector 1 1 1 {two active—short zero (0 0 0)—two active—long zero (1 1 1)}. In an active vector, output load is connected to the dc input source, while in a zero vector, the output load is short-circuited. When one of the outputs has an active or short zero (0 0 0) vector, the other output has long zero (1 1 1) vector.

III. SVM FOR NINE-SWITCH INVERTER

In regard to Fig. 3, each leg can be in three different semiconductors ON-OFF position. These position can be called {1}, {0}, and {−1}, as is illustrated in Table I. In Table I, *J* refers to leg *A*, *B*, or *C* and *U*, *M*, *L* refers to upper, mid, and lower semiconductor, respectively.

Table I
Semiconductors ON-OFF Position of Legs

ON-OFF Position	S_{JU}	S_{JM}	S_{JL}
1	**ON**	**OFF**	**ON**
0	**OFF**	**ON**	**ON**
-1	**ON**	**ON**	**OFF**

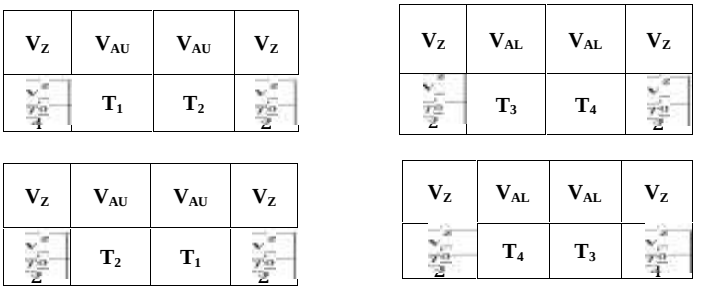

Fig. 5. Typical SVM switching vector sequence

The combination of switching vector of both outputs in Fig. 4 creates a specific sequence as shown in Fig. 5. This sequence is used to design SVM method.

TABLE II
SVM SWITCHING VECTORS

Vector	Leg A	Leg B	Leg C	Type
1	1	0	0	Upper Active
2	1	1	0	
3	0	1	0	
4	0	1	1	
5	0	0	1	
6	1	0	1	
7	-1	1	1	Upper Active
8	-1	-1	1	
9	1	-1	1	
10	1	-1	-1	
11	1	1	-1	
12	-1	1	-1	
13	1	1	1	Zero
14	0	0	0	
15	-1	-1	-1	

There are 12 vectors in each switching cycle: {two upper active (*VAU*)—zero (*VZ*)—two upper active (*VAU*)—zero (*VZ*)—two lower active (*VAL*)—zero (*VZ*)—two

lower active (*VAL*)—zero (*VZ*)}. The switching vectors are listed in Table II. The vectors *V*1–*V*6 are upper active vectors. In these vectors, the upper output is in active state, and the lower output is in zero state. There is an inverse logic in lower active vectors (*V*7–*V*12). In zero vectors (*V*13–*V*15), both outputs are in zero state.

Table II does not include all possible variations of switching states {1}, {0}, and {−1}. Since a vector including {−1} and {0} connects both loads to the dc source at the same time, the loads lose their independence and they cannot have independent frequencies. This is the reason for avoiding a vector that includes combinations of {−1} and {0}. In none of the switching vectors as listed in Table II, both outputs are not in an active state at the same time. However, in vectors including both {−1} and {0} such as {−1, 1, 0}, both outputs are in active state. These vectors are ignored because there are not all combinations of active vectors for both outputs. For example, if upper output be in active vector (1 1 0), lower output can be in vectors (0 0 0), (1 0 0), (0 1 0), or (1 1 0) as shown in Fig. 6. However, vectors (0 1 1), (0 0 1), and (1 0 1) are not available for lower output. Therefore, outputs cannot be controlled independently.

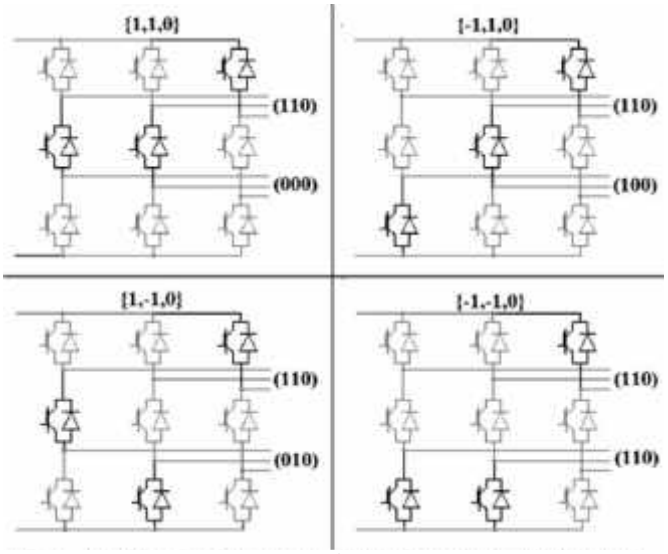

Fig. 6. Available switching vectors of nine-switch inverter while upper output is in active vector (1 1 0).

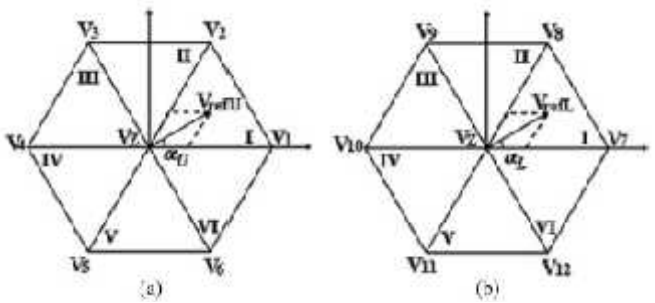

Fig. 7. Space vector diagrams for nine-switch inverter. (a) Upper output. (b) Lower output.

To determine the proper active vectors, two space vector diagrams are proposed as shown in Fig. 7. The diagrams (a) and (b) are used to determine the upper and lower active vectors, respectively. The SVM active vectors are determined with regard to location of upper reference signal $(\bar{V}_{\text{ref U}})$ in the diagram (a) and lower reference signal $(\bar{V}_{\text{ref L}})$ in the diagram (b). The reference signals for the upper and lower outputs are defined as

$$\bar{V}_{\text{ref U}} = V_{\text{ref U}} \angle\alpha_U \quad \ldots\ldots(1)$$

$$\bar{V}_{\text{ref L}} = V_{\text{ref L}} \angle\alpha_L \quad \ldots\ldots(2)$$

where

$$\angle\alpha_U = 2\pi f_U t + \phi_U \quad \ldots\ldots(3)$$

$$\angle\alpha_L = 2\pi f_L t + \phi_L \quad \ldots\ldots(4)$$

where f_U , f_L are the frequencies, and ϕ_U , ϕ_L are the phases. All zero vectors *V*13, *V*14 , and *V*15 can be used for zero states. The type of zero vectors can be selected based on control goals and optimizations such as minimum number of semiconductor switchings.

The switching time intervals of vectors are calculated as

$$T_1 = \frac{\sqrt{3}}{2} m_U T \sin\left(\frac{\pi}{3} - \alpha_U\right) \quad \ldots\ldots(5)$$

$$T_2 = \frac{\sqrt{3}}{2} m_U T \sin(\alpha_U) \quad \ldots\ldots(6)$$

$$T_3 = \frac{\sqrt{3}}{2} m_L T \sin\left(\frac{\pi}{3} - \alpha_L\right) \quad \ldots\ldots(7)$$

$$T_4 = \frac{\sqrt{3}}{2} m_L T \sin(\alpha_L) \quad \ldots\ldots(8)$$

$$T_0 = T - T_1 - T_2 - T_3 - T_4 \quad \ldots\ldots(9)$$

where *T*1, *T*2 are the time interval of upper active vectors, *T*3, *T*4 are time of lower active vectors, *To* is time of zero vectors and *T* is switching period. m_U and m_L are upper and lower modulation indices, respectively, and defined by

$$m_U = 2\frac{V_{\text{ref U}}}{V_i} \quad \ldots\ldots(10)$$

$$m_L = 2\frac{V_{\text{ref L}}}{V_i} \quad \ldots\ldots(11)$$

The sum of active vector time intervals must be less or equals to *T*. Thus, the following constrain must be satisfied (see Appendix):

$$m_U + m_L \leq \frac{2}{\sqrt{3}} \approx 1.155 \quad \ldots\ldots(12)$$

Equation (12) clearly indicates that in the proposed SVM scheme, sum of modulation indices increases about 15%—a very important feature to provide higher torque for a given input dc-voltage. In the case of washing machines, the above capability translates to higher machine capacity (in terms of cloth load) at high spin speed (e.g., 1800 r/min)—an important product feature in market place.

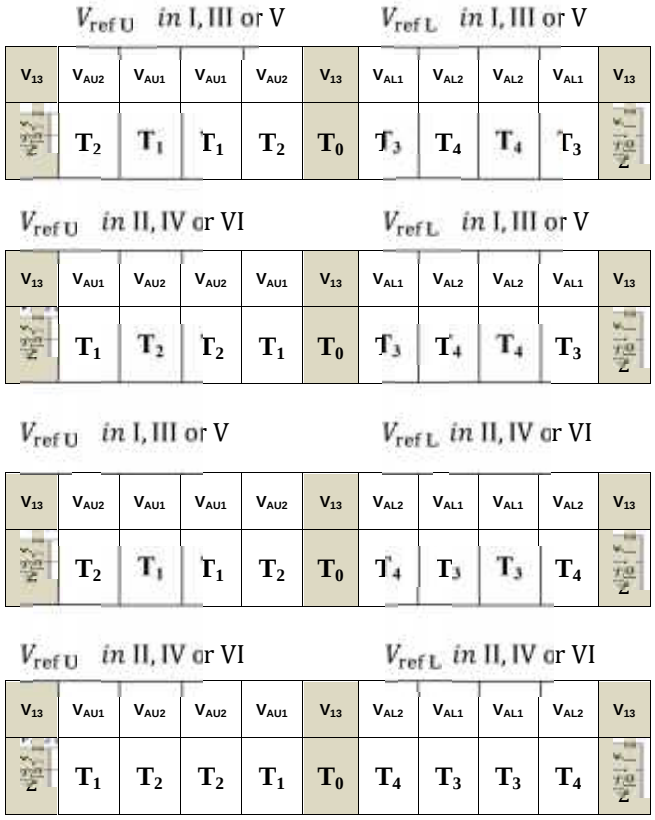

Fig. 8. SVM with reduced number of semiconductor switching.

A switching vector sequence for the proposed SVM is shown in Fig. 8. This switching sequence is developed to reduce the number of semiconductor switching. The zero vectors are placed just between two upper and lower active vectors. In upper active vectors, legs are in state {1} or {0} and in lower active vectors, legs are in state {1} or{−1}. If V_{13} zero vector is placed between the active vectors, minimum number of switching is required. While if V_{14} or V_{15} zero vectors are used, number of switching is increased.

There are two odd active vectors (V_1, V_3, V_5, V_8, V_{10}, and V_{12}) and two even active vectors (V_2, V_4, V_6, V_7, V_9 , and V_{11}) in a switching sequence. In an even active vector, two legs are in state {1}, while in an odd active vector only one leg is in state{1}. If even active vectors are placed next to V_{13}, number of switching will be reduced even more (see Fig. 8).

There are other possible switch generation methods too, e.g., a switching method, to reduce THD. To minimize THD, active vectors for each output should be centrally placed within the switching period [11]. Fig. 9 shows a switching vector sequence that shifts active vector into center of switching period, hence reducing THD. In this sequence, zero vectors are inserted between active vectors. In Fig. 9, V_{14} is inserted between upper active vectors and V_{15} is inserted between lower active vectors.

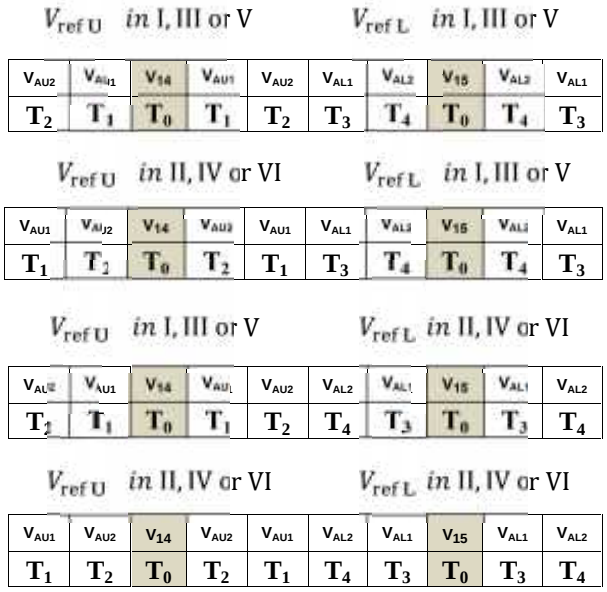

Fig. 9. SVM with reduced THD.

IV. NINE-SWITCH-Z-SOURCE INVERTER SVM

The nine-switch-z-source inverter is shown in Fig. 2. This inverter has an extra z-source network including two inductors (L_1 and L_2), two capacitors (C_1 and C_2) and a diode (D). The z-source network is similar to a dc/dc boost converter with [12]

$$V_i = BV_o \quad (13)$$

where V_o is input dc voltage and V_i is output of z-source network. B is known as boost factor and is given by following equation:

$$B = \frac{1}{1-2(T_{SC}/T)} \quad (14)$$

where T_{SC} is shoot-through time. In the shoot-through times, the output of z-source network is shorted through the switches of the inverter. During shoot-through state, since the inverte (output of z-source network) is shorted, inverter cannot have an active vector. Therefore a shoot-through state can only occur when the inverter has a zero state. Table III shows all the vectors that the inverter includes zero state and

the z-source network has a shoot-through state. These vectors are known as shoot through vectors. There is a new state (state {2}) in Table III. The ON-OFF position of switches of a leg in state {2} is shown in Table IV. All vectors of Table III can be used for generating a shoot-through state.

TABLE III
SHOOT-THROUGH VECTORS OF NINE-SWITCH Z-SOURCE INVERTER

Vector	Leg A	Leg B	Leg C
16	2	2	2
17	2	2	0
18	2	2	1
19	2	2	-1
20	2	0	2
21	2	1	2
22	2	-1	2
23	0	2	2
24	1	2	2
25	-1	2	2
26	2	0	0
27	2	1	1
28	2	-1	-1
29	0	2	0
30	1	2	1
31	-1	2	-1
32	0	0	2
33	1	1	2
34	-1	-1	2

TABLE IV
ON-OFF POSITION OF SEMICONDUCTOR SWITCHES IN STATE {2}

	S_{JU}	S_{JM}	S_{JL}
2	ON	ON	ON

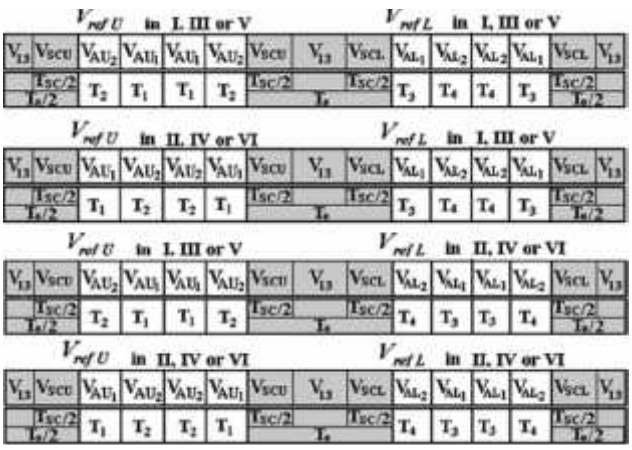

Fig. 10. Nine-switch-z-source inverter SVM with reduced switching.

Fig. 10 shows a SVM vector sequence for nine-switch inverter with reduced number of switching. The sequence is a modified version of Fig. 8. Two shoot-through vectors are placed in both sides of zero vector (V_{13}). Here, the shoot-through vector close to upper active vector is called upper shoot-through vector (V_{SCU}) and the shoot-through vector close to lower active vector is called lower shoot-through vector (V_{SCL}). All vectors listed in Table III can be used as the upper and lower shoot-through vectors. However, vectors V_{27}, V_{30} , and V_{33} are preferred because those vectors have only one state {2} and need less switching. As shown in Fig. 10, even active vectors are placed close to shoot-through vectors (the reason described in Section III). In even active vectors, two legs are in state {1} and one leg is in state {0} or {−1}. On other hand, in shoot through vectors V_{27}, V_{30}, and V_{33}, two legs are in state {1} and one leg is in state {2}. To reduce the number of switching, the two legs in state {1} must have the same state in an even active vector and shoot-through vector close to it. Table V can be used for shoot-through vectors selection.

TABLE V
DETERMINING UPPER AND LOWER SHOOT-THROUGH VECTOR WITH REDUCED NUMBER OF SWITCHING

Section of V_{refU}	V_{SCU}	Section of V_{refL}	V_{SCL}
I	V_{33}	I	V_{27}
II	V_{33}	II	V_{36}
III	V_{27}	III	V_{36}
IV	V_{27}	IV	V_{33}
V	V_{36}	V	V_{33}
VI	V_{36}	VI	V_{27}

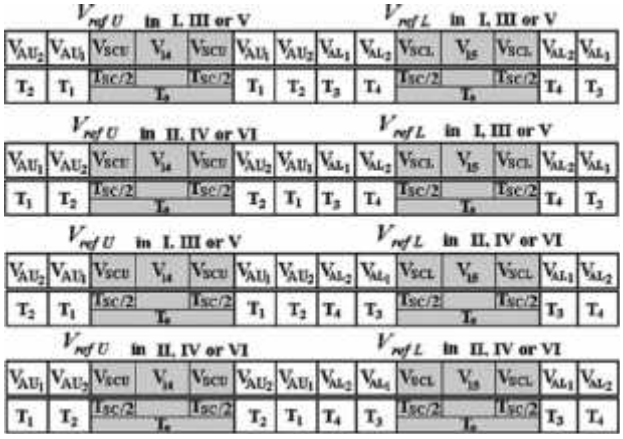

Fig. 11. Nine-switch-z-source inverter SVM with reduced THD.

TABLE VI
DETERMINING UPPER AND LOWER SHOOT-THROUGH VECTOR WITH REDUCED THD

Section of V_{refU}	V_{SCU}	Section of V_{refL}	V_{SCL}
I	V_{26}	I	V_{34}
II	V_{29}	II	V_{34}
III	V_{29}	III	V_{28}
IV	V_{32}	IV	V_{28}
V	V_{32}	V	V_{31}
VI	V_{26}	VI	V_{31}

For reducing THD, switching sequence shown in Fig. 11 is developed for nine-switch-z-source inverter. Similar to Fig. 9, zero vectors and shoot-through vectors are inserted between similar active vectors. Table VI can be used for shoot-through vector selection with reduced THD.

V. MAXIMUM GAIN

The magnitude of peak phase voltage of ac outputs of nine switch inverter can be expressed by

$$V_{acU} = m_U \frac{V_i}{2} \quad \ldots\ldots(15)$$

$$V_{acL} = m_L \frac{V_i}{2} \quad \ldots\ldots(16)$$

According to (12), in nine-switch inverter, sum of modulation indices should be smaller than 1.15. If the same amplitude for both ac outputs is desired, we have

$$V_{acU_{max}} = V_{acL_{max}} = \frac{V_i}{2\sqrt{3}} \quad \ldots\ldots(17)$$

If amplitude of one of the outputs is set to zero, maximum amplitude of other output can be increased

$$V_{ac_{max}} = \frac{V_i}{\sqrt{3}} \quad \ldots\ldots(18)$$

For nine-switch-z-source inverter, the magnitude of peak phase voltage of ac outputs can be expressed by

$$V_{ac_U} = Bm_U \frac{V_0}{2} \quad \ldots\ldots(19)$$

$$V_{ac_L} = Bm_L \frac{V_0}{2} \quad \ldots\ldots(20)$$

The voltage gains can be defined by [13]

$$G_U = Bm_U \quad \ldots\ldots\ldots\ldots (21)$$

$$G_L = Bm_L \quad \ldots\ldots\ldots\ldots (22)$$

Boost factor is limited by voltage rating of semiconductor switches (V_S). For a given voltage rating, maximum boost factor can be calculated by

$$B_{max} = \frac{V_S}{V_0} \quad \ldots\ldots(23)$$

Maximum voltage gain is determined by:

$$G_{max} = B_{max}\, m_{maxB} \quad \ldots\ldots\ldots (24)$$

where m_{maxB} is the maximum possible modulation index, when B is at its maximum value. If the same amplitude for both ac outputs is desired m_{maxB} can be calculated by

$$m_{max}B = \frac{1}{2\sqrt{3}} \left(1/B_{max} + 1\right) \quad \ldots\ldots(25)$$

Thus

$$G_{max} = \frac{1}{2\sqrt{3}} (B_{max} + 1) \quad \ldots\ldots(26)$$

If amplitude of one of the outputs is set to zero, maximum possible modulation index for other output can be determined

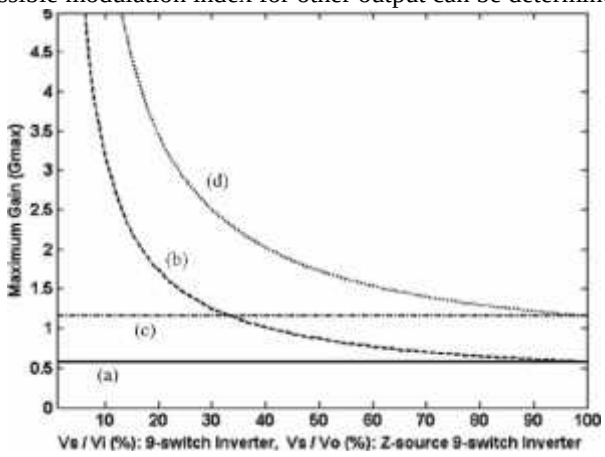

Fig. 12. Maximum voltage gain (G_{max}) versus V_o (for nine-switch inverter) or V_i (for nine-switch-z-source inverter) for a given switch voltage rating (V_S). (a) Nine-switch inverter: equal maximum amplitudes. (b) Nine-switch-z-source inverter: equal maximum amplitudes. (c) Nine-switch inverter: maximum amplitude for one of the outputs. (d) Nine-switch-z-source inverter: maximum amplitude for one of the outputs.

TABLE VII
SIMULATION PARAMETERS

Parameter		Value
Switching Frequency		3 kH
f_U		25 Hz
f_L		50 Hz
R_{load}		5.6 Ohm
L_f		1 mH
C_f		20 uF
Nine-Switch Inverter	m_U	0.35
	m_L	0.55
Nine-Switch Z-Source Inverter	m_U	0.40
	m_L	0.35
	B	1.5

by

$$m_{max}B = \frac{1}{\sqrt{3}} \left(1/B_{max} + 1\right) \quad \ldots\ldots(27)$$

Thus

$$G_{max} = \frac{1}{\sqrt{3}} (B_{max} + 1) \quad \ldots\ldots(28)$$

Fig. 12 shows maximum possible voltage gains for a given switch voltage rating.

VI. SIMULATIONS AND EXPERIMENTAL RESULTS

The proposed SVMs are simulated for nine-switch inverter and nine-switch-z-source inverter. Prototypes of both converters also were built usingDSP for verifying the proposed SVMs. Two similar resistive loads with*LC*filters are connected to the outputs of inverter. Simulation parameters are listed in Table VII.

The nine-switch inverter with input dc source of 150 V is simulated and implemented with reduced number of switching SVM. Figs. 13 and 14 show line–line voltage and phase voltage of both outputs, respectively. It can be seen that both outputs have expected frequencies. The load current is shown in Fig. 15. It can be seen that the load currents have nearly sinusoidal waveforms.

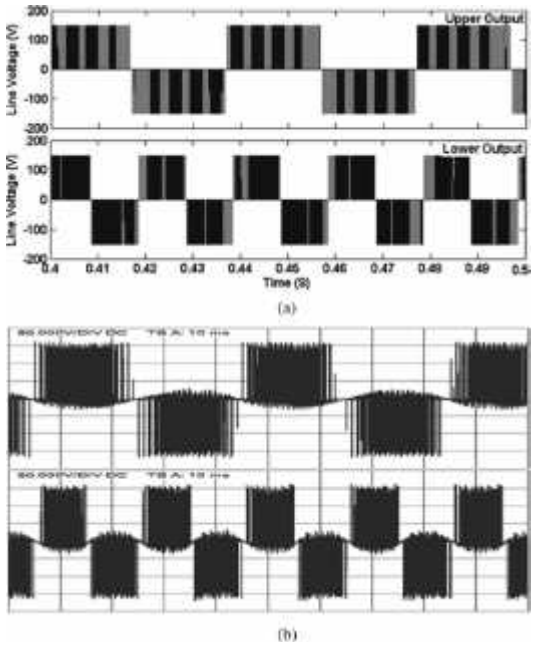

Fig. 13. (a) Line voltage of nine-switch inverter (simulation). (b) Line voltage of nine-switch inverter (experimental), (50 V/DIV, 10 ms/DIV).

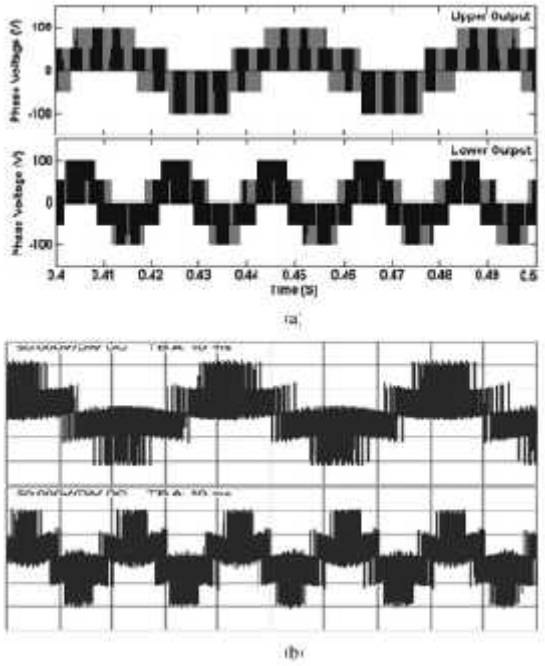

Fig. 14. (a) Phase voltage of nine-switch inverter (simulation). (b) Phase voltage of nine-switch inverter (Experimental), (50 V/DIV, 10 ms/DIV).

In second simulation, a z-source network including L_1 = L_2 = 2 mH and C_1 = C_2 = 2.2 mF was added to nine-switch inverter. An input dc source of 100 V is used. To boost input voltage to 150 V, T_{SC}/T was set to 0.166 considering (14). The output of z-source network (V_i) is shown in Fig. 16. As expected, V_i magnitude changes between 0 and 150V, respectively. Fig. 17 shows z-source network capacitor voltages. The voltage is equal to expected value of 125 V. Capacitor voltage is 0.5 (V_O + V_i), as described in [5]. Figs. 18 and 19 show line–line voltage and phase voltage of both outputs, respectively. The load current is seen in Fig. 20.

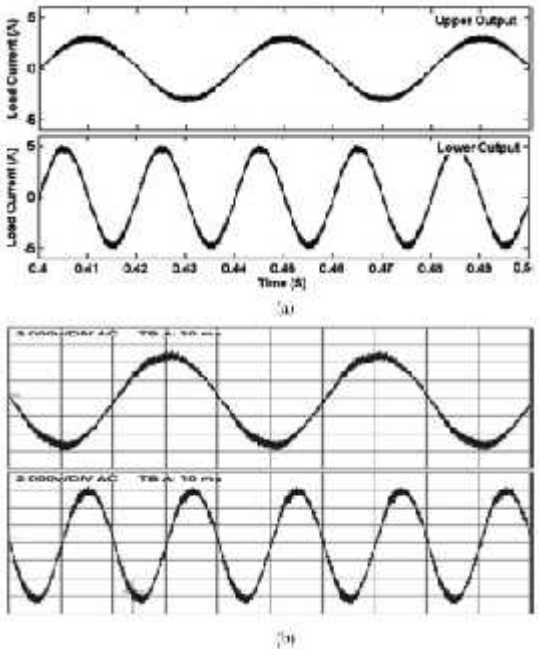

Fig. 15. (a) Output currents of nine-switch inverter (simulation). (b) Output currents of nine-switch inverter (experimental), (2 A/DIV, 10 ms/DIV).

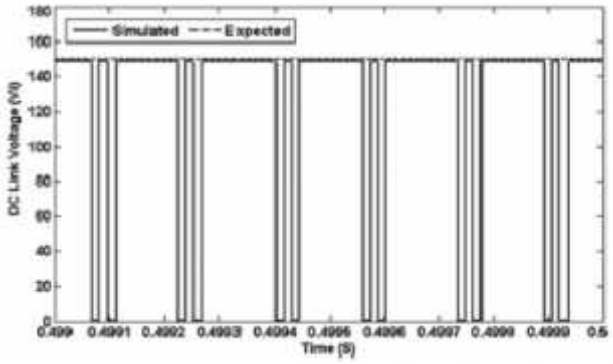

Fig. 16. Output voltage of z-source network (simulation).

Number of switching of semiconductors for nine-switch inverter and z-source-nine-switch inverter using carrier-based PWM and the proposed SVMs are shown in Table VIII. Number of switching for 0.1 s with parameters of Table VII is calculated. As seen in Table VIII, number of switching is considerably reduced using proposed SVMs.

Fig. 21 shows THDof load current versus load current magnitude for four different cases: 1) carrier-basedPWM,2) minimum number of switching SVM, 3) reduced THD SVM, and 4) six switch inverter with SVM. Note that, for six switch inverter, dc bus voltage is set to 75 V, while for nine-switch inverters; dc bus voltage is set to 150 V. It is seen that the reduced THD SVM has best harmonic performance for nine-switch inverters. As seen in Fig. 21, six-switch inverter has better harmonic performance.

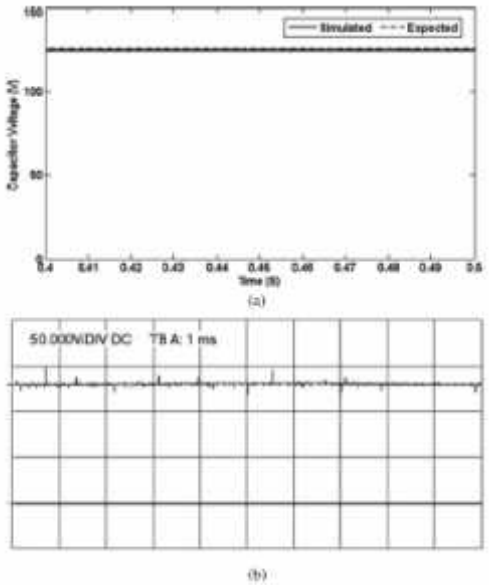

Fig. 17. (a) Capacitor voltage of nine-switch-z-source inverter (simulation). (b) Capacitor voltage of nine-switch-z-source inverter (experimental), (50 V/DIV, 1 ms/DIV).

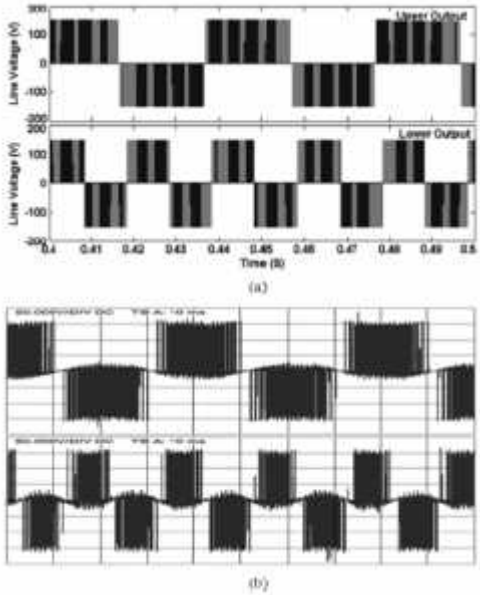

Fig. 18. (a) Line voltage of nine-switch-z-source inverter (simulation). (b) Line voltage of nine-switch-z-source inverter (experimental), (50 V/DIV, 10 ms/DIV).

TABLE VIII
NUMBER OF SEMICONDUCTOR SWITCHING

	SPWM	SVM (Minimum Switching)	SVM (Minimum THD)
Nine-Switch Inverter	3600	2400	3400
Z-Source Nine-Switch Inverter	5400	2400	3400

Main reason is that in nine-switch inverter, active vectors are not centered within the switching period.

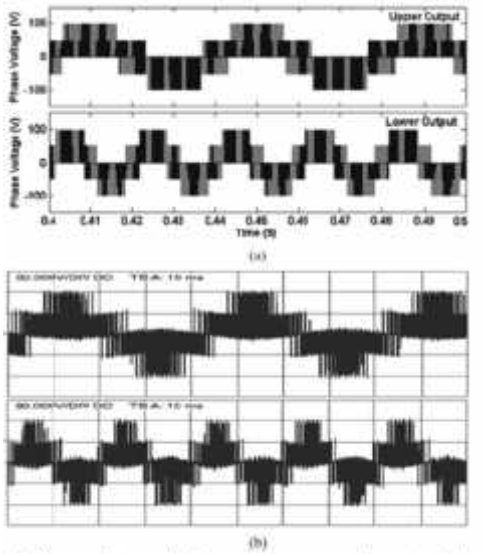

Fig. 19. (a) Phase voltage of nine-switch-z-source inverter (simulation). (b) Phase voltage of nine-switch z-source inverter (experimental), (50V/DIV,10 ms/DIV).

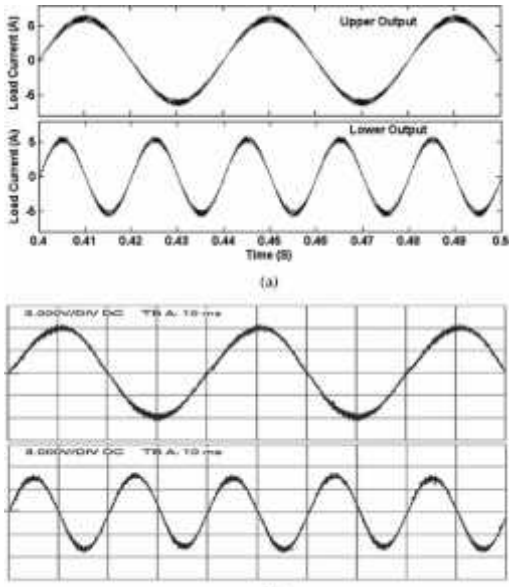

Fig. 20. (a) Output currents of nine-switch-z-source inverter (simulation). (b) Output currents of nine-switch-z-source inverter (experimental), (3 A/DIV,10 ms/DIV).

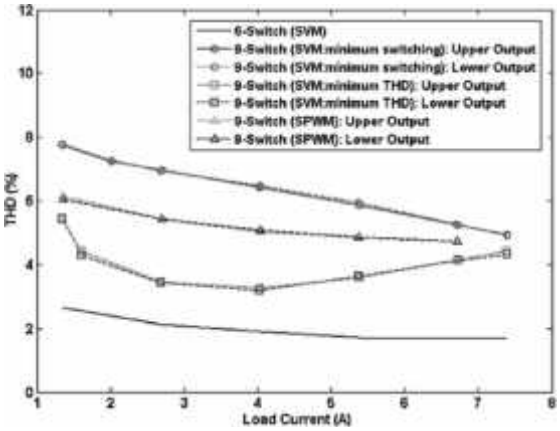

Fig. 21. THD of load current of nine-switch inverter and six-switch inverter.

VII. CONCLUSION

In this paper, the SVM of nine-switch inverter and nine switch-z-source inverter was proposed. Switching sequence of the proposed SVM is composed of the upper active vectors, the lower active vectors and the zero vectors. The upper and lower active vectors are determined via two space vector diagram. The proposed SVM increases sum of modulation indices up to 17%, an important feature in providing higher torque for a given input dc-voltage. The proposed SVM is also developed for nine switch-z-source inverter via extra shoot-through vectors. For both inverters, two SVM algorithms are developed to reduce THD and number of semiconductor switching. The proposed SVMs were simulated for both nine-switch inverter and z-source nine-switch inverter. An experimental setup was developed using a digital signal processor (DSP). The performance of the proposed SVMs was verified using computer simulation, and it was validated using experimental data.

APPENDIX

The sum of active vector time intervals must be less or equals to *T*. Thus

$$(T_1 + T_2 + T_3 + T_4) \leq T. \qquad (A1)$$

From (5)–(8) and (A1) we have

$$\left[m_U \sin\left(\frac{\pi}{3} - \alpha_U\right) + m_U \sin(\alpha_U) + m_L \sin\left(\frac{\pi}{3} - \alpha_L\right) + m_L \sin(\alpha_L)\right] \leq \frac{2}{\sqrt{3}} \qquad (A2)$$

The left term of (A2) can be divided to following two term:

$$A = m_U \sin\left(\frac{\pi}{3} - \alpha_U\right) + m_U \sin(\alpha_U), \qquad 0 \leq \alpha_U \leq \frac{\pi}{3} \qquad (A3)$$

$$B = m_L \sin\left(\frac{\pi}{3} - \alpha_L\right) + m_L \sin(\alpha_L), \qquad 0 \leq \alpha_L \leq \frac{\pi}{3} \qquad (A4)$$

The value of terms *A* and *B* changes regarding to α_U and α_L . Equation (A2) should be true when the terms *A* and *B* have their maximum value. This happens when $\alpha_U = \pi/6$ and $\alpha_L = \pi/6$.

Thus

$$A_{max} = m_U \sin\left(\frac{\pi}{3} - \frac{\pi}{6}\right) + m_U = m_U \qquad (A5)$$

$$B_{max} = m_L \sin\left(\frac{\pi}{3} - \frac{\pi}{6}\right) + m_L = m_L \qquad (A6)$$

Therefore, from (A2)

$$m_U + m_U \leq \frac{2}{\sqrt{3}} \qquad \text{(A7)}$$

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