HIGH PERFORMANCE FPGA Implementation of RS Codec for DVB

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ABSTRACT

Reed Solomon Forward Error Correction (FEC) Codes plays an important role in digital communication and storage systems to increase the transmission reliability and to achieve better error correction performance. RS codes are applied in many systems and adopted by various standards such as storage devices, mobile communications, high-speed modems, DVB T, DVB S, DVB DSNG, DVB C, IEEE 802.16, OTN G.709, etc. In this paper, design and FPGA implementation of RS (204, 188) encoder and decoder is presented for DVB application. This paper proposed a performance analysis and efficient design methodology for serial concatenation coding for DVB system and its implementation on the Virtex 4 xc4vlx15-12-sf363 FPGA chip. The area occupied and speeds at which the proposed design can run are two performance metrics used for performance analysis.

INTRODUCTION

In recent years, the tremendous growth in mobile and multimedia communications has produced a corresponding increase of demand and efforts in the development of highly efficient data transmission codes. The received data is very much error prone in wireless channel, which require them to be protected prior transmission. One of the popular techniques used is Forward Error Correction (FEC) scheme that employs a certain error correction codes [1]. Therefore, Error Control Coding (ECC) is done to prevent the output of erroneous bits despite noise and other imperfections in the channel in which extra bits are added to the data at the transmitter (redundancy) to permit error detection or correction at the receiver.

Error detection and retransmission and Forward Error Correction (FEC) are two techniques to correct the transmission errors. Error detection in a block of data can then request a retransmission, known as Automatic Repeat Request (ARQ) for sensitive data. It is appropriate for Low delay channels and Channels with a return path and not appropriate for delay sensitive data, e.g. real time speech and data. Forward Error Correction (FEC) coding is designed so that errors can be corrected at the receiver. This is appropriate for delay sensitive and oneway transmission (e.g., broadcast TV) of data. Block codes and Convolution Codes are two types of FEC Codes. Reed-Solomon (RS) codes are popular FEC scheme discovered and described in a paper by Reed and Solomon in 1960 [2]. RS codes are very effective in correcting random symbol errors and random burst errors. RS Codes are Reed-Solomon codes are block-based error correcting codes and applied in wide range of systems including storage devices such as, Compact disc DVD, wireless and mobile Communications e.g. microwave links, cellular telephones, Digital satellite Communications and Digital television/Digital Video broadcasting (DVB) [3] and high-speed modems, power line Communication and High speed modem such as ADSL etc.

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The encoder attaches parity symbols to the data before transmission using a predetermined algorithm before transmission. At the receiving side, the decoder detects and corrects a limited predetermined number of errors occurred during transmission. Transmitting the extra parity symbols requires extra bandwidth compared to transmitting the original data but transmitting additional symbols introduced by FEC is better than retransmitting the whole package when at least an error has been detected by the receiver. Implementing Reed- Solomon codec on reconfigurable devices is becoming more attractive because FPGAs provide flexibility where the algorithm parameters can be altered to provide different error correction capabilities. Also they provide a rapid development cycle, resulting in a short time to market.

DIGITAL VIDEO BROADCASTING

The *Digital Video Broadcasting (DVB)* Project is an alliance and industry-led consortium of over 260 broadcasters, manufacturers, network operators; Regulatory bodies committed to designing technical specifications for the global delivery of digital television and data services [4]. DVB has three standards that use identical RS code parameters. These are satellite (DVBS), cable (DVB-C) and terrestrial (DVB-T).All DVB standards employ the same (204,188) RS code and operate in GF

(2_8).Therefore, the same Galois Field arithmetic units and hardware can be used for different DVB standards. Table I summarize RS parameters for DVB standard.

Table I : RS Code Specification for DVB Standard

Code specification			
Symbol width (Bits/Symbol)	m	8	
Field Generator polynomial	$P(x)= x^8+x^4+x^3+x^2+1$		
Code Generator polynomial	$g(x)=(x-\alpha^0)(x-\alpha^1)(x-\alpha^2)\ldots\ldots\ldots\ldots(x-\alpha^{15})$		
Symbol per block (code length)	n	204	Range 4:255
Data symbols (message length)	k	188	Range 76:202

REED SOLOMON CODEC

Reed-Solomon Codes Overview

Channel coding systems based on Forward Error Correction (FEC) systems, play a crucial role in today's digital transmission and storage systems. Reed-Solomon (RS) codes are a prominent representative of FEC block codes that allow recovering as many lost packets (erasures) as the number of parity packets transmitted. They were discovered in 1960 by

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Reed and Solomon and can be considered as a special case of a larger class of FEC block codes called BCH (Bose-Chaudhuri-Hochquenghem) codes. RS codes are based and operate on a special area of mathematics known as Galois fields or finite fields. A finite field has the property that arithmetic operations (+, -,× , /, etc) on field elements always have a result in that field. The elements of the Galois field are often referred to as the RS symbols .A RS encoder or decoder needs to carry out these arithmetic operations. All valid codeword are exactly divisible by the generator polynomial which generate RS codeword. The general form of the generator polynomial is given as [1]:

The General form of polynomial is given as :

$$G(x)=(x-\alpha^1)(x-\alpha^{i+1})\ldots\ldots\ldots(x-\alpha^{1+2t}) \qquad [1]$$

Codeword is constructed using [2]

$$C(x)= G(x).\ I(x) \qquad [2]$$

Where G(x) is a generator polynomial, I (x) is the information blocks, C(x) is valid codeword and α is referred as primitive element of the field.

The block length determines which field the code is defined over. In particular, if m is the number of bits employed to represent each symbol, the block length n is equal to 2_m- 1.The most commonly used RS code operates on GF (256) with symbols of eight bits (one byte), such that there is a direct translation between bytes and RS symbols. Systematic Reed Solomon codes are referred to as RS (n, k, 2t) code, where the first k (k < n) symbols are the source symbols which are to be protected, and the remaining (n -k) symbols are the parity (repair) symbols which are calculated based on the source data. k/n is the code rate. Reed-Solomon codes can correct as many lost symbols than the number of parity symbols transmitted if reliable erasure information is provided. On the other hand, when there are too many errors/erasures, the RS decoder will not be able to correct anything, and just provide output as source symbols without error correction. A RS code operating on symbols of eight bits allows code parameters of any k < 255, and any n, with k <n≤255.

Concatenated FEC Codes For Improved Performance

It is known that the concatenated coding scheme using inner code and outer code can achieve good BER performance. In satellite communication systems, the concatenated coding scheme using the convolutional coding with Viterbi decoding for the inner code and the Reed Solomon (RS) code for the outer code is used. In the concatenated coding scheme, the interleaving and de interleaving are required between the inner code and outer code because the burst errors occur in the output of convolutional decoder in the receiver.

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This paper focuses only on forward error correction (FEC) Coder and decoder and its implementation. In this paper, transmission system that we use is composed of serial concatenation of the Reed-Solomon RS (204,188) shortened) code and rate ¾ punctured convolutional code with 64 QAM [5]. Convolutional FEC codes are very popular because of their powerful error correction capability and are especially suited for correcting random errors.

PROPOSED CONCATENATED FEC CODEC DESIGN

Matlab Based Design and Simulation

The proposed FEC codec for DVB standard has been designed and simulated using Matlab 2007a. The proposed design models the transmitter in its 2k mode, as prescribed in the standard, model one possible receiver design and generate error statistics that will help in determining whether the receiver model satisfies the performance requirements. Proposed model includes the major functional blocks as shown in table II. Fig 1 shows the concatenation of convolutional code as inner code and Reed Solomon code as outer codes.

Table II : Major Processes and Functional Blocks in Proposed Model

Outer Coder	(204,188) Shortened RS Encoder
Inner coder	Rate ¾ punctured Convolution code
Outer Interleaver	Convolution Interleaver I=12
Inner Interleaver	DVB Inner Inerleaver
Mapper and Demapper	DVB 64 QAM Mapper and Demapper
Transmitter and Receiver	OFDM Transmitter and Receiver
Channel	AWGN channel

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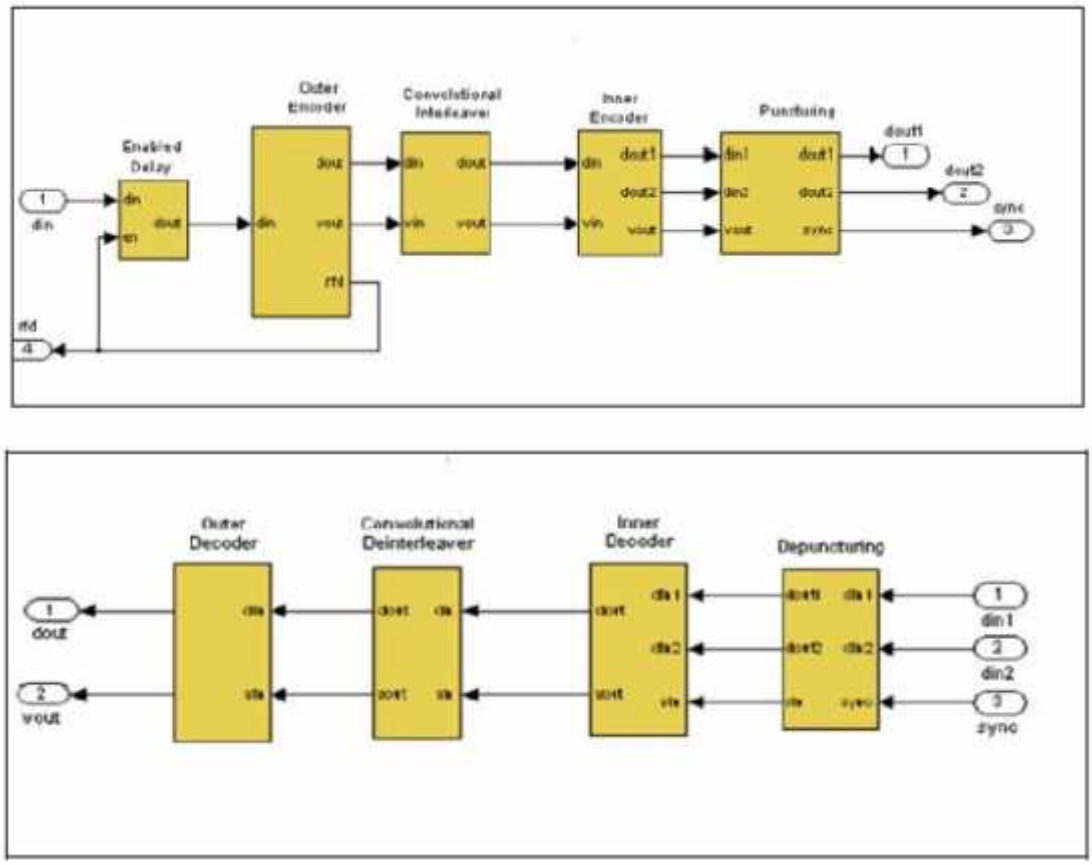

Fig 1 : DVB channel Transmitter and Receiver

Proposed FEC Codec also includes a source of random data, a channel model, error statistic calculators, and several sinks as shown in figure 2. Soft decisions are computed using an A64-QAM demapper that makes soft decisions, producing a set of six real numbers for each complex number in its input. These six numbers represent soft decisions on the real and imaginary components first bit, second bit, and third bit. The Viterbi Decoder subsystem interprets the soft-decision numbers and uses them to decode the punctured convolutional code properly.

In-phase and quadrature phase signal components are extracted after appropriately scaling the received signal, and then they are shifted to obtain soft decisions for various bits. Rectangular QAM Demodulator block can be configured to compute exact bitwise log-likelihood ratios (LLRs). Noise variance needs to be provided and it is computed using the received signal and the signal generated by the DVB 64-QAM Mapper. This technique makes derivation of soft decisions easy for any signal constellation. Block Diagram of Matlab Simulation model of Concatenated DVB channel coding is shown in Fig 2.

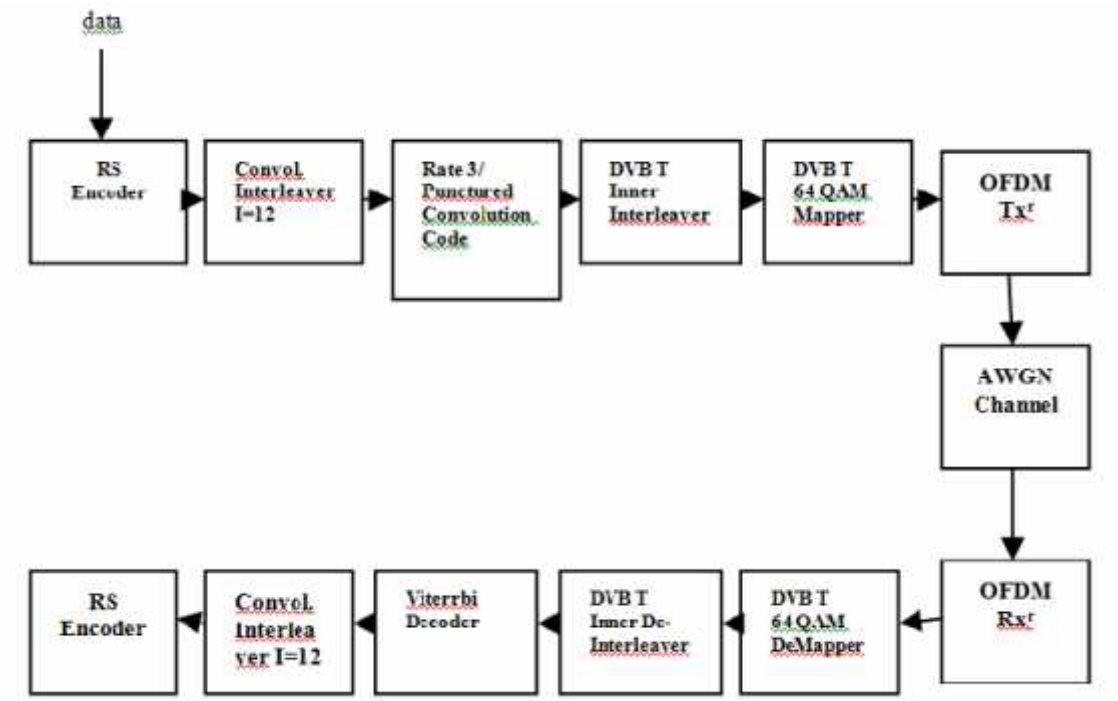

Fig 2 : Block Diagram of Matlab Simulation Model

Reed-Solomon codes (RS codes) are non-binary BCH codes. The error-correcting capability of RS codes is more powerful combined with data interleaving technique. Unscramler is added to front end of decoder and lnterleaver is added to Back- End of encoder. An interleaver can be used to spread the Viterbi output error bursts across multiple R-S codewords for burst error correction. Thus burst error of memory systems are scatter and burst error becomes random error .Based on above designs of codec and Interleaver, error-correcting ability is simulated by Matlab for RS (204,188) code. Simulation waveforms of RS decoding for DVB standard is shown as Fig.3.

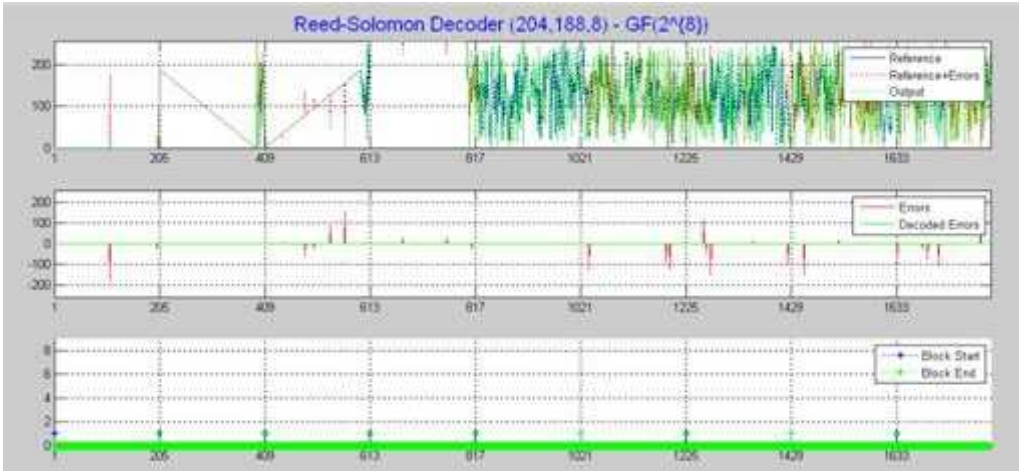

Fig 3 : Simulation Waveform RS (204,188) Decoder

Spectrum scope display that shows the received signal spectrum and Scatter plot display that shows the received signal constellation are given by figure 4 and 5 respectively.

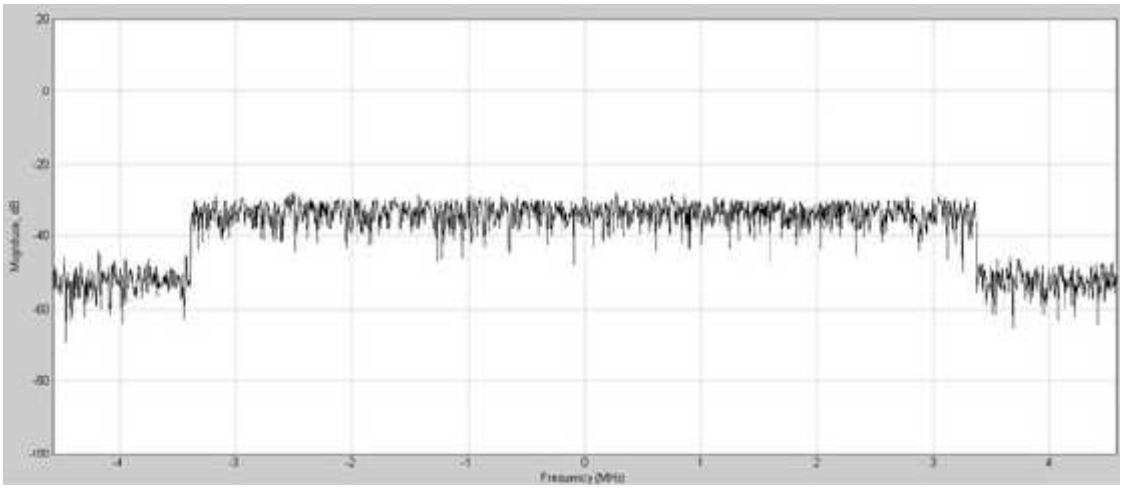

Fig 4 : Received Signal Spectrum Output

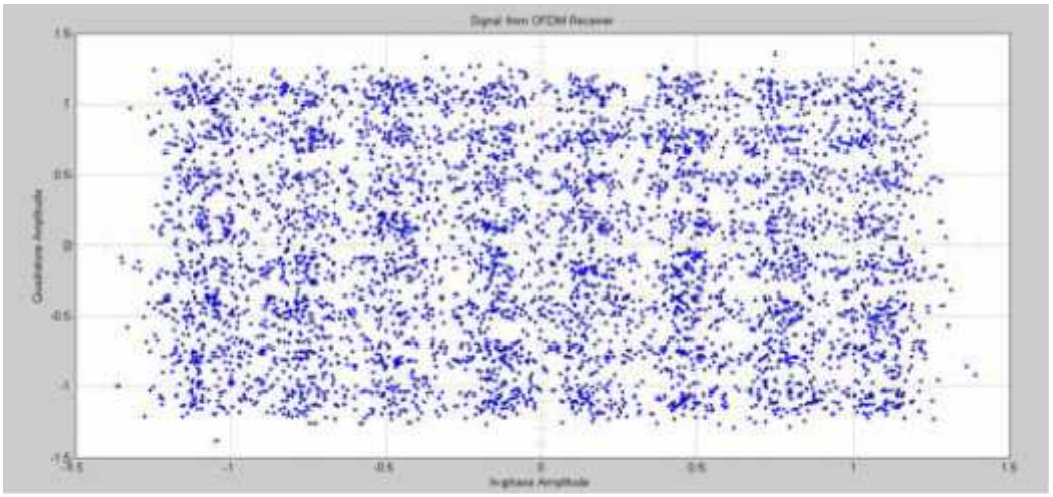

Fig. 5 : Received Signal Constellation Output

FPGA IMPLEMENTATION OF RS CODEC

The Reed-Solomon (255,239) was implemented using VHDL hardware description language, which offers high abstraction level during the implementation. The VHDL description was simulated and implemented in a Xilinx ISE 9.2i Virtex 4 **xc4vlx15-12-sf363** FPGA.

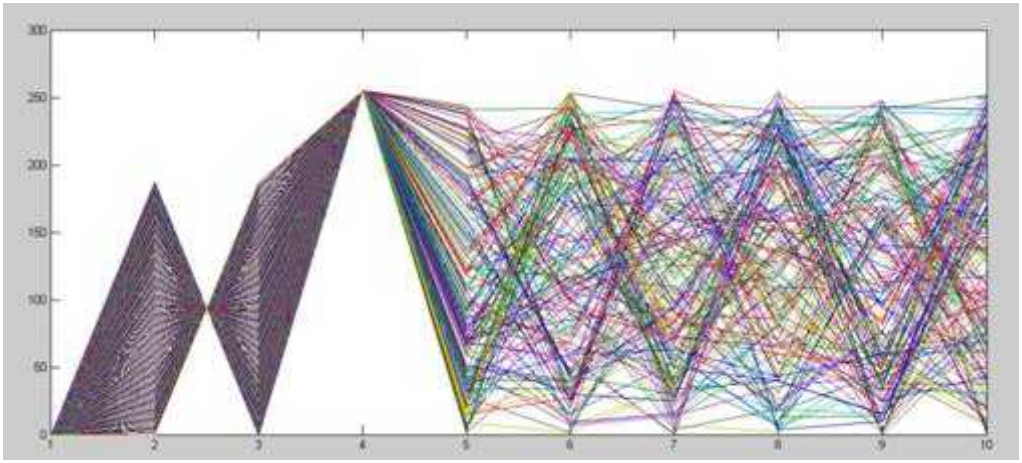

Fig. 6 : Codeword

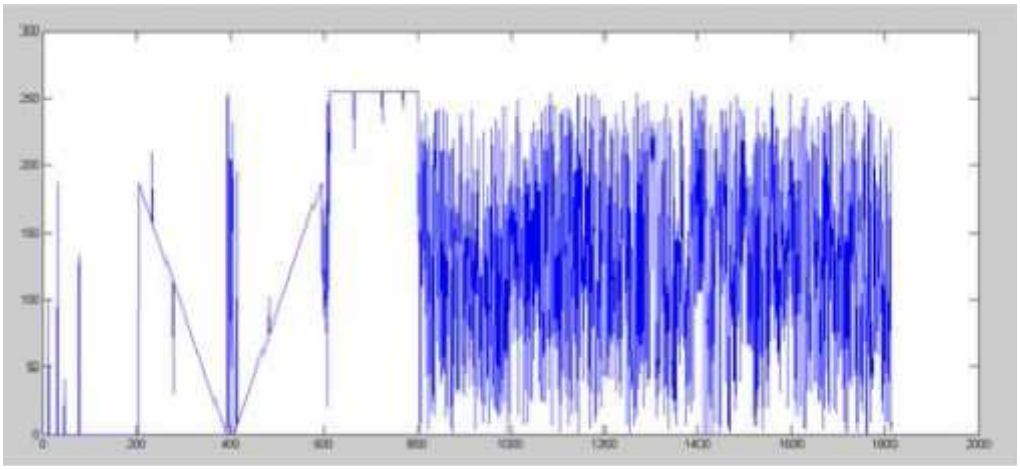

Fig. 7 : RS Coded Data

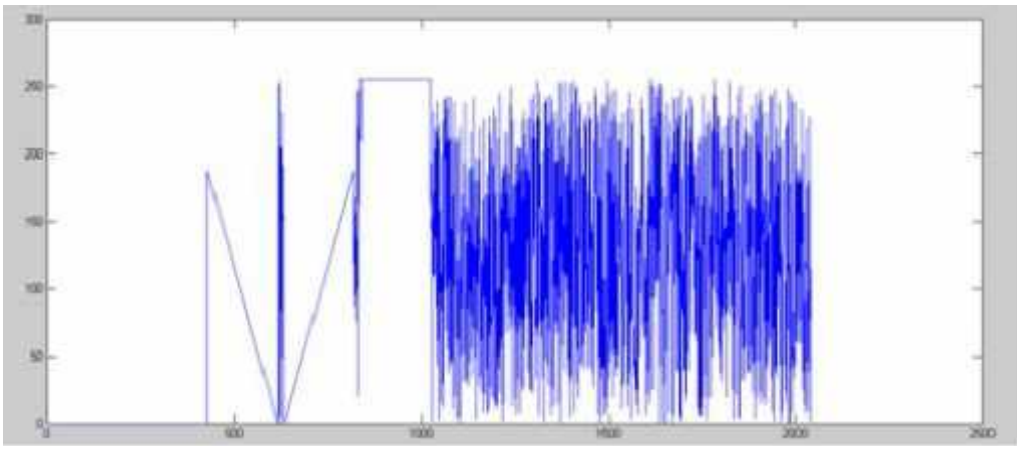

Fig. 8 : Showing All Corrected Errors and Erasures after Decoding

The FPGA Realization of FEC Codec

1. **Encoder :** The data is systematically coded. It is first sent the original data, followed by the parity symbols, which are calculated according to the polynomial generator. It is used a "2t step" polynomial generator, given by expression.

$$g(x) = \prod_{i=b}^{b+2t-1} (x + \alpha^i) \qquad [3]$$

where b is a random number. It must be carefully chosen to avoid increasing the system complexity. The DVB standard takes b as 0. Encoder includes feedback shift register, finite field adders, finite field multipliers, switches. Computing unit is mainly finite field multipliers and finite field adders. Because the domain is characterized by 2, so finite field adders and multipliers are implemented by exclusive-OR logic, and switches are implemented by AND logic.

2 **Decoder :** The decoder is comprised of five blocks: Syndrome Calculator, Key Equation Solver, Error Locator, FIFO and Error Evaluator, as indicated in Figure 9.

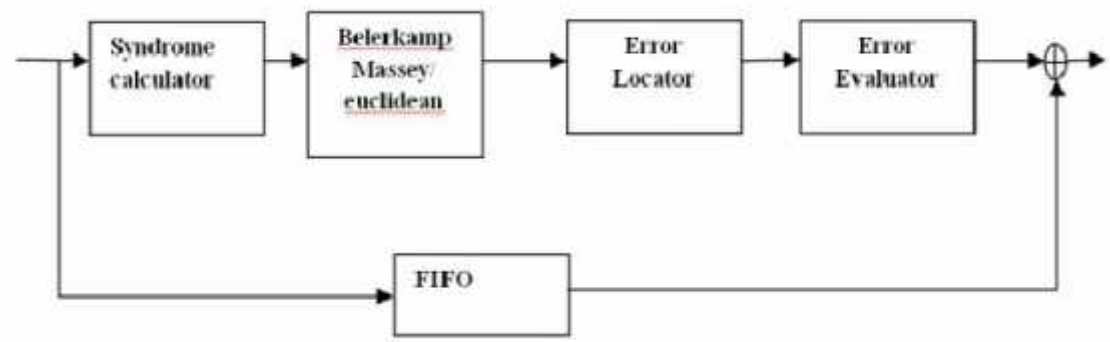

Fig. 9 : Block Diagram of Implemented RS Decoder

The Syndrome Calculator is the first block which monitors the arriving data to evaluate if data correction processing is necessary. It verifies if an error occurred du during the transmission by obtaining all the polynomial roots throughout the data. If the number of errors is smaller than or equal to t, then the syndrome is delivered to the Key Equation Solver block. If the number of errors is larger than t, an error signal is generated to indicate that no correction is possible. Finally, if no errors are found, the data is delivered without any further processing, besides removing the parity symbols.

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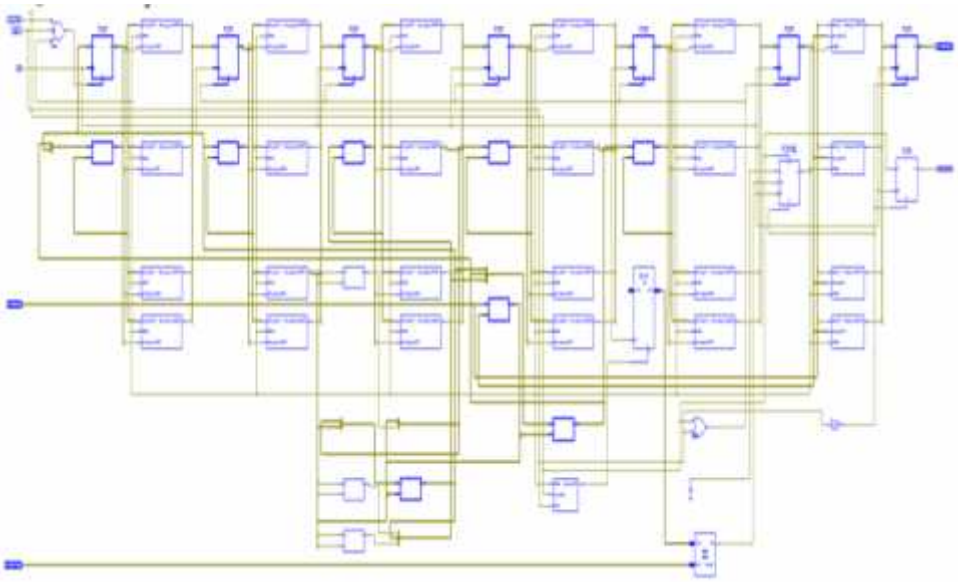
The Euclidian and the Berlekamp-Massey algorithm are two possible algorithm options for the Key Equation Solver. Error Locater finds the error locations using the Chien Search algorithm. The error magnitude to be added to those locations in order to correct the symbol is also determined by this [7].

In this paper, the design has been accomplished RTL description using VHDL and continues with the synthesis using Xilinx Virtex 4 **xc4vlx15-12-sf363** FPGA using ISE Synthesis tool. Both encoder and decoder are synthesized targeting **xc4vlx15-12-sf363** .The synthesis report of the RS Encoder and RS Decoder when using Virtex 4 **xc4vlx15-12-sf363** as target device is summarized in table III .

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	30	12,288	1%	
Number of 4 input LUTs	58	12,288	1%	
Logic Distribution				
Number of occupied Slices	31	6,144	1%	
Number of Slices containing only related logic	31	31	100%	
Number of Slices containing unrelated logic	0	31	0%	
Total Number of 4 input LUTs	58	12,288	1%	
Number of bonded IOBs	16	240	6%	
Number of BUFG/BUFGCTRLs	1	32	3%	
Number used as BUFGs	1			
Number used as BUFGCTRLs	0			
Total equivalent gate count for design	628			
Additional JTAG gate count for IOBs	768			

DEVICE UTILIZATION SUMMARY



RTL VIEW

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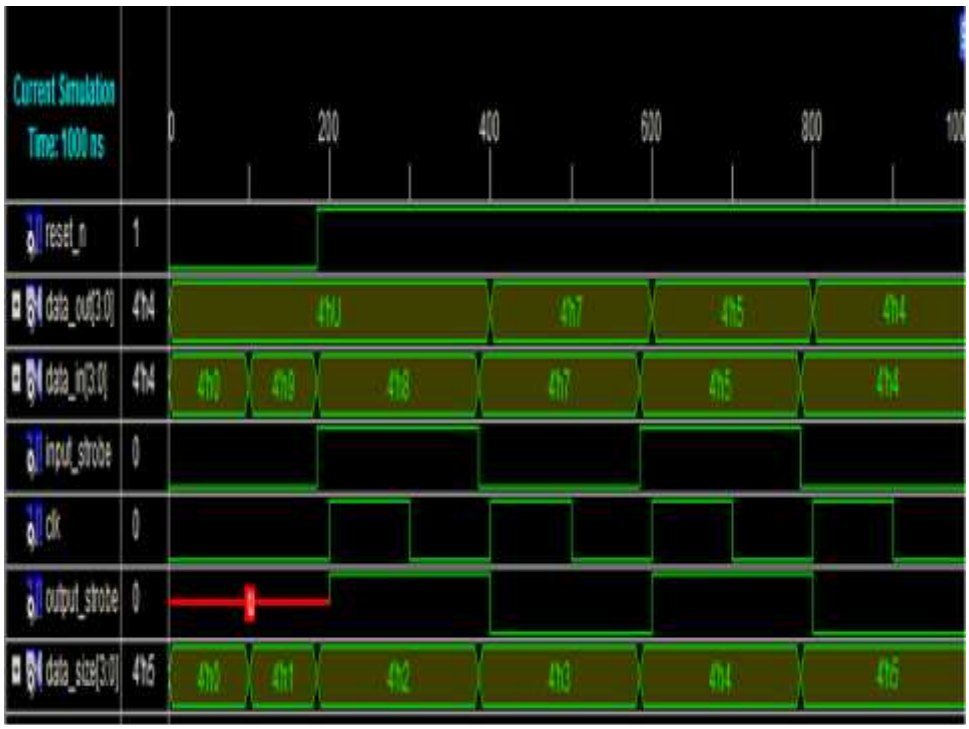

WAVEFORM

Contrast With Other Design

We compare our design with other existing codec solutions[5] for RS Encoder and Decoder as listed in Table III . We can see from this comparison table that the LEs count of our design is the least. That means the RS Codec in this paper has reduced hardware complexity. The design in [5] is a RS codec which used parameterization approach for both DVB and 802.16 networks.

Table III : The Comparison Table of Hardware and Timing Performance of RS Encoder

	RS ENCODER (5)	**PROPOSED RS ENCODER**
Device Utilization Summary		
Number of Slices	95 out of 6144	31 out of 6144
No. of slice flip flops	156 out of 12288	30 out of 12288
No. of 4 input LUTs	168 out of 12288	58 out of 12288
No . of bonded IOBs	16 out of 240	16 out of 240
Timing summary		
Speed grade	-12	-12
Minimum Period	3.676 ns	3.2420 ns
Maximum frequency	272.045 MHz	308.5 MHz

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CONCLUSION

In this paper, Concatenated FEC Codec has been presented to remove error in wireless communication particularly for DVB-T application.The FEC Codec design is done by concatenating RS (Reed Solomon) and Convolution codes. The analysis and simulation is done using Matlab 2007a. We implemented a concatenated coding system based on (204, 188) RS code via a very high-speed hardware description language (VHDL) and synthesized for the FPGA chip Vertex IV xc4vlx15-12-sf363.The result shows that the coder could operate at a max frequency of 308.5 MHz . This design is also suitable for systems such as cable modem and other digital video broadcasting (DVB) standards such as DVB C, DVB S. The proposed Reed Solomon codec has

higher maximum frequency as well as occupies less area of FPGA in comparison to RS Codec proposed in [5] design.

FUTURE SCOPE

Coding field of communication is highly growing area in present era of research. Still, it needs a lot of improvement in the field of error correction and coding techniques. By improving concatenation technique i.e. by concatenation of LDPC (Low Density Parity Check) as inner code and RS (Reed Solomon) as outer coding, we can enhance the performance of FEC system for DVB application. The goal of our present work is to reduce the occupied area of FPGA and increase the efficiency. The development of highly effective decoding algorithms for the implementation is another area where the significant amount of research work can be done and RS code can be made more suitable for different standards for DVB i.e. DVB S2, DVB C, etc.

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