INTERLEAVED SINGLE- STAGE PFC AC-DC CONVERTER FOR ASYNCHRONOUS MOTOR

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***Abstract*--A new interleaved single-stage ac–dc converter is proposed in this paper to reduce line current harmonics while achieving power factor correction (PFC). The proposed rectifier can produce input currents that do not have dead band regions with high PFC, operate with a continuous output current, and minimize the input electromagnetic interference filter size. In this paper, the operation of the new converter is explained, its features and design are discussed in results, and its operation is confirmed with experimental results obtained from a prototype and the performance of asynchronous motor is tested.**

Index Terms—AC–DC power conversion, single-stage power factor correction (PFC), three-level converters, three-phase ,asynchronous motor.

I.INTRODUCTION

Three phase ac-dc power conversion with input power factor correction (PFC) and transformer isolation is typically done using a six-switch front-end ac-dc converter to do the PFC and a four-switch full-bridge converter to do the dc-dc conversion [1]. This approach, however, is expensive and complicated as it needs ten active switches along with associated gate drive and control circuitry. Moreover, the converter must be operated with sophisticated control methods that require the sensing of certain key parameters such as the input current sand voltages; this is particularly true if online pulse width modulation (PWM) techniques are used. POWER factor correction (PFC) is needed in ac–dc power supplies for them to comply with harmonic standards such as IEC 1000-3-2 [1]–[3]. Although it is possible to satisfy these standards by adding passive filter elements to the traditional passive diode rectifier/LC filter input combination, the resulting converter would be very bulky and heavy due to the size of the low-frequency inductors and capacitors. The most common approach to PFC is to use two-stage power conversion schemes. These two-stage schemes use a front-end ac–dc converter stage to perform ac–dc conversion with PFC with the output of the front-end converter fed to a back-end dc–dc converter stage that produces the desired isolated dc output voltage [4].

Using two converter stages in this manner, however, increases the cost, size, and complexity of the overall ac–dc converter, and this has led to the emergence of single-stage power-factor-corrected converters. In order to reduce the cost, size, and complexity associated with two-stage ac–dc power conversion and PFC, researchers have tried to propose single-stage converters that integrate the functions of PFC and isolated dc–dc conversion in a single power converter. Several single-phase [5]–[11] and three-phase [4], [12]-[18] converters have been proposed in the literature, with three-phase converters being preferred over single-phase converters for higher power applications. Previously proposed three-phase single-stage ac–dc converters, however, have at least one of the following drawbacks that have limited their widespread use

1) They are implemented with three separate ac–dc single stage modules [13]–[15].

2) The converter components are exposed to very high dc bus voltages so that switches and bulk capacitors with very high voltage ratings are required [17].

3) The input currents are distorted and contain a significant amount of low-frequency harmonics because the converter has difficulty performing PFC and dc–dc conversion simultaneously [16].

4) The converter must be controlled using very sophisticated techniques and/or nonstandard techniques [5]–[11]. This is particularly true for resonant-type converters that need variable-switching-frequency control methods to operate.

5) The output inductance must be very low, which makes the output current to be discontinuous. This results in a very high output ripple so that secondary diodes with high peak current ratings and large output capacitors to filter the ripple are needed [13]

6) Most of them are in discontinuous conduction mode at the input and need to have a large input filter to filter out large high-frequency harmonics [4], [13]–[15], [17],[18].

The authors proposed a three-phase single-stage three-level converter to mitigate these drawbacks in[18] . Although the converter proposed in that paper was an advance over previously proposed three-phase single-stage converters, it still suffered from the need to have a discontinuous output inductor current at light-load conditions to keep the dc bus capacitor voltage < 450 V, and it needed to operate with discontinuous input current, which resulted in high component current stress and the need for significant input filtering due to the large amount of ripple.

1) This paper presents a new interleaved three-phase single stage rectifier that does not have any of these drawbacks. The work presented in this paper can be considered to be a follow-up work in relation to what was presented in[18] . In comparison to the converter presented in[18]. the converter presented in this paper has an interleaved structure, requires two fewer diodes in the dc bus, has an output current which is continuous for all load ranges, has a dc bus voltage that is less than 450 V for all load conditions, and has a much better input current harmonic content. In this paper, the operation of the new converter is explained, its features and design are discussed in results, and its operation is confirmed with experimental results obtained from a prototype.

II. CONVERTER OPERATION

The proposed converter and its key waveforms are shown in Figs. 1 and 2, respectively. The proposed converter uses auxiliary windings that are taken from the converter transformer to act as “magnetic switches” to cancel the dc bus capacitor voltage so that the voltage that appears across the diode bridge output is zero.

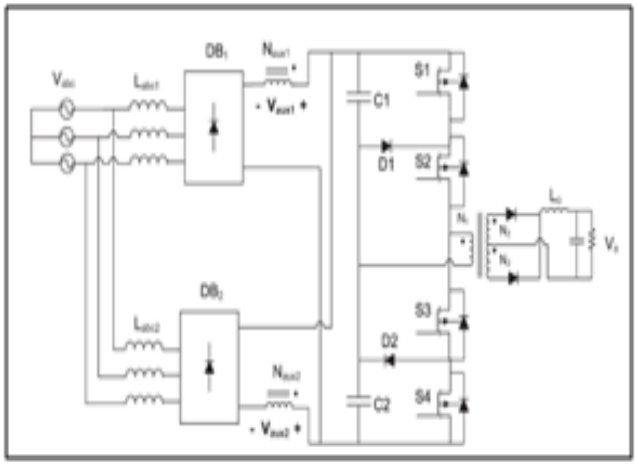


Fig 1: Proposed interleaved three phase three level converter

.When the primary voltage of the main transformer is positive, auxiliary winding 1 (*N*aux1/*N*1 = 2) cancels out the dc bus voltage so that the output voltage of diode bridge 1 (DB1) is zero and the currents in input inductors *La*1, *Lb*1, and *Lc*1 rise. When the primary voltage of the main transformer is negative, auxiliary winding 2 (*N*aux2/*N*1 = 2) cancels out the dc bus voltage so that the output voltage of diode bridge 2 (DB2) is zero and the currents in input inductors *La*2, *Lb*2, and *Lc*2 rise. When there is no voltage across the main transformer primary winding, the total voltage across the dc bus capacitors appears at the output of the diode bridges and the input currents fall since this voltage is greater than the input voltage. If the input currents are discontinuous, the envelope of the input current will be sinusoidal and in phase with the input voltages.

The converter modes of operation are explained in this section. The typical converter waveforms are shown in Fig. 2. The equivalent circuit in each stage is shown in Fig. 3. The converter goes through the following modes of operation.

Mode 1 (*t*0 < *t* < *t*1) [Fig. 3(a)]: During this interval, switches *S*1 and *S*2 are ON. In this mode, the energy from dc bus capacitor *C*1 flows to the output load. Due to magnetic coupling, a voltage appears across auxiliary winding 1 which is equal to the dc bus voltage but has opposite polarity and cancels the total dc bus capacitor voltage; the voltage at the diode bridge output is zero, and the input currents in *La*1, *Lb*1, and *Lc*1 rise.

Mode 2 (*t*1 < *t* < *t*2) [Fig. 3(b)]: In this mode, *S*1 is OFF, and *S*2 remains ON. The energy stored in *L*1(*L*1 = *L*abc1) during the previous mode starts to transfer into the dc bus capacitors. The voltage that appears across auxiliary winding 1 is zero. The primary current of the main transformer circulates through *D*1 and *S*2. With respect to the converter’s output section, the load inductor current freewheels in the secondary of the transformer, which defines a voltage across the load filter inductor equal to −*VL*.

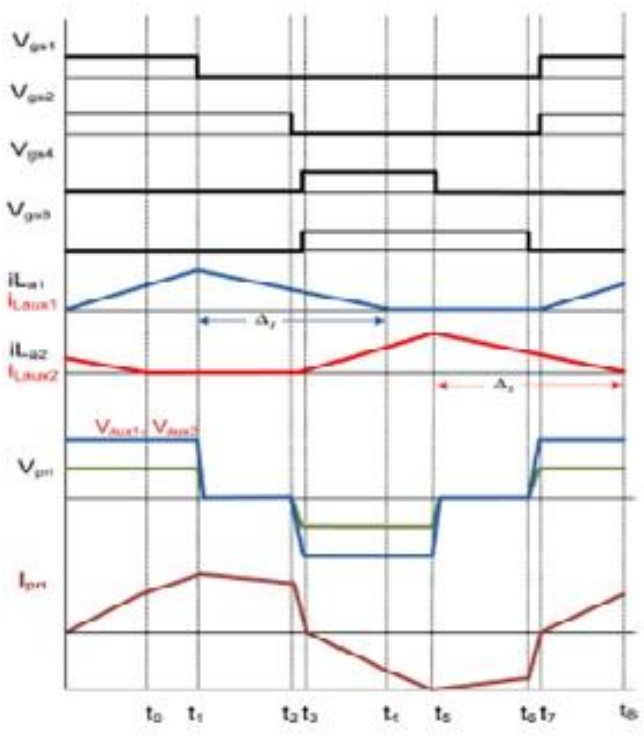
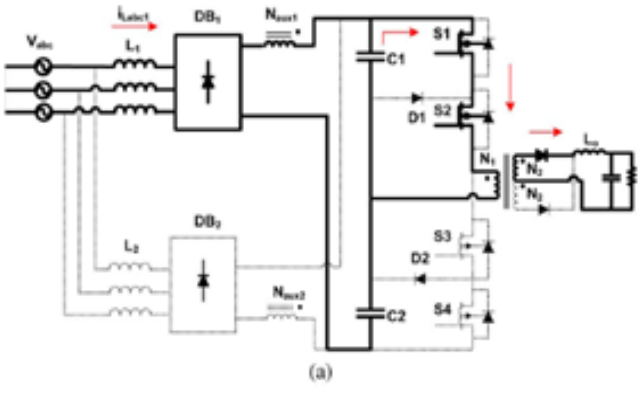


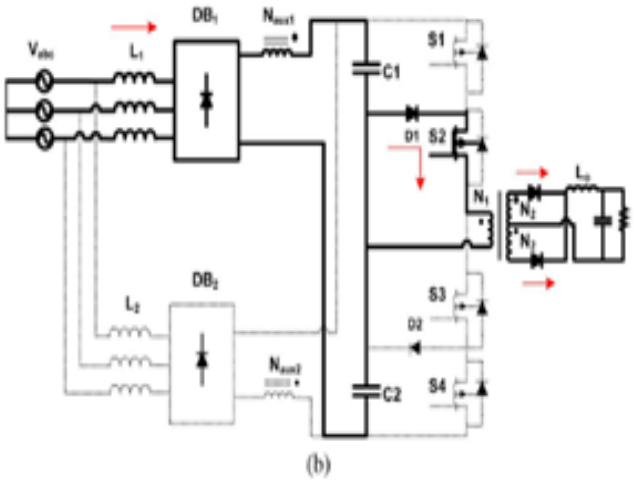
Fig 2: Typical waveforms describing the modes of operation

Mode 3 ($t2 < t < t3$) [Fig. 3(c)]: In this mode, $S1$ and $S2$ are OFF. The energy stored in $L1$ still is transferring into the dc bus capacitor. The primary current of the transformer charges $C2$ through the body diodes of $S3$ and $S4$. Switches $S3$ and $S4$ are switched ON at the end of this mode.

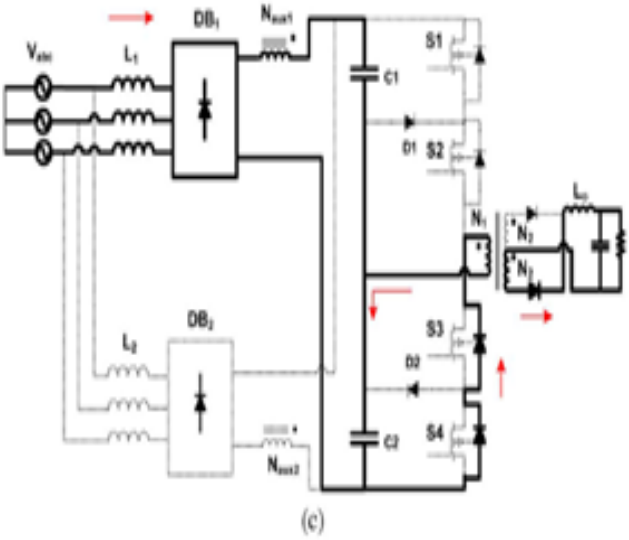
Mode 4 ($t3 < t < t4$) [Fig. 3(d)]: In this mode, $S3$ and $S4$ are ON, and the energy flows from capacitor $C2$ into the load. The voltage appears across auxiliary winding 2 which is equal to the dc bus voltage but acts like a magnetic



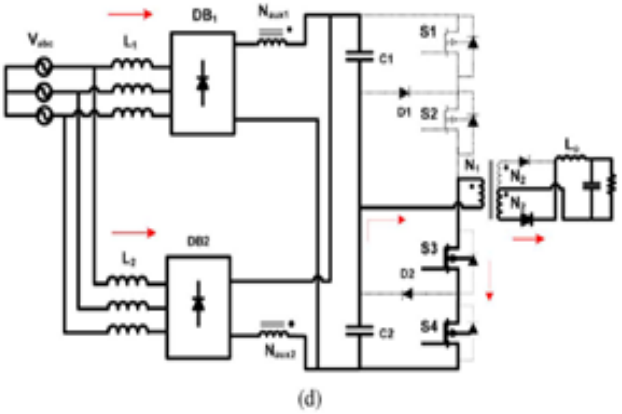
(a) Mode 1 ($t_0 < t < t_1$).



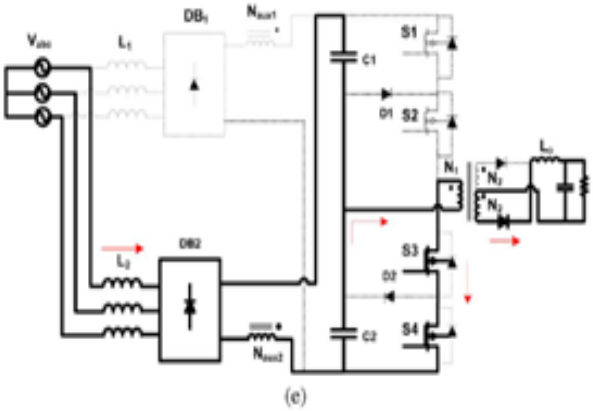
(b) Mode 2 ($t_1 < t < t_2$).



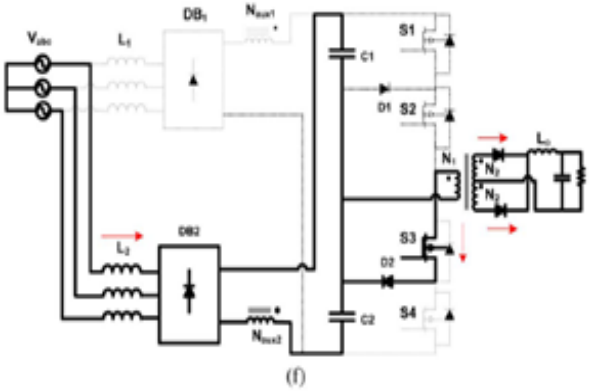
(c) Mode 3 ($t_2 < t < t_3$)



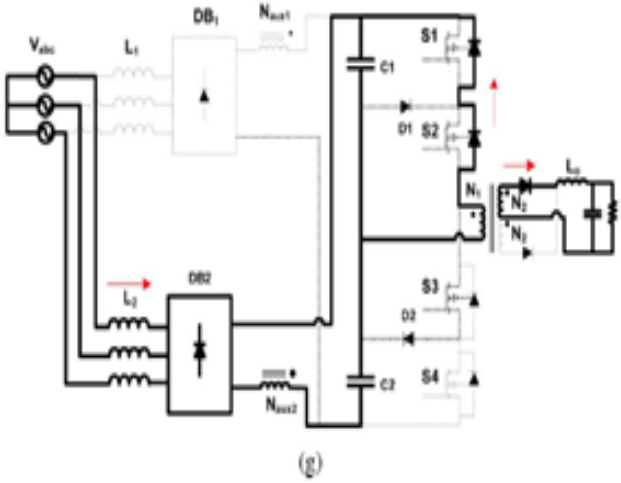
(d) Mode 4 ($t3 < t < t4$)



(e) Mode 5 ($t_4 < t < t_5$).

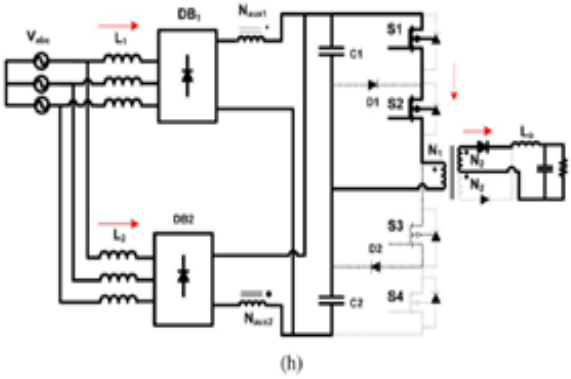


f) Mode 6 ($t_5 < t < t_6$).



(g) Mode 7 ($t_6 < t < t_7$).

(h) Mode 8 ($t_7 < t < t_8$).).



Fig(3)shows modes of operations

switch and cancels out the dc bus voltage. The voltage across the boost inductors *L*2 (*L*2 = *L*abc2) becomes only the rectified supply voltage of each phase, and the current flowing through each inductor increases. This mode ends when the energy stored in *L*1 completely transfers into the dc bus capacitor. For the remainder of the switching cycle, the converter goes through modes 1–4 but with *S*3 and *S*4 ON instead of *S*1 and *S*2 and with DB2 instead of DB1.

Mode 5 (*t*4 < *t* < *t*5) [Fig. 3(e)]: In this mode, *S*3 and *S*4 are ON, and a symmetrical period begins. In this mode, the energy flows from capacitor *C*2 into the load. The voltage

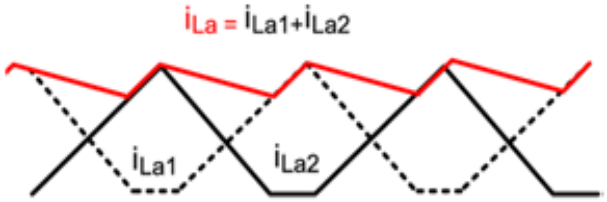


Fig.4. Interleaving between two input inductor currents

across the boost inductors *L*2 becomes only the rectified supply voltage of each phase, and the current flowing through each inductor.

Mode 6 (*t*5 < *t* < *t*6) [Fig. 3(f)]: In this mode, *S*3 is ON and *S*4 is OFF, and the primary current of the main transformer circulates through diode *D*2 and *S*3. The energy stored in the boost inductors *L*2 during the previous mode starts transferring into the dc bus capacitor. The output inductor current also freewheels in the secondary of the transformer during this mode.

Mode 7 (*t*6 < *t* < *t*7) [Fig. 3(g)]: In this mode, *S*3 and *S*4 are OFF, and the primary current of the transformer charges capacitor *C*1 through the body diodes of *S*1 and *S*2. The energy stored in the boost inductors *L*2 transfers into the dc bus capacitor

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Mode 8 ($t7 < t < t8$) [Fig. 3(h)]: In this mode, $S1$ and $S2$ are ON. In this mode, the energy from dc bus capacitor $C1$ flows to the output load. This mode ends when the energy in the inductors $L2$ completely transfers into the dc bus capacitors. Time $t8$ is the end of the switching cycle, and another switching cycle begins with the same modes.

It should be noted that the input current is the summation of inductor currents $iL1$ and $iL2$ which are both discontinuous. However, by selecting appropriate values for $L1$ (= $La1$ = $Lb1$ = $Lc1$) and $L2$ (= $La2$ = $Lb2$ = $Lc2$) in such a way that two inductor currents such as iLa1 and iLa2 have to overlap each other, the input current can be made continuous as shown in Fig. 4, thus reducing the size of the input filter significantly. There is a natural 180◦ phase difference between the currents in $L1$ and the currents in $L2$ as one set of currents rises when the transformer primary is impressed with a positive voltage and the other set rises when the transformer primary is impressed with a negative voltage—these two events occur 180◦ apart during a switching cycle.

III. CONVERTER ANALYSIS AND DESIGN

The analysis and the design of the proposed interleaved converter are almost identical to that presented in [18] and therefore are not presented here. Readers are referred to [18] for details. In this paper, only differences in the analysis and the design are presented. With respect to analysis, steady-state operating points are identified using a computer program such as the one presented in[18] . The only difference between the analysis of the proposed converter and the one in[18] is the analysis and design of the input inductors. In the proposed interleaved converter, there are two sets of inductors ($L1$ and $L2$) at the input side, with each set conducting half the current. The analysis needs to consider the current in both these sets instead of just one.

The values for $L1$ and $L2$ should be low enough to ensure that their currents are fully discontinuous under all operating conditions but not so low as to result in excessively high peak currents. The worst case to be considered is the case when the converter operates with minimum input voltage and maximum load since, if the input current in each set of inductors is discontinuous under these conditions, it will be discontinuous for all other operating conditions, and thus, an excellent power factor will be achieved.

Based on the results of the analysis, graphs of steady-state characteristics, such as the ones shown in Fig. 5, can be drawn and then used as part of a design procedurein [18] . Although the design procedures of the two converters are the same, what should be noted when comparing graphs of steady-state characteristics for the two converters is that it is much easier to design the converter in such a way that the dc bus voltage is not excessive (< 800 V). It is the fact that the dc bus voltage is not excessive that allows for greater flexibility in the design of the converter such as a greater output inductor, which results in less output current ripple.

IV. THREE PHASE ASYNCHRONOUS MOTOR

An electrical motor is such an electromechanical device which converts electrical energy into a mechanical energy. In case of three phase AC operation, most widely used motor is Three phase induction motor as this type of motor does not require any starting device or we can say they are self starting induction motor. For better understanding the principle of three phase induction motor**,** the basic constructional feature of this motor must be known to us. This Motor consists of two major parts:

Stator: Stator of three phase induction motor is made up of numbers of slots to construct a 3 phase winding circuit which is connected to 3 phase AC source. The three phase winding are arranged in such a manner in the slots that they produce a rotating magnetic field after AC is given to them.

Rotor: Rotor of three phase induction motor consists of cylindrical laminated core with parallel slots that can carry conductors. Conductors are heavy copper or aluminum bars which fits in each slots & they are short circuited by the end rings. The slots are not exactly made parallel to the axis of the shaft but are slotted a little skewed because this arrangement reduces magnetic humming noise & can avoid stalling of motor.

Working principle: Here the relative velocity between the rotating flux and static rotor conductor is the cause of electric current generation; hence as per Lenz's law the rotor will rotate in the same direction to reduce the cause i.e. the relative velocity. Thus from the working principle of three phase induction motor it may observed that the rotor speed should not reach the synchronous speed produced by the stator. If the speeds equals, there would be no such relative velocity, so no emf induction in the rotor, & no electric current would be flowing, and therefore no torque would be generated. Consequently the rotor can not reach at the synchronous speed. The difference between the stator (synchronous speed) and rotor speeds is called the slip. The rotation of the magnetic field in an induction motor has the advantage that no electrical connections need to be made to the rotor.

Thus the **three** phase induction motor **is:**

• Self-starting.

• Less armature reaction and brush sparking because of the absence of commutators and brushes that may cause sparks.

• Robust in construction.

• Economical.

• Easier to maintain.

V. EXPERIMENTAL RESULTS AND CONVERTER COMPARISON

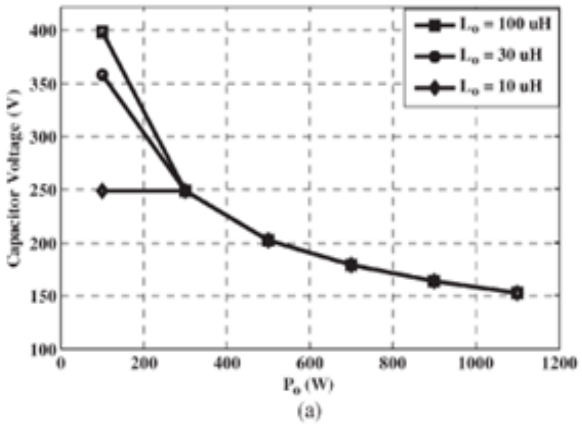
An experimental prototype of the proposed converter was built to confirm its feasibility. The prototype was designed according to the following specifications:

Input voltage *V*in = 208 ± 10% Vrms (line−line)
Output voltage *Vo* = 48 V
Output power *Po* = 1.1 kW
Switching frequency *f*sw = 100 kHz.

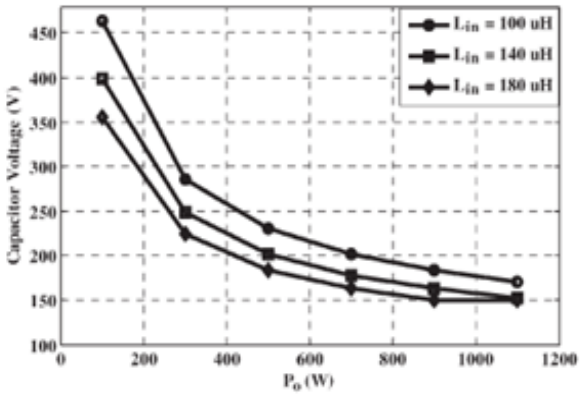
The typical converter waveforms are shown in Fig. 6. It can be seen that the proposed converter can operate with nearly sinusoidal input currents with no dead band regions. It is a multilevel full-bridge converter that the switch stresses are half the dc bus voltage; it also can operate with a continuous output current, unlike most other converters of the same type.

The experimental results obtained for the proposed converter are compared to those of the converter proposed in [18], as shown in Tables I and II. The converter in [18] is a single-stage three-level PFC converter and is a non interleaved version of the proposed converter with just one set of input inductors instead of two. The output inductor current in[18] was designed to be continuous for heavy loads and discontinuous for light loads to keep the dc bus voltage less than 450 V.

Compared to the non interleaved converter that was presented in [18], the interleaved converter that is proposed in this paper has several advantages in addition to reduced input current ripple. The proposed converter can operate with a continuous current at the output from 10% of the full load to full load, which makes the output current have less ripple. This is because the proposed converter has an interleaved structure that results in a change of the energy equilibrium at the dc bus (the net equivalent inductance at the input is larger in the proposed converter), which makes the dc bus small enough to permit the output inductor to be sufficiently large.
A larger output inductor means that there is considerably less ripple in the output inductor current of the interleaved converter than there is in the non interleaved converter proposed in[18]



(a)



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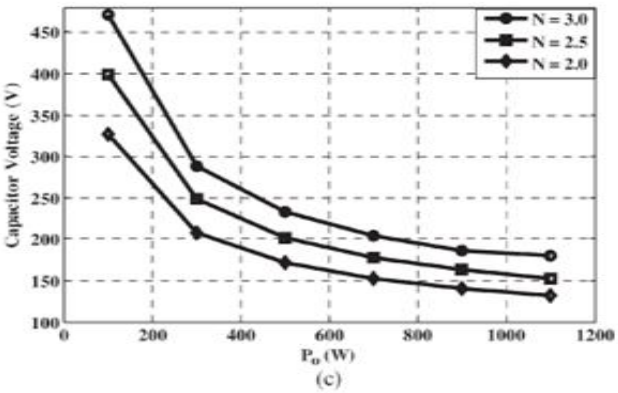

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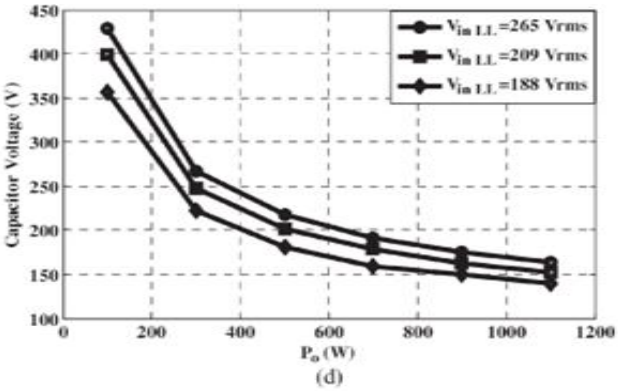
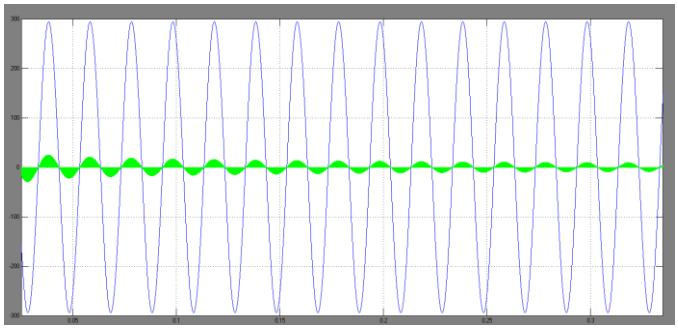


(d)



V : 100 V/div; *t*: 4 μs/div). (b) Primary voltage of the main transformer (*V* : 100 V/div; *t*: 4 μs/div). (c) Input current and voltage (*V* : 100 V/div; *I*: 4 A/div). (d) Output inductor current (*I*: 10 A/div; *t*: 4 μs/div).

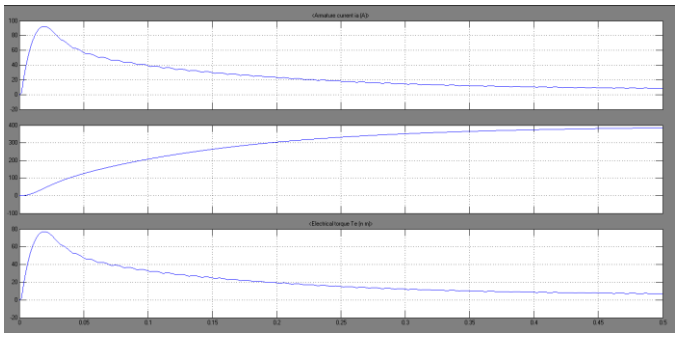


Fig 6. Experimental results. (a) Top switch voltages *V*ds1 and *V*ds2

V : 100 V/div; *t*: 4 μs/div). (b) Primary voltage of the main transformer (*V* : 100 V/div; *t*: 4 μs/div). (c) Input current and voltage (*V* : 100 V/div; *I*: 4 A/div). (d) Output inductor current (*I*: 10 A/div; *t*: 4 μs/div).

This helps reduce secondary component stresses and filtering. It should be noted that the converter has been implemented with an output inductor that is larger than necessary to show that the proposed converter can operate with a continuous output current and a primary-side dc bus voltage that is not excessive. It should also be noted that no additional input filtering was used for the proposed interleaved converter, and the input current waveform shown in Fig. 6(c) is just the summation of an input phase current of diode bridge 1 and the corresponding phase current of diode bridge 2. Fig. 7 shows the efficiency of the proposed converter at various output power levels. It should be noted that the proposed converter has a higher efficiency than the converter proposed in [18] . This is because it does not have any diode in the dc link, whereas the converter proposed in [18] must have. It is also due to the fact that the switch voltage turn-on losses have been

TABLE I
COMPARISON OF ELEMENTS FOR THE NONINTERLEAVED AND INTERLEAVED CONVERTERS

Components	Converters	
	Non-interleaved three-level PFC converter	**Interleaved** three-level PFC converter
S_1-S_4	4 * FDL100N50F - 500V	
Clamp diodes	2 * MUR 860	
Rectifire diodes	DSSK60-02A	
Auxiliary rectifire diodes	DSI45-16A	-
Diode bridge	2 * SC50VB80-G	SC50VB80-G
Bus Capaciotrs	2 * 2200 uF	
Input boost indutor	80 µH	2 * 140 µH
Input filter inductor	3 * 20 µH	-
Input filter capacitor	3 * 1 µF	-
Output filter inductor	15 µH	100 µH
Output filter capacitor	450µF	450µF
Transformer turns ratio	25:10:10	25:10:10

TABLE II
COMPARISON OF FEATURES FOR THE NONINTERLEAVED AND INTERLEAVED CONVERTERS

Parameters	Converters	
	Non-interleaved three-level PFC converter	**Interleaved** three-level PFC converter
ΔV_o(pk-pk)	1.2 V	0.06 V
ΔI_o(pk-pk)	7.5 A	0.8 A
D_{max}	0.61	0.77
$V_{bus,max}$	533	302
THD of input current	2.9 %	0.8 %

reduced considerably as there is much less voltage across the switch; it is because the proposed converter has much less dc bus voltage in comparison to that in[18] (Table II). Figs. 8 and 9 show the input current harmonics at *Po* = 1.1 kW and *Po* = 550Wand *V*in = 220 Vrms (line–line). It can be seen that the converter's harmonics are below the harmonic levels that are specified by the IEC 1000-3-2 standard.

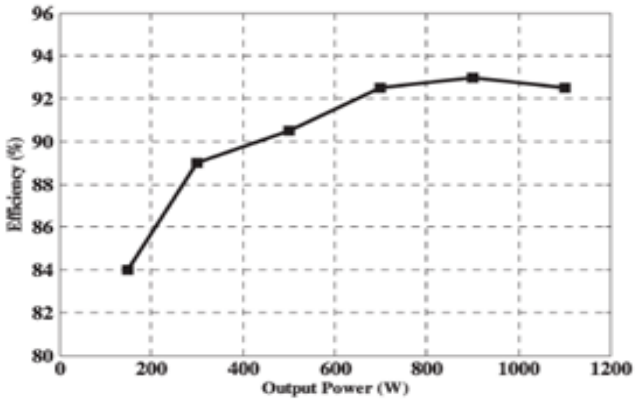


Fig 7: Efficiency of the proposed converter at various power levels

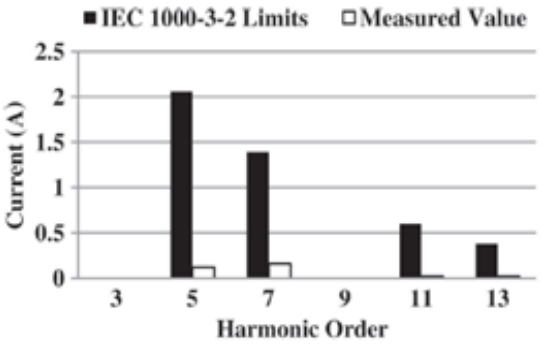


Fig 8: Input current harmonic at Vin = 220 Vrms (line-line) and Po = 1.1 KW compared to the IEC standard

VI. CONCLUSION

A new three-phase three-level single-stage power-factor corrected ac–dc converter with interleaved input has been proposed in this paper. The converter operates with a single controller to regulate the output voltage and uses auxiliary windings taken from its power transformer as magnetic switches to cancel the dc bus voltage so that the input section operates like a boost converter.

The proposed converter has the following features.

1) The proposed converter can operate with lower peak voltage stresses across its switches and the dc bus capacitors as it is a three-level converter. This allows for greater flexibility in the design of the converter and ultimately improved performance.

2) The proposed converter can operate with an input current harmonic content that meets the EN61000-3-2 Class A standard with reduced input filter due to the interleaved structure.

3) The output inductor of the proposed converter can be designed to work in continuous conduction mode over a wide range of load variation and input voltage. This results in a lower output inductor current ripple than that found in previously proposed converters which helps reduce secondary component stresses and filtering.

4) The aforementioned features are all an improvement on the original non interleaved converter that was presented in [18] . Moreover, the proposed interleaved converter operates with greater efficiency than the converter proposed in[18] because it has fewer diodes in the dc bus and it has
less turn-on losses.

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