Power Quality Improvement by using UPQC Topology with Reduced DC-link Voltage Rating

K.RAJKUMAR
M. Tech Student Scholar
Department of EEE,
S.R Engineering College,
Warangal, T.S, India

T. Ashok Kumar
Assistant Professor
Department of EEE,
S.R Engineering College,
Warangal, T.S, India

LOKESH N
Assistant Professor
Department of EEE,
S.R Engineering College,
Warangal, T.S, India

ABSTRACT

The main aim of this paper is to improve, the power quality in the Facility side i.e. in Distribution side by the help of the Unified Power Quality Conditioner. The UPQC is a customer power device, which is used to mitigate the power quality problems. By the help of the UPQC, the various power quality concerns such as voltage sag, swell, harmonics can be eliminated. In our paper the modified, three phase four wire distribution is used to control the reactive power in the line. And also it uses, the both voltage source inverter which are connected in back to back manner with the help of reduced d. c. link capacitor.

Keywords-Power Quality, switching frequency, dc-link voltage, unified power quality conditioner (UPQC)

I.INTRODUCTION

The use of sophisticated equipment/loads at transmission and distribution level has increased considerably in recent years due to the development in the semiconductor device technology. The equipment needs clean power in order to function properly. At the same time, the switching operation of these devices generates current harmonics resulting in a polluted distribution system. The power-electronics-based devices have been used to overcome the major power quality problems [1]. To provide a balance, distortion-free, and constant magnitude power to sensitive load and, at the same time, to restrict the harmonic, unbalance, and reactive power demanded by the load and hence to make the overall power distribution system more healthy, the unified power quality conditioner-(UPQC) is one of the best solutions [2] [3].

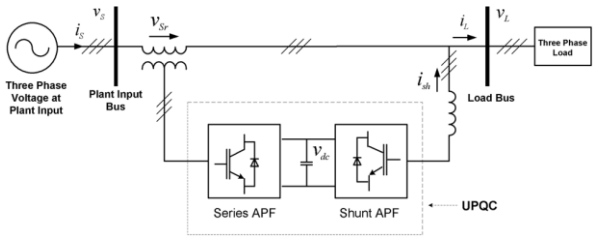

Fig.1. Shows Basic UPQC system configuration

A unified power quality conditioner (UPQC)[4], [5], [6]–[7], is another mitigating device that is similar in construction to a unified power flow controller (UPFC) [8]. A UPFC is employed in power transmission system where as a UPQC is employed in a power distribution system, to perform the shunt and series compensation simultaneously. But a UPFC only needs to provide balance shunt and/or series compensation, since a power transmission system generally operates with balanced, distortion free environment. The primary objective of a UPFC is to control the flow of power at fundamental frequency only. On the other hand, a power distribution system may contain dc components, distortion, and unbalance. Therefore, a UPQC must operate under these environments while performing shunt and/or series compensation. The basic configuration of UPQC-based system is shown in Fig. 1. It

consists of two voltage source inverters (VSIs) connected back to back, sharing a common dc link in between. One inverter acts as a shunt APF, whereas the other as a series APF. The load-reactive power compensation in most of the UPQC based power quality compensation application is done by shunt APF, whereas, the series APF is generally utilized to compensate voltage related problems [4], [5], [6]–[7]. In a typical distribution system the voltage sag and/or swell, flicker, un-balance, etc. are short duration power quality problems. On the other hand current harmonics, load-reactive power demand etc. are load dependant issues and constant for a particular type of load. Therefore the utilization factor of shunt APF is much higher than that of series APF during normal steady-state operation .Also, the rating of shunt APF is significantly affected by the reactive power needs [9].Three-phase four-wire system, neutral-clamped topology is used for UPQC [10], [11]. This topology enables the independent control of each leg of both the shunt and series inverters, but it requires capacitor voltage balancing [12]. In [13], four-leg VSI topology for shunt active filter has been proposed for three-phase four-wire system. This topology avoids the voltage balancing of the capacitor, but the independent control of the inverter legs is not possible. To overcome the problems associated with the four-leg topology, in [14], [15], the authors proposed a T-connected transformer and three-phase VSC based DSTATCOM. However, this topology increases the cost and bulkiness of the UPQC because of the presence of extra transformer. UPQC topology with reduced dc-link voltage is proposed. The topology consists of capacitor in series with the interfacing inductor of the shunt active filter. The series capacitor enables reduction in dc-link voltage requirement of the shunt active filter and simultaneously compensating the reactive power required by the load, so as to maintain unity power factor, without compromising its performance.

II.CONVENTIONAL UPQC TOPOLOGY

The Conventional UPQC Topology is Back -Back connected device. It deals with both load current and supply voltage imperfections. UPQC can simultaneously act as shunt and series active power filters. The series part of the UPQC is known as dynamic voltage restorer (DVR). It is used to maintain balanced, distortion free nominal voltage at the load. The shunt part of the UPQC is known as distribution static compensator (DSTATCOM), and it is used to compensate load reactive power, harmonics and balance the load currents thereby making the source current balanced and distortion free with unity power factor. It consisting of two dc-link capacitors V_{dbus}=2*V_{dc}

where

V_{dc}=520V (Conventional)

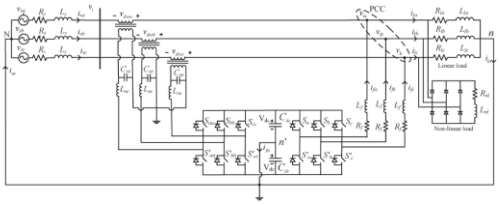

Fig.2.Shows Equivalent circuit of Conventional VSI Topology based UPQC

The conventional topology of the UPQC is discussed in detail. Fig. 2 shows the power circuit this section, of the neutral-clamped VSI topology-based UPQC which is considered as the conventional topology in this study. Even though this topology requires two dc storage devices, each leg of the VSI can be controlled independently, and tracking is smooth with less number of switches when compared to other VSI topologies [16]. In this figure shows $V_{sa,}$ $V_{sb,}$ $V_{sc,}$are source voltages of phases a, b and c respectively. Similarly, V_{ta},$V_{tb}$and $\boldsymbol{V_{tc}}$ are terminal voltages. The voltages V_{dvra}, V_{dvrb}, and V_{dvrc} are injected by the series active filter. The three phase source currents are represented by i_{sa}, i_{sb}, and i_{sc}, load currents are represented by $i_{la,}$ i_{lb} and i_{lc}. The shunt active filter currents are denoted by $i_{fa,}$$i_{fb}$,$i_{fc}$ and i_{ln} represents the current in the neutral leg. L_s and R_s represent the feeder inductance and resistance, respectively. The interfacing inductance and resistance of the shunt active filter are represented by L_f and R_f respectively, and the interfacing inductance and filter capacitor of the series active filter are represented by L_{se} and C_{se}, respectively. The load constituted of both linear and nonlinear loads as shown in this figure. The dc-link capacitors and voltages across them are represented by $C_{dc1} = C_{dc2} = C_{dc}$ and $V_{dc1} = V_{dc2} = V_{dc}$, respectively, and the total dc-link voltage is represented by V_{dbus}(V_{dc1}+ $V_{dc2} = 2V_{dc}$). In this conventional topology, the voltage across each common dc-link

capacitor is chosen as 1.6 times the peak value of the source voltages as given in [16].

III. PROPOSED UPQC TOPOLOGY

The Proposed UPQC Topology is Back-Back to device. It deals with both load current and supply voltage imperfections. UPQC can simultaneously act as shunt and series active power filters. The series part of the UPQC is known as dynamic voltage restorer(DVR). It is used to maintain balanced, distortion free nominal voltage at the load. The shunt part of the UPQC is known as distribution static compensator (DSTATCOM), and it is used to compensate load reactive power, harmonics and balance the load currents thereby making the source current balanced and distortion free with unity power factor. It consisting of single dc-link capacitor V_{dbus} =750V (Proposed).

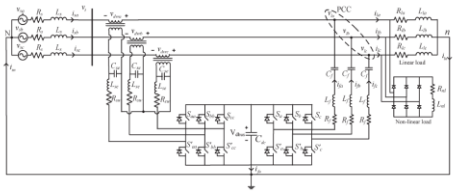

Fig.3.Shows Equivalent Circuit of modified VSI Topology for UPQC Compensation system

The equivalent circuit of the proposed VSI topology for UPQC compensated system. In this topology, the system neutral has been connected to the negative terminal of the dc bus along with the capacitor C_f in series with the-interfacing inductance of the shunt active filter. This topology is referred to as modified topology. The passive capacitor C_f has the capability to supply a part of the reactive power required by the load, and the active filter will compensate the balance reactive power and the harmonics present in the load. The addition of capacitor in series with the interfacing inductor of the shunt active filter will significantly reduce the dc-link voltage requirement and consequently reduces the average switching frequency of the switches. This concept will be illustrated with analytic description in the following section. The reduction in the dc-link voltage requirement of the shunt active filter enables us to the match the dc-link voltage requirement with the series active filter. This topology avoids the over rating of the series active filter of the UPQC compensation system. The design of the series capacitor C_f and the other VSI parameters have significant effect on the performance of the compensator.

IV.DESIGN OF UPQC TOPOLOGY PARAMETERS

The important parameters that need to be taken into consideration while designing conventional VSI are V_{dc}, C_{dc}, L_f , L_{se}, C_{se}, and switching frequency (f_{SW}). The design details of the VSI parameters for the shunt and series active filter are given in [17], [18].

A .Design of Shunt Active filter parameters:

Consider the active filter is connected to an X_{KVA} system and deals with $0.5X_{KVA}$ and $2X_{KVA}$ handling capability under transient conditions for n cycles. During transient, with an increase in system KVA load, the voltage across each dc-link capacitor (V_{dc}) decreases and vice versa. Allowing a maximum of 25% variation in V_{dc} during transient, the differential energy (ΔE_c) across C_{dc} is given by

$$\Delta E_C = \frac{C_{dc}[(1.125V_{dc})^2-(0.875V_{dc})^2]}{2} \quad (1)$$

The change in system energy (ΔE_S) for a load change from 2X KVA to 0.5X KVA is

$$\Delta E_{s=}\left(2X-\frac{X}{2}\right)nT \quad (2)$$

Equating (1) and (2), the dc-link capacitor value is given by

$$C_{dc} = \frac{2\left(2X-\frac{X}{2}\right)nT}{(1.125V_{dc})^2-(0.875V_{dc})^2} \quad (3)$$

where, V_m is the peak value of the source voltage, X is the KVA rating of the system, n is number of cycles, and T time period of each cycle. An empirical study has been carried out for various values of interfacing inductance values with the variation of the dc-link voltage in [17], with V_{dc} = mV_m

Where $m = \frac{1}{\sqrt{1-f_{swmin}/f_{swmax}}}$ (4)

It is found that m = 1.6 gives fairly good switching performance of the VSI. The approximate relationship between *m* and minimum (f_{swmin}), maximum switching frequency (f_{smax}) is obtained by-analysis of the VSI in [17], and this is given below. For switching frequency variation approximately from 6 kHz to 10 kHz, the value of m is 1.58, which is taken as 1.6 in the study. Based on this, the shunt interfacing inductance has been derived taking into consideration of the maximum switching frequency and is given below [17].

$$L_f = \frac{mV_m}{4h_1 f_{swmax}} \qquad (5)$$

where

$$h_1 = \sqrt{\frac{K1(2m^{2-1})f_{swmax}}{K_2 4m^2}} \qquad (6)$$

where h1 is the hysteresis band limit. k1and k2 are proportionality constants

B. Design of Series Active Filter parameters:

The series active filter system a first-order system, a resistor is added in series with the filter capacitor, referred as switching band resistor (R_{sw}) [18]. The rms value of the capacitor current can be expressed as

$$I_{se} = \sqrt{I^2{}_{inv} - I_l{}^2}$$

I_{inv} is the series inverter current rating and *Il* is the load current. The capacitor -branch current is divided into two components—a fundamental current *I*se1, corresponding are given to the fundamental reference voltage (*V*ref1) and a switching frequency current I_{sw}, corresponding to the band voltage (V_{sw}). The DVR voltage and the current of the capacitor are given by

$$V_{dvr} = \sqrt{{V_{ref_1}}^2 + {I_l}^2}$$

$$I_{sc} = \sqrt{{I_{se}}^{1^2} + {I_{sw}}^2}$$

$$V_{sw} = I_{sw}R_{sw} = \frac{h_2}{\sqrt{3}}$$

where

h_2 is the hysteresis band voltage.

$$V_{ref1} = I_{SC1}X_{C1} = \frac{Ise1}{2\pi f 1 Cse} \qquad (7)$$

The resistance (R_{sw}) and the capacitance (C_{se}) values are expressed in terms of band voltage V_{sw} and rated references voltage (V_{ref1}), respectively, and are given by

$$R_{sw} = \frac{h_2}{I_{sw}\sqrt{3}}$$

$$C_{se} = \frac{Ise1}{Vref12\pi f1} \qquad (8)$$

The interfacing inductor L_{se} has been designed based on the switching frequency of the series active filter and is given by

$$L_{se} = \frac{(V_{bus})R_{SW}}{4f_{swmax}h2} \qquad (9)$$

where V_{bus} is the total dc-link voltage across both the dc-link capacitors. A design example is illustrated for a rated voltage of 230 V line to neutral and the dc-link voltage reference (V_{dvref}) of the conventional VSI topology has been taken as 1.6 for each capacitor [12], [17]. The hysteresis band ($h1$) is taken as 0.5 A. From (5), the interfacing inductance (L_f) is computed to be 26mh. The base KVA rating of the system is taken as 5 KVA. Using (3), C_{dc} is computed and found to be $2200u_f$. The rated series VSI voltage is chosen as 50% of the rated voltage, i.e., the maximum injection capacity of the series active filter is 115V. The hysteresis band (h_2) for series active filter is taken as 3% of the rated voltage, i.e., 6.9V.

TABLE-I
SYSTEM PARAMETERS

System Quantities	Values
System Voltages	230V(Line to neutral), 50HZ
Feeder impedance	$Z_S = 1 + j3.141\Omega$
Linear Load	$Z_{la} = 34 + j47.5\Omega$, $Z_{lb} = 81 + j39.6\Omega$, $Z_{lc} = 31.5 + j70.9\Omega$
Non-linear Load	Three-phase full bridge rectifier load feeding a R-L Load of 150Ω-300mh
Shunt-VSI Parameters	$C_{dc} = 2200\mu F, L_f = 26mH$, $R_f = 1\Omega$, $V_{dbus} = 2 * V_{dc} = 1040V(Conventional)$ $V_{dbus} = 560V(Proposed)$
Series-VSI Parameters	$C_{se} = 80\mu f, L_{se} = 5mh$, $R_{SW} = 1.5\Omega$
Series interfacing transformer	1:1,100V,and 700V
PI Controller gains	$K_P = 6.6, K_i = 5.5$
Hysteresis band	$h_1 = \pm 0.5A, h_2 = \pm 6.9V$

C. Design of C_f proposed Topology:

The design of the C_f depends upon the value to which the dc-link voltage is reduced. In general, loads with only nonlinear components of currents are very rare, and most of the electrical loads are combination of the linear inductive and nonlinear loads. Under these conditions, the proposed topology will work efficiently. The design of the value of C_f is carried out at the maximum load current, i.e., with the minimum load impedance to ensure that the designed C_f will perform satisfactorily at all other loading conditions. If S_{wmax} is the maximum KVA rating of a system and V_{base} is the base voltage of the system, then the minimum impedance in the system is given as

$$Z_{min=} \frac{V_{base}^2}{S_{max}} = |Rl + jXl)| \qquad (10)$$

In order to achieve the unity power factor, the shunt active filter current needs to supply the required reactive component of the load current, i.e., the fundamental imaginary part of the filter Current should be equal to the imaginary part of the load current. The filter current and load current in a particular phase are given below

$$I_{filter} = \frac{V_{inv1} - V_{l1}}{R_{f+j(Xlf-Xcf)}} \qquad (11)$$

$$I_{load} = \frac{Vl1}{Rl+jXl} \qquad (12)$$

where

$$V_{inv1} = \frac{0.612 V_{dc}}{2\sqrt{3}} \qquad (13)$$

V.UPQC CONTROL BLOCK DIAGRAM

In this work, the load currents are unbalanced and distorted, these currents flow through the feeder impedance and make the voltage at terminal unbalanced and distorted. The series active filter makes the voltages at PCC balanced and sinusoidal. However, the voltages still contain switching frequency components and they contain some distortions. If these terminal voltages are used for generating the shunt filter current references, the shunt algorithm results in erroneous compensation [19]. To remove this limitation of the algorithm, fundamental positive sequence voltages $v+la1(t)$, $v+lb1(t)$, and $v+lc1(t)$ of the PCC voltages are extracted and are used in control algorithm for shunt active filter [19]. The expressions for reference compensator currents are given in (17). In this equation, P_{lavg} is the average load power, p_{loss} denotes the switching losses in actual compensator, and it is generated using a capacitor voltage PI controller. The term P_{lavg} is obtained using a moving average filter of one cycle window of time T in seconds. The term φ is the desired phase angle between the source voltage and current

$$i_{fa}{}^* = i_{la} - i_{sa}{}^* = i_{la} - \frac{V_{+la1} + \gamma(V_{+lb1} - V_{+lc1)(P_{lavg}+P_{loss})}}{\Delta_{+1}}$$

$$i_{fb}{}^* = i_{lb} - i_{sb}{}^* = `i_{lb} - \frac{V_{+lb1} + \gamma(V_{+lc1} - V_{+la1)(P_{lavg}+P_{loss})}}{\Delta_{+1}}$$

$$i_{fc}{}^* = i_{lc} - i_{*sc} = i_{lc} - \frac{V_{+lc1} + \gamma(V_{+la1} - V_{+lb1)(P_{lavg}+P_{loss})}}{\Delta_{+1}} \qquad (14)$$

where:

$$\Delta = \sum_{j=a,b,c}(V_{+lj1})^2 \ , \quad \gamma = \frac{tan\varphi}{\sqrt{3}}$$

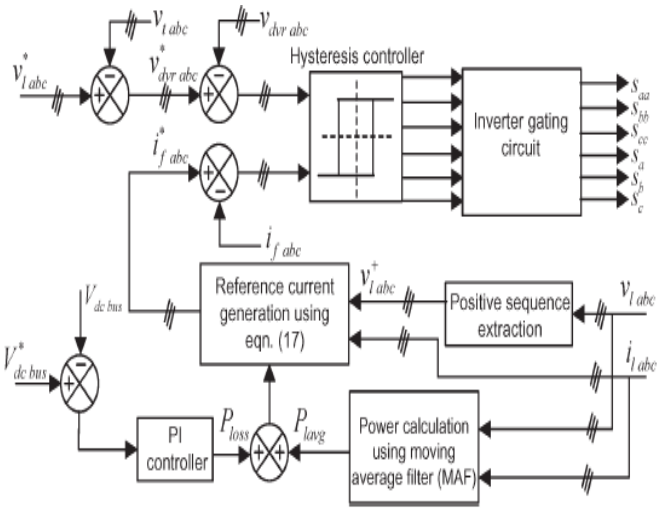

Fig.4.Shows Control Block diagram of UPQC

The above algorithm gives balanced source currents after compensation irrespective of unbalanced and distorted supply. The reference voltages for series active filter are given as

$$V_{dvri}{}^{*} = V_{li}{}^{*} - V_{ti}$$

i = a, b, c

Where $V_{li}{}^{*}$ represents the desired load voltages in three phases, and represents $V_{dvri}{}^{*}$ the reference series active filter voltages. The switching Control for shunt active filter is given below as:

If $i_{fa \geq i_{fa}{}^{*}+h_1}$, then bottom switch is turned ON whereas top switch is turned OFF (Sa = 0,Sa' =1).

If $i_{fa} \leq i_{fa}{}^{*} - h_1$, then top switch is turned ON whereas bottom switch is turned OFF (Sa = 1, Sa'= 0).

Similarly the switching commands for series active filter are given as follows.
If $V_{dvra} \geq V_{dvra}{}^{*} + h_2$, then bottom switch is turned ON whereas top switch is turned OFF (S_{aa} = 0, $S_{aa}{}''$ = 1).

If $V_{dvra} \leq V_{dvra}{}^{*} - h_2$, then top switch is turned ON whereas bottom switch is turned OFF (S_{aa}= 1, $S_{aa}{}''$ = 0).

VII.SIMULINK DIGRAMS AND RESULTS

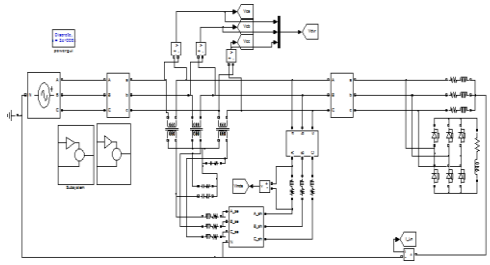

Fig: 5. Shows simulation model of Conventional Topology of UPQC

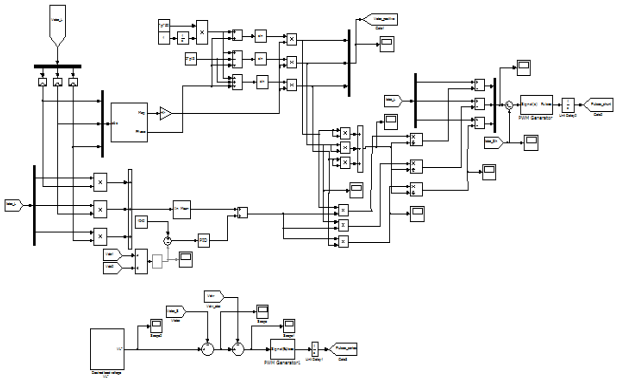

Fig: 6. Shows Control circuit of Conventional Topology of UPQC

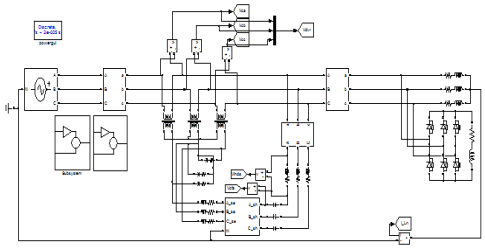

Fig: 7. Shows Simulation model of Modified Topology of UPQC

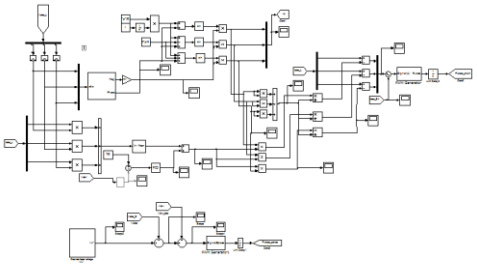

Fig.8. Shows Control Circuit of Modified Topology of UPQC

SIMULATION RESULTS:
CONVENTIONAL TOPOLOGY RESULTS:

In order to validate the Conventional topology, simulation is carried out using MATLAB software

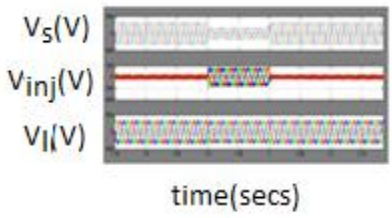

Fig. 9. a) Terminal voltages with sag b) DVR-injected voltages c) load voltages after compensation

Fig: 9. Shows a) The compensation performance of the series active filter. A Sag of 50% is considered in all phase of the terminal voltages for five cycles, which start form 1.9s and ends at 2.0s. fig. 9.b. shows the compensated DVR voltages and load voltages after compensation as shown in fig. c. The load voltage are maintained to the desired voltage using series active filter

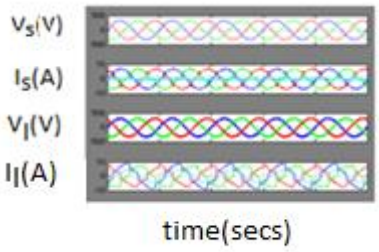

Fig. 10. a) Source voltage b) source current c) Load voltage d)Load current

Fig.10.Shows the load currents and terminal voltages after compensation. The load currents are unbalanced and distorted, also the terminal voltages are distorted because these load currents flow through the feeder impedance in the system.

Fig.11.Shows.a) The three-phase shunt compensators currents are shown in fig. b)The voltage across the interfacing inductor in phase-a, as shown in fig. The peak-to-peak voltage across the inductor is 1040V.

Fig.12. Shows The dc-link voltage across the top and bottom dc-link capacitors are shown in fig. Using PI controller, the voltage across both dc capacitors are maintained constant to a reference values of 520V as shown in fig.

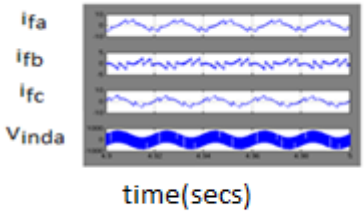

Fig.11. a) Shunt active filter currents. b)voltage across the interfacing inductor in phase-*a* of the shunt active filter.

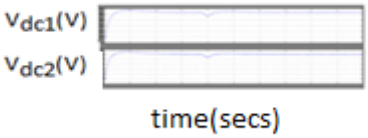

Fig.12. dc- link capacitor voltages

PROPOSED TOPOLOGY RESULTS:

In order to validate the Conventional topology, simulation is carried out using MATLAB software

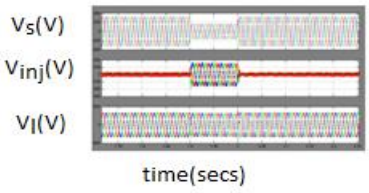

Fig. 13. a) Terminal voltages with sag b)DVR-injected voltages c) load voltages after compensation

Fig.13. Shows a) The compensation performance of the series active filter. A Sag of 50% is considered in all phase of the terminal voltages for five cycles, which start form 1.9s and ends at 2.0s.b)The compensated DVR voltages and load voltages

after compensation as shown in fig. c) The load voltage are maintained to the desired voltage using series active filter

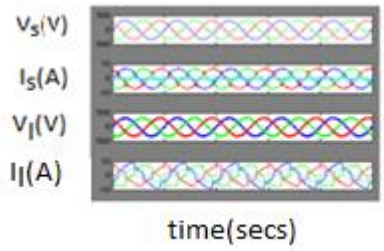

Fig.14. a) Source voltage b) source current c) Load voltage d)Load current

Fig.14. Shows The load currents and terminal voltages after compensation using proposed Topology are shown in fig. The load currents are unbalanced and distorted as shown in fig. The terminal voltages are also distorted because these load currents flow through the feeder impedance in the system as shown in fig.

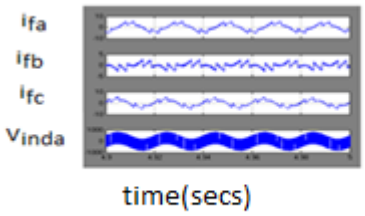

Fig.15. a) Shunt active filter currents. b) voltage across the interfacing inductor in phase-*a* of the shunt active filter.

Fig.15.Shows a) The three-phase shunt compensators currents are shown in fig b) The voltage across the inductor is shown in Fig. the peak-to-peak voltage is 560 V, which is far lesser than the voltage across the inductor using conventional topology. As the voltage across inductor is high in case of conventional topology, the rate of rise of filter currentd_{if}/dt will be higher than that of modified topology. This will allow the filter current to hit the hysteresis boundaries at a faster rate and increases the switching, whereas in modified topology, the number of switching will be less. Thus, the average switching frequency of the switches in the proposed topology will be less as compared to conventional topology. Since the average switching is less, the switching loss will also decrease in modified topology.

Fig.16. DC - link capacitor voltage

Fig.16. Shows The dc-link voltage across the dc-link capacitor are shown in fig. Using PI controller, the voltage across dc capacitor are maintained constant to a reference values of 750V as shown in fig.

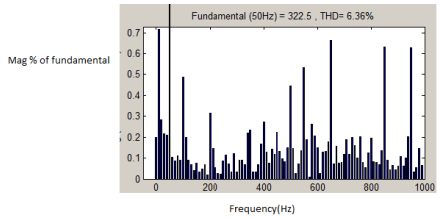

Fig.17.THD of Conventional Topology

Fig.17.Shows THD(total harmonic distortion) of Load Voltage in Conventional topology is high compared to proposed topology because high switching operation

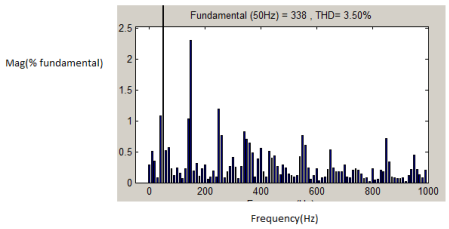

Fig.18.THD of Proposed Topology

Fig.18.Shows in proposed topology total harmonic distortion (THD) reduces because less voltage across the inductor is that the hysteresis band violation will be less. This will improve the quality of compensation, and total harmonic distortion (THD) reduces in the proposed topology. Similarly, the switching in the series active filter also reduces

VIII.CONCLUSION

The voltage sag, swell and other power quality problem can be removed with the help of the Unified Power Quality Conditioner. The design of the modified three phases four wire topology had given and the reduction of the dc link capacitor are discussed. The reduction of average switching loss can be achieved by the help of the control of each leg independently. The control circuit for the UPQC and the generation of the reference current are also explained. The output of the UPQC for the various conditions had been explained by the help of the simulation result. The average switching loss details are explained in the tabulated manner the study, it is found that the modified topology has less average switching frequency, less THDs in the source currents, and load voltages with reduced dc link voltage as compared to the conventional UPQC topology.

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