# A New PFC Rectifier for Air conditioner Applications

TANNERU DURGA PRASAD[1], Asst.Prof N.SAIDA RAO[2]
*Department of Electrical and Electronics Engineering,*
*Anurag Engineering College,*
*Kodad,Nalgonda(Dist),Telangana,India*
[1] durga3300@gmail.com
[2] saidarao.nerella@gmail.com

***Abstract*---** With the widespread use of non-linear loads, such as variable speed drives (VSDs), power factor improvement has become more difficult. The presence of harmonic currents cause power capacitors to absorb them, as capacitor impedance is inversely proportional to frequency. The effects are overheating and increased dielectric stress of power capacitors, which result in their premature failure. These traditional approaches can also interact with harmonics, leading to harmonic amplifications at resonant frequency, which can damage the capacitors or components of the system. A new integrated three-level ac–dc converter is presented. The proposed converter integrates the operation of the boost power factor correction and the three-level dc–dc converter. The converter is made to operate with two independent controllers—an input controller that performs power factor correction and regulates the dc bus and an output controller that regulates the output voltage. The input controller prevents the dc-bus voltage from becoming excessive while still allowing a single-stage converter topology to be used. The paper explains the operation of the new converter in detail and discusses its features and a procedure for its proper design.

***Keywords*- Power factor correction , converters , single stage**

## I.INTRODUCTION

HIGHER power ac–dc converters are required to have some sort of power factor correction (PFC) capability to comply with harmonic standards such as IEC61000-3-2. PFC methods can generally be divided into the following three categories:

1) *Passive PFC converters:* They use passive elements such as inductors and capacitors to filter low frequency input current harmonics and make the input current more sinusoidal. Although these converters are simple and inexpensive, they are also heavy and bulky and are thus used in a limited number of applications.

2) *Two-stage converters:* They consist of an ac–dc boost preregulator converter that shapes the input current and an isolated dc–dc full-bridge converter that converts the preregulator output into the required dc voltage. Two-stage converters, however, require two separate switch-mode converters (each with its own controller), and thus, can be expensive. Moreover, they have poor efficiency when perating under light-load conditions as there are two converter stages that are operating—each with its own set of fixed losses—while a small amount of power is actually transferred to the load. These fixed losses are dominant under light-load operating conditions.

3) *Single-stage converters:* They can perform PFC/ac–dc conversion and dc–dc conversion with just a single full-bridge converter. There have been numerous publications about single-stage PFC (SSPFC) converters particularly for low-power ac–dc fly back and forward converters [1]–[8]. Research on the topic of higher power ac–dc single-stage full-bridge converters, however, has proved to be more challenging, and thus, there have been much fewer publications [9]–[18]. Previously proposed single-stage ac–dc full-bridge converters have the following drawbacks:

a) Some are current-fed converters with a boost inductor connected to the input of the full-bridge circuit. Although they can achieve a near-unity input power factor, they lack an energy-storage capacitor across the primary-side dc bus, which can result in the appearance of high voltage overshoots and ringing across the dc bus. It also causes the output voltage to have a large low-frequency 120-Hz ripple that limits their applications [10].

b) Some are resonant converters [15], [16] that must be controlled using varying switching-frequency control, which makes it difficult to optimize their design (especially theirmagnetic components) as they must be able to operate over a wide range of switching frequency.

c) Most are voltage-fed, single-stage, pulsewidth modulation (PWM) converters with a large energystorage capacitor connected across their primaryside dc bus. These converters do not have the drawbacks of resonant and current-fed SSPFC converters. They operate with fixed switching frequency, and the bus capacitor prevents voltage overshoots and ringing from appearing across the dc bus and the 120-Hz ac component from appearing at the output. Voltage-fed converters, however, have the following drawbacks:

i) The primary-side dc-bus voltage of the converter may become excessive under highinput- line and low-output-load conditions [10]. This is because SSPFC converters are implemented with just a single controller to control the output voltage, and the dc-bus voltage left unregulated. The high dc-bus voltage results in the need for higher voltage rated devices and very large bulk capacitors for the dc bus.

 

For example, the converter in [9] has a dc-bus voltage of 600 V.

ii) The input power factor of a single-stage voltage-fed converter is not as high as that of current-fed converters. For example, the converter proposed in [12] has an input current that is neither continuous nor discontinuous, but is "semicontinuous" with a considerable amount of distortion.

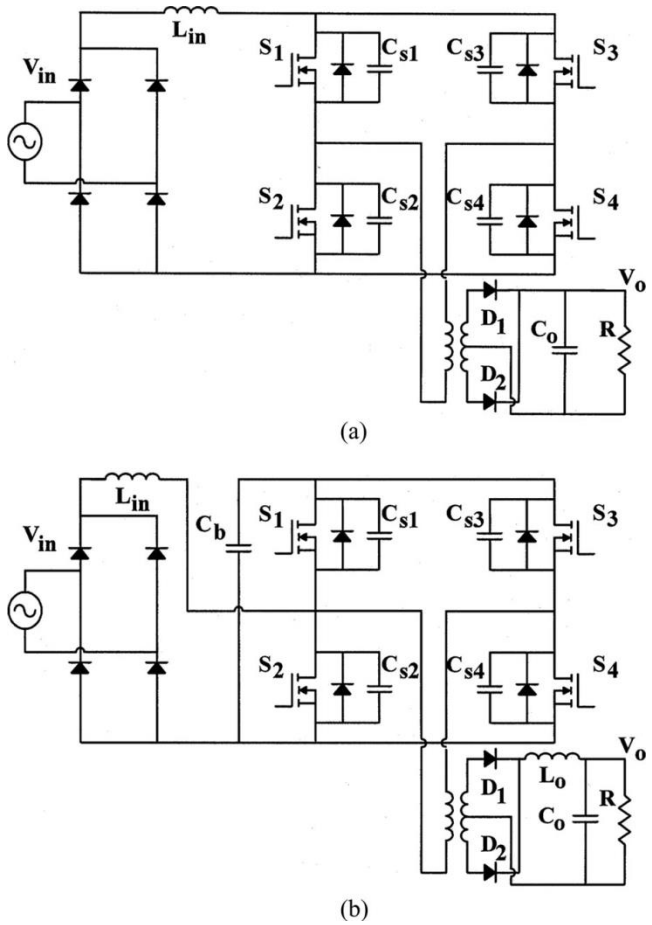


Fig. 1. Various single-stage power factor correction converters. (a) Boostbased current-fed ac–dc PWM integrated full-bridge converter [3]. (b) SSPFC PWM full-bridge converter [10].

iii) The converter is made to operatewith an output inductor current that is discontinuous for all operation conditions or some parts of operation conditions [9], [11], [12], [18], to try to prevent the dc-bus voltage from becoming excessive; output inductor current and dc-bus voltage are related, as shown in [11]. Doing so results in the need for components that can handle high peak currents and additional output filtering to remove ripple.

Problems associated with single-stage converters; excessive dc-bus voltages due to the lack of a dedicated controller to regulate these voltages, large output ripple, distorted input currents, reduced efficiency (particularly for lowinput line voltages due to a low dc-bus voltage generally exist for two-level single-stage converters, such as the ones shown in Fig. 1 and three-level converters [15], [16], [19]–[22].

In the paper, a new single-stage ac–dc converter that does not have the drawbacks of previously proposed single-stage and two-stage converters is proposed. The paper introduces the new converter, explains its basic operating principles and its modes of operation, and discusses its features and its design. The feasibility of the new converter is confirmed with experimental results obtained from a prototype converter.

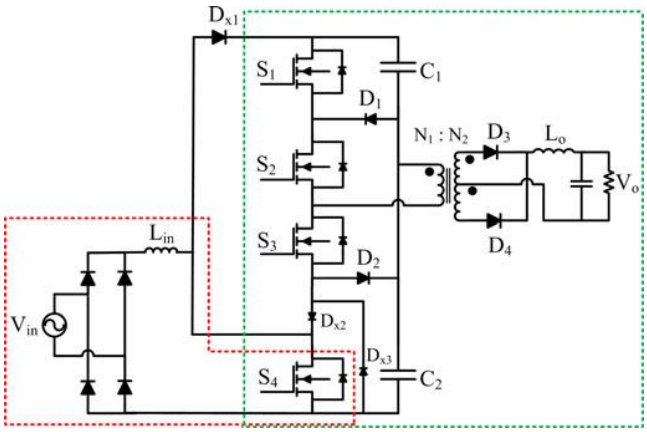


Fig. 2. Proposed single-stage three-level converter.

## II. Operation of the Proposed Converter

The proposed converter, which is shown in Fig. 2, integrates an ac–dc boost PFC converter into a three-level dc–dc converter. The ac–dc boost section consists of an input diode bridge, boost inductor $L_{in}$ , boost diode $D_{x1}$ , and switch $S_4$ , which is shared by the multilevel dc–dc section. When $S_4$ is off, it means that no more energy can be captured by the boost inductor. In this case, diode $D_{x2}$ prevents input current from flowing to the midpoint of capacitors $C_1$ and $C_2$ and diode $D_{x1}$ conducts and helps to transfer the energy stored in the boost inductor $L_{in}$ to the dcbus capacitor. Diode $D_{x3}$ bypasses $D_{x2}$ and makes a path for circulating current. Although there is only a single converter, it is operated with two independent controllers. One controller is used to perform PFC and regulate the voltage across the primaryside dc-bus capacitors by sending appropriate gating signals to $S_4$ . The other controller is used to regulate the output voltage by sending appropriate gating signals to $S_1$ to $S_4$ .

It should be noted that the control of the input section is decoupled from the control of the dc–dc section and thus can be designed separately. The gating signal of $S_1$ , however, is dependent on that of $S_4$ , which is the output of the input controller; how this signal is generated

is discussed in detail later in this paper. The gating signals for $S_2$ and $S_3$ are easier to generate as both switches are each ON for half a switching cycle, but are never ON at the same time.

Typical converter waveforms are shown in Fig. 3, and equivalent circuit diagrams that show the converter's modes of operation are shown in Fig. 4 with the diode rectifier bridge output replaced by a rectified sinusoidal source. it is assumed that the supply voltage is constant within a switching cycle. It is also assumed that the input current is discontinuous, although there is no reason why the input current cannot be made to be continuous if this is what is desired. The converter has the following modes of operation:

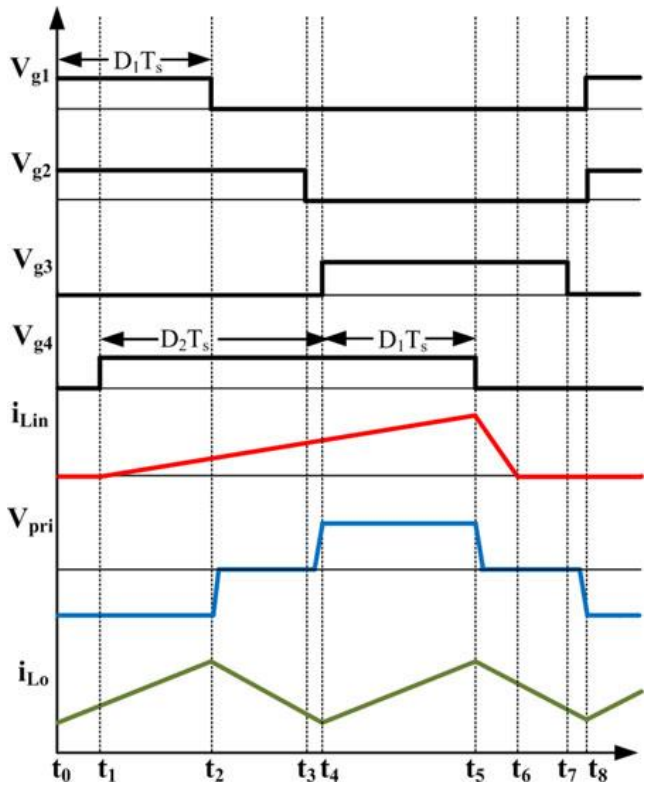


Fig. 3. Typical waveforms describing the modes of operation.

1) *Mode 1 ($t_0 \le t \le t_1$ ):* During this mode, switches $S_1$ and $S_2$ are ON and energy from dc-bus capacitor $C_1$ is transferred to the output load. In the output section, a positive voltage of $(V_{pri}/n) - V_0$ (where $n$ is the ratio of primary to secondary transformer turns) is impressed across $L_o$ and the current through it rises.

2) *Mode 2 ($t_1 \le t \le t_2$ ):* In this mode, $S_1$ and $S_2$ remain ON and $S_3$ turns ON. The energy from dc bus capacitor $C_1$ is transferred to the output load. At the same time, the diode bridge output voltage $V_{rec}$ is impressed across input inductor $L_{in}$ so that the current flowing through this inductor rises.

3) *Mode 3 ($t_2 \le t \le t_3$ ):* In this mode, $S_1$ and $S_2$ remain ON and $S_3$ turns ON. The energy from dc-bus capacitor $C1$ is transferred to the output load. At the same time, the diode bridge output voltage $V_{rec}$ is impressed across input inductor $L_{in}$ so that the current flowing through this inductor rises voltage $V_{rec}$ is impressed across input inductor $L_{in}$ so that the current flowing through this inductor rises.

4) *Mode 4 ($T_3 \le t \le T_4$ ):* In this mode, $S_1$ and $S_2$ are OFF and $S_4$ is ON. The current in the primary of the transformer charges capacitor $C_2$ through the body diode of $S_3$ and $DX_3$.

5) *Mode 5 ($T_4 \le t \le T_5$ ):* In this mode, $S_3$ and $S_4$ are ON. Energy flows from capacitor $C_2$ flows into the load while the current flowing through input inductor $L_{in}$ continues to rise.

6) *Mode 6 ($T_5 \le t \le T_6$ ):* In this mode, $S_4$ turns off. The current in input inductor flows thorough the diode $DX_1$ to charge the capacitors $C_1$ and $C_2$ . The current in the transformer primary flows thorough the $S_3$ and $D2$. This mode ends when the inductor current reaches zero. Also during this mode, the load inductor current freewheels in the secondary of the transformer.

7) *Mode 7 ($T_6 \le t \le T_7$ ):* In this mode, the load inductor current freewheels in the secondary of the transformer. This mode ends when the switches $S_3$ turns off.

8) *Mode 8 ($T_7 \le t \le T_8$ ):* In this mode, $S_3$ is OFF and the current in the primary of the transformer charges capacitor $C_1$ through the body diodes of $S_1$ and $S_2$ . Finally, converter reenters Mode 1.

The simplified schematic of the power converter and the respective controllers are shown in Fig. 5. The decoupling of the input controller and output controller can occur because the crossover frequencies of the two loops are very different. The crossover frequency of the input controller, which performs input power factor correction and converts input ac into an intermediate dc-bus voltage (voltage across the two primary-side dc-bus capacitors), is much lower than that of the output controller, which converts the intermediate dc-bus voltage into the desired output voltage. Since the two crossover frequencies are far apart, it is therefore possible to consider the design of one controller to be separate from that of the other. Since the two controllers are decoupled, the standard designs for an ac–dc

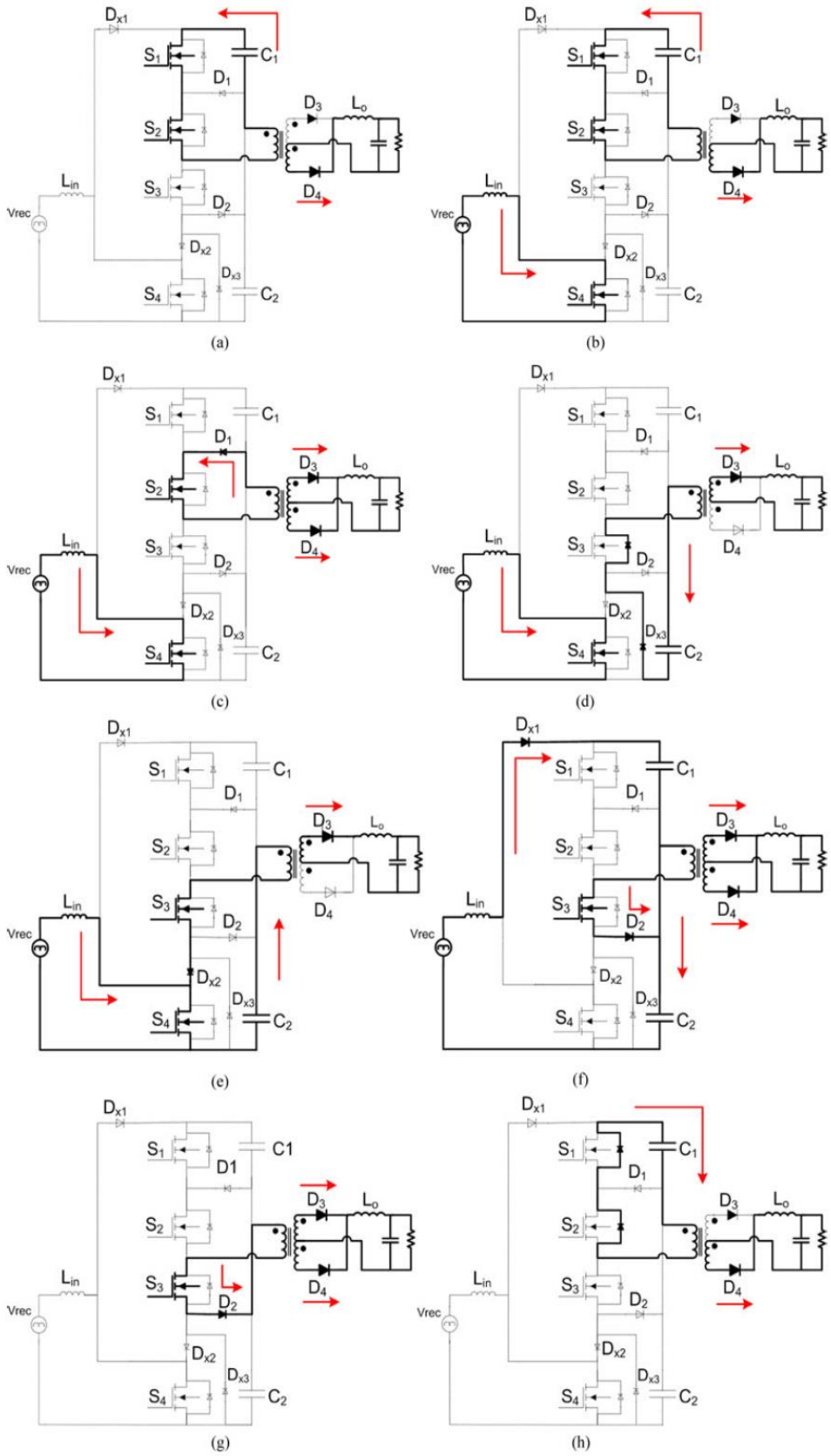


Fig. 4. Equivalent circuits for each operation stage for the converter. (a) Mode 1 $(t_0 < t < t_1)$. (b) Mode 2 $(t_1 < t < t_2)$. (c) Mode 3$(t_2 < t < t_3)$. (d) Mode 4$(t_3 < t < t_4)$. (e) Mode 5 $(t_4 < t < t_5)$. (f) Mode 6 $(t_5 < t < t_6)$. (g) Mode 7 $(t_6 < t < t_7)$. (h) Mode 8 $(t_7 < t < t_8)$

Fig. 5 shows a simple diagram of the controller scheme that has two elements of control. One element is to control dc–dc conversion of the dc-bus voltage to the desired output voltage, and this can be done by controlling the gating signals of $S_1$ to $S_4$ through controlling duty cycle of $D_1$ . The other element is to control duty cycle of the switch $S_4$ to regulate the dc-bus voltage and to perform input power factor correction. This can be done by controlling $D_2$ and then adding duty cycle of $D_2$ to $D_1$ (where $D_1$ and $D_2$ are defined in Fig. 3); thus $S_4$ performs two tasks; one part ($D_1$ ) participate to control output voltage and another part ($D_2$ ) to regulate dc-bus voltage.

## III. Converter Features

The proposed converter has the following features:

1) *Reduced cost compared to two-stage converters:* Although the proposed converter may seem expensive, the reality is that it can be cheaper than a conventional two-stage converter. This is because replacing a switch and its associated gate drive circuitry with four diodes reduces cost considerably even though the component count seems to be increased—this is especially true if the diodes are ordered in bulk numbers.
2) *Better performance than a single-stage converter:* The proposed single-stage converter can operate with a better input power factor for universal input line applications than a single-controller, single-stage because it does have a dedicated controller for its input section that can perform PFC and regulate the dc-bus voltage. The presence of a second controller also allows the converter to operate with better efficiency and with less output ripple as each section of the converter can be made to operate in an optimal manner.
3) *Improved light-load efficiency:* The proposed converter can be designed so that it has a conventional dc-bus voltage of 400 V. Since the converter is a multilevel converter, a 400 V dc bus means that each switch will be exposed to a maximum voltage of 200 V. Having 200 V across a MOSFET device instead of 400 V (as is the case with two-level converters) results in a 75% reduction in turnon losses when the converter is operating under light-load conditions and there is an insufficient amount to current available to discharge the switch output capacitances before the switches are turned on.
4) *Increased design flexibility:* Since the converter is a multilevel converter, it can be operated with high dc-bus voltage (800 V), standard dc-bus voltage (400 V), or any dc-bus voltage 400 V < $V_{bus}$ < 800 V. There are advantages to operating with high dc-bus voltage or with standard dcbus voltage. The fact there is flexibility in the level that the dc-bus voltage is set means that there is considerable flexibility in the design of the converter. This gives the designer options as to how to optimize the design of the converter for other factors such as efficiency profile and cost (i.e. cost of switches based on voltage rating considerations and availability). It should be noted that this design flexibility makes the design of the three-level converter to be much simpler than that of a single-stage two-level converter or that of a single-controller three-level single-stage converter as the dc-bus voltage can be fixed to a desired level that is considered appropriate. determining whether to use the proposed converter versus a conventional two-stage converter, the main tradeoff that needs to be considered is lower cost and improved light-load efficiency versus heavy-load efficiency.

## IV. Converter Design

A procedure for the design of the converter is presented in this section and is demonstrated with an example. The converter is to be designed with the following parameters for the example:

1) input voltage: $V_{in} = 90-265\ V_{rms}$ ;
2) output voltage: $V_o = 48$ V;
3) maximum output power: $P_o = 1350$ W
4) switching frequency: $f_{sw}=1/T_{SW} = 50$ kHz;
5) input current harmonics: IEC1000-3-2 for Class D electrical equipment.

### *A. Step 1: Determine Value for Output Inductor $L_o$*

The output inductor should be designed so that the output current is made to be continuous under most operating conditions. The minimum value of $L_o$ should be the value of $L_o$ with which the converter's output current will be continuous on the when the converter is operating with maximum input voltage, minimum duty cycle ($D_{min}$), and at least 50% of maximum load. The minimum value of $L_o$ can, therefore, be determined to be

$$L_{O,min} \geq \frac{V_O^2}{0.5\ P_{O.max}} \frac{1-D_m}{2} \frac{T_{SW}}{2} \quad (1)$$

Substituting $P_{o,max} = 1350$ W, $V_o = 48$ V, $T_{SW} = 20\ \mu$s, and $D_m = 0.45$ gives $L_{o,min} \geq 9.36\ \mu$H and the value of $L_o$ should be larger to provide some margin. It should be noted that such a value is considerably higher than what is typically found in most other single-stage full-bridge converters, which must operate with very low output inductor values to prevent the dc-bus voltage from becoming excessive. A value of $L_o = 10\ \mu$H, which is just above 9.36 $\mu$H, is chosen.

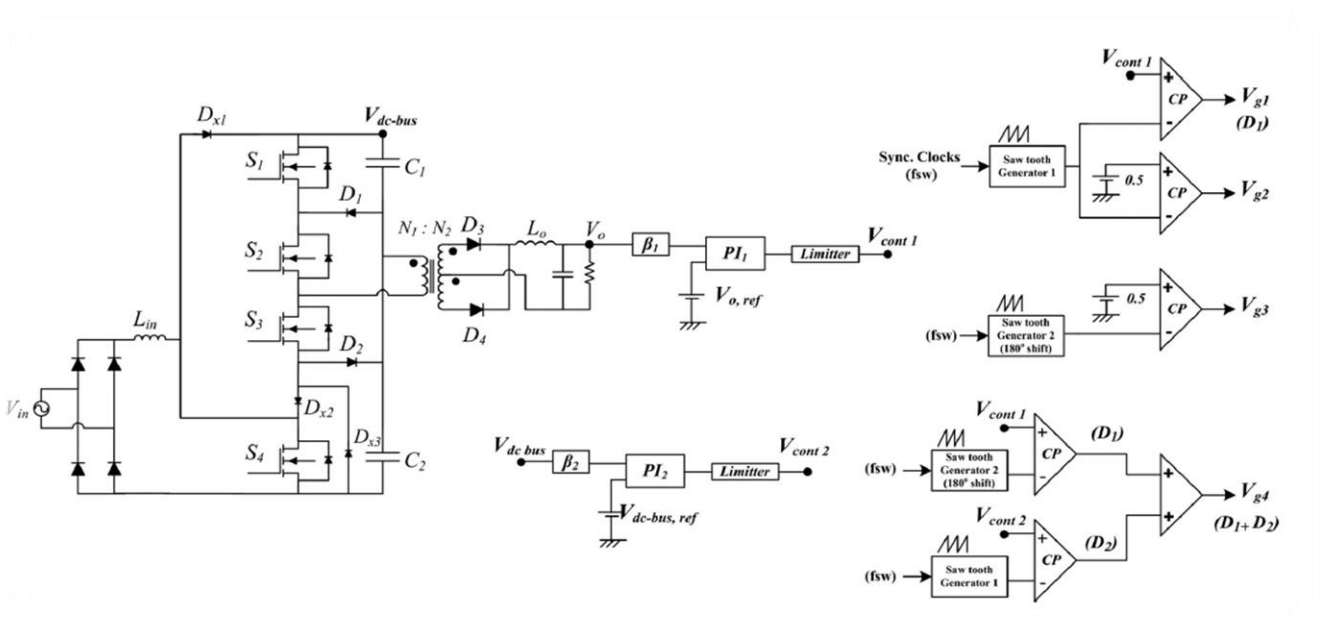


Fig. 5. Simplified schematic control of the proposed converter.

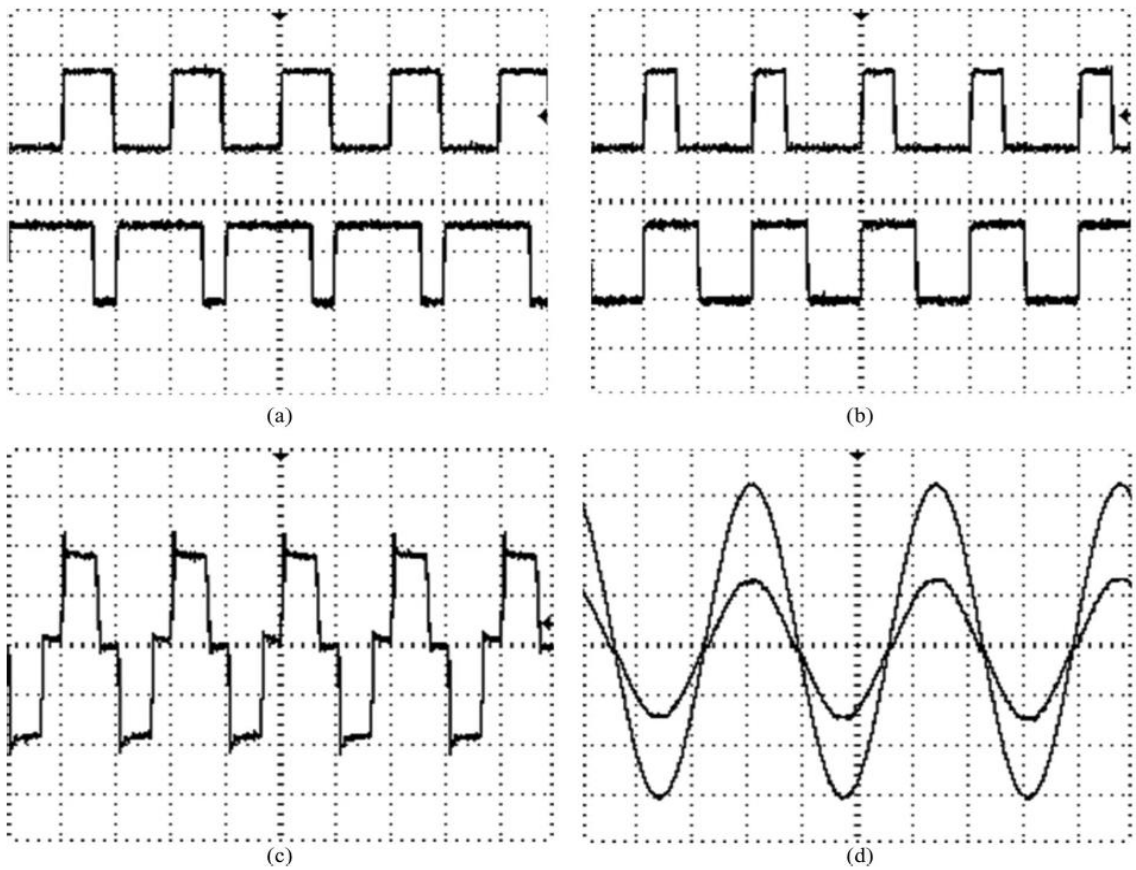


Fig. 6. Typical Experimental results. (a) Top switch voltages $V_{gs1}$ and $V_gs2$. (b) Bottom switch voltages $V_{gs3}$ and $V_{gs4}$. (c) Primary voltage of the main transformer. (d) Input current and voltage.

 

B. Step 2: Determine Value for Turns Ratio of Main Transformer N

The relation between $V_{bus}$, D, $V_o$ and N is

$$V_o = \frac{V_{bus}}{2N}.D. \quad (2)$$

The minimum value of N can be found by considering the case when the converter must operate with minimum input line and, thus, minimum primary-side dc-bus voltage $V_{bus,min}$ and maximum duty cycle $D_{max}$. If the converter can produce the required output voltage and can operate with continuous output currents in this case, then it can do so for all cases

$$V_o \geq \frac{V_{bus,min}}{2V_o}.D_{max} \quad (3)$$

$V_{bus}$ = 650 V and it is achieved by controlling the $S_4$ . Substituting $V_o$ = 48 and $D_{max}$ = 0.75, then the value of N should be equal or more than 5. In this example, the value of transformer ratio is considered to be equal to N = 5.

C. Step 3: Determine Value for Inductor $L_{in}$

The value for $L_{in}$ should be low enough to ensure that the input current is fully discontinuous under all operating conditions, but not so low as to result in excessively high peak current. For the case where $L_{in}$ is such that the input current remains discontinuous for all operating conditions, the minimum value of $L_{in}$ determine as

$$L_{in}, max < \frac{[(V_{bus,min})]^2 * D_{max} * (1-D_{max})^2}{2P_{o,max} f_{SW}} \quad (4)$$

where $D_{max}$ = 0.75, $V_{bus,min}$ = 650 V, $P_{o,max}$ = 1.35 kW, and $f_{SW}$ = 50 kHz. The minimum value of $L_{in}$ = 114 $\mu$H is found. For this design, $L_{in}$ = 80 $\mu$H is used.

It should be noted that two controllers can be designed taking into considerations that their crossover frequencies should be wide apart on the *s*-plane. This is to ensure that the two controllers do not interact with each other. As mentioned earlier, one controller is used to control dc-bus voltage and shape the input current and one controller for control output voltage. The time constant for PFC controller should be faster in compare to output voltage controller.

## V. Experimental Results

A 48 Vdc, 50 kHz experimental prototype of the proposed converter was built to confirm its feasibility. The input voltage $V_{in}$ = 90–265 $V_{rms}$ . The main switches ($S_1$, $S_2$ , and $S_3$ ) were FDL100N50 F and switch $S_4$ was IXFH20N100P and the diodes were UF1006DICT. The input inductance is $L_{in}$ = 80 $\mu$H, $L_o$ = 10 $\mu$H, and $C_1$ and $C_2$ = 2200 $\mu$F. The main transformer ratio was 5:1.

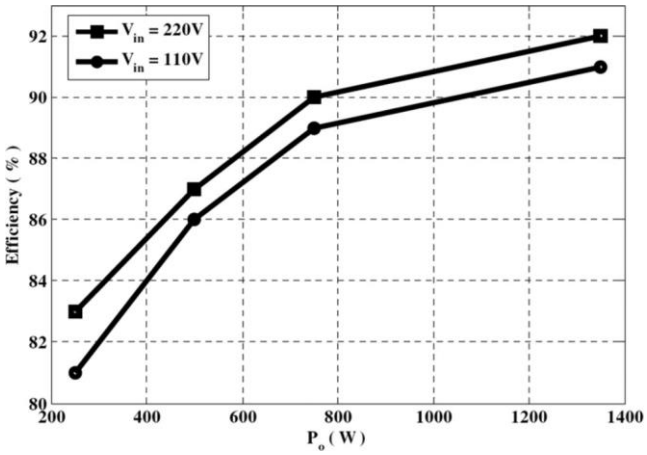


Fig 7 . Experimental efficiency at different value of output power.

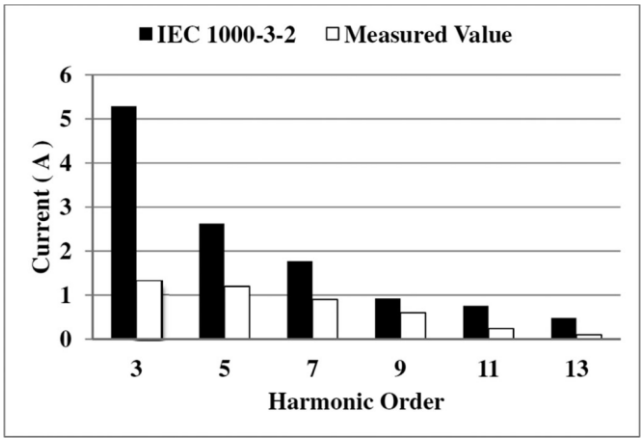


Fig. 8. Input current harmonics at $V_{in}$ = 100 $V_{rms}$, $P_o$ = 1.35 kW compared to IEC1000-3-2 Class A standard.

Typical converter waveforms are shown in Fig. 6. Fig. 6(a) shows typical gating voltage waveforms of the top switches and Fig. 6(b) shows the typical gating voltage waveforms of the bottom switches. Fig. 6(c) shows the voltage across the primary side of the main transformer. It can be seen that the proposed converter manages to impress a standard square voltage waveform across the transformer primary. Fig. 5(d) shows the input voltage and input current after filtering; it can be seen that the input current has no deadbands like those found in single-stage converter

 

input currents, and thus, it has a near unity input power factor.

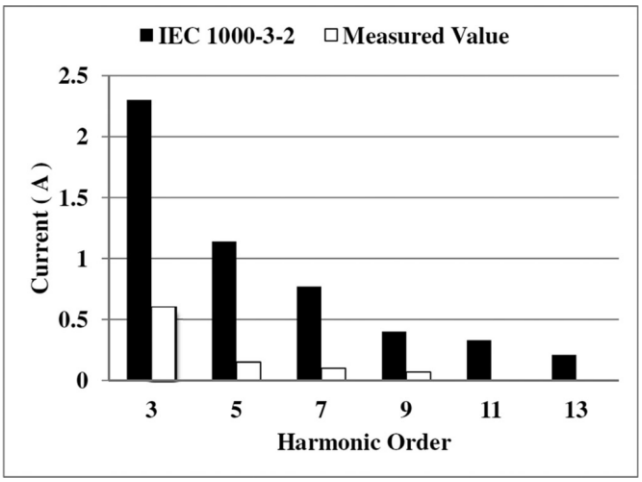


Fig. 9. Input current harmonics at $V_{in}$ = 230 $V_{rms}$, $P_o$ = 1.35 kW compared to the IEC1000-3-2 Class A standard.

Fig. 7 shows the experimental efficiency at different value of output power. It should be noted that the dc-bus voltage was regulated for 650 V for the experimental results. Figs. 8 and 9 show the input current harmonic when $V_{in}$ = 100 and 230 $V_{rms}$ respectively; it can be seen from Figs. 8 and 9 that the converter can meet the IEC1000-3-2 Class A standard for electrical equipment.

## VI. Conclusion

A New PFC Rectifier for Air conditioner Applications With the widespread use of non-linear loads, such as variable speed drives (VSDs), power factor improvement has become more difficult. The presence of harmonic currents cause power capacitors to absorb them, as capacitor impedance is inversely proportional to frequency. The effects are overheating and increased dielectric stress of power capacitors, which result in their premature failure. These traditional approaches can also interact with harmonics, leading to harmonic amplifications at resonant frequency, which can damage the capacitors or components of the system. A new integrated three-level ac–dc converter is presented. The proposed converter integrates the operation of the boost power factor correction and the three-level dc–dc converter. The converter is made to operate with two independent controllers—an input controller that performs power factor correction and regulates the dc bus and an output controller that regulates the output voltage. The input controller prevents the dc-bus voltage from becoming excessive while still allowing a single-stage converter topology to be used. The paper explains the operation of the new converter in detail and discusses its features and a procedure for its proper design.

## Extension:

We can also connect a inverter and use this for BLDC motor drive applications which are used in compressors of Air conditioners. In base paper author discussed only DC-DC converter, now we are converting the obtained DC to AC and then fed to drives

## References

1) J.-Y. Lee, "Single-stage AC/DC converter with input-current dead-zone control for wide input voltage ranges," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 724–732, Apr. 2007.
2) D. D.-C. Lu, H. H.-C. Iu, and V. Pjevalica, "A single-stage AC/DC converter with high power factor, regulated bus voltage, and output voltage," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 218–228, Jan. 2008.
3) H. Ma, Y. Ji, and Y. Xu, "Design and analysis of single-stage power factor correction converter with a feedback winding," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1460–1470, Jun. 2010.
4) H. S. Athab and D. D.-C. Lu, "A high-efficiency ac/dc converter with quasi-active power factor correction," *IEEE Trans. Power Electron.*, vol. 25, no. 5, p. 1103-1109, May 2010.
5) J. M. Kwon, W. Y. Choi, and B. H. Kwon, "Single-stage quasi-resonant flyback converter for a cost-effective PDP sustain power module," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2372–2377, Jun. 2011.
6) H. J. Chiu, Y. K. Lo, H. C. Lee, S. J. Cheng, Y. C. Yan, C. Y. Lin, T. H. Wang, and S. C. Mou, "A single-stage soft-switching flyback converter for power-factor-correction applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2187–2190, Jun. 2011.
7) H. Athab and D. Lu, "A single-switch ac/dc flyback converter using a CCM/DCM quasi-active power factor correction front-end," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1517–1526, Mar. 2012.
8) N. Golbon and G. Moschopoulos, "A low-power ac–dc single-stage converter with reduced dc bus voltage variation," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3714–3724, Jan. 2012.
9) P. K. Jain, J. R. Espinoza, and N. Ismail, "A single-stage zero-voltage zero-current-switched full-bridge DC power supply with extended load power range," *IEEE Trans. Ind. Electron.*, vol. 46, no. 2, pp. 261–270, Apr. 1999.
10) G. Moschopoulos, "A simple AC–DC PWM full-bridge converter with integrated power-factor correction," *IEEE Trans. Ind. Electron.*, vol. 50, no. 6, pp. 1290–1297, Dec. 2003.

 

11) G. Moschopoulos, Q. Mei, H. Pinheiro, and P. Jain, "PWM full-bridge converter with natural input power factor correction," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 39, no. 2, pp. 660–674, Apr. 2003.
12) P. Das, S. Li, and G. Moschopoulos, "An improved AC–DC single-stage full-bridge converter with reduced DC bus voltage," *IEEE Trans. Ind. Electron.*, vol. 56, no. 12, pp. 4882–4893, Dec. 2009.
13) M. S. Agamy and P. K. Jain, "A three-level resonant single-stage power factor correction converter: analysis, design, and implementation industrial electronics," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2095–2107, Jun. 2009.
14) H. L. Cheng, Y. C. Hsieh, and C. S. Lin, "A novel single-stage highpowerfactor ac/dc converter featuring high circuit efficiency," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 524–532, Feb. 2011.
15) M. S. Agamy and P. K. Jain, "A variable frequency phase-shift modulated three-level resonant single-stage power factor correction converter," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2290–2300, Sep. 2009.
16) M. S. Agamy and P. K. Jain, "An adaptive energy storage technique for efficiency improvement of single-stage three-level resonant AC/DC converters," *IEEE Trans. Power Electron.*, vol. 47, no. 1, pp. 176–184, Sep. 2011.
17) H.-L. Cheng,Y.-C.Hsieh, and C.-S. Lin, "Anovel single-stage highpowerfactor AC–DC converter featuring high circuit efficiency," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 524–532, Feb. 2011.
18) G. Moschopoulos and P. Jain, "Single-phase single-stage power-factor corrected converter topologies," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 23–35, Feb. 2005.
19) Y. Gu, Z. Lu, and Z. Qian, "Three level LLC series resonant DC/DC converter," *Proc. IEEE APEC*, pp. 1647–1652, 2004.
20) P. Barbosa, F. Canales, J. Burdio, and F. Lee, "A three level converter and its application to power factor correction," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1319–1327, Nov. 2005.
21) C. Wu and R. Xinbo, "Zero-voltage-switching PWM hybrid full-bridge three-level converter with secondary-voltage clamping scheme," *IEEE Trans. Ind. Electron.*, vol. 55, no. 2, pp. 644–654, Feb. 2008.
22) M. Pahlevaninezhad, P. Das, P. Jain, A. Bakhshai, and G. Moschopoulos, "A self sustained oscillation controlled three level AC/DC single stage converter," *Proc. IEEE APEC*, pp. 1172–1178, 2012.


## AUTHOR'S PROFILE

**TANNERUDURGA PRASAD** received the B.Tech degree in Electrical and Electronics Engineering from ACE Engineering , India in 2012 and at present Pursuing M.Tech with the Specialization of Power Electronics and Electric Drives in Anurag Engineering college Kodad.

**SAIDARAO.NERELLA** graduated in EEE from JNT University Hyderabad in 2009.He received M.Tech degree in the stream of Power Electronics and Electrical Drives in JNT University Hyderabad in 2013, Presently working as Assistant Professor in Anurag Engineering college