Design And Implementation Of MOSFET using ITRS Road map

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Abstract—MOSFETs are used both as discrete devices and as active elements in digital and analog monolithic integrated circuits (ICs). In recent years, the device feature size of such circuits has been scaled down into the deep sub micrometer range. In this paper, a 90 nm NMOS in 3-D structure was designed and simulated to study its electrical characteristics using Visual TCAD with GENIUS simulator with ITRS guideline of 90nm device.

Keywords—**MOSFET, ITRS, Doping**

I. Introduction

The gate length of high-performance MOSFETs has been aggressively scaled year by year because of a strong requirement for constant improvement of circuit performance. The history of the International Technology Roadmap for Semiconductors (ITRS) demonstrates how the gate length of high-performance MOSFETs was scaled in the past and was required to set the pace for scaling in the future. This technology is now well-developed and similar processes of MOSFET fabrication are widely used in industry throughout the world. The scaling of the Complementary Metal Oxide Semiconductor (CMOS) devices to smaller physical dimensions have became the driving force for the semiconductor industry to meet the market's demand for greater functionality and performance of the integrated circuit at Smaller MOSFETs are desirable by main reasons.

II. Proposed Model

a. Structure and Symbol of MOSFET

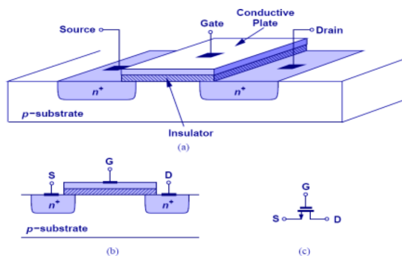

Fig.1

This device is symmetric, so either of the n+ regions can be source or drain.

b. State of the Art MOSFET Structure

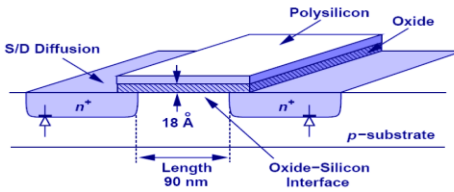

Fig.2

C. Formation of Channel

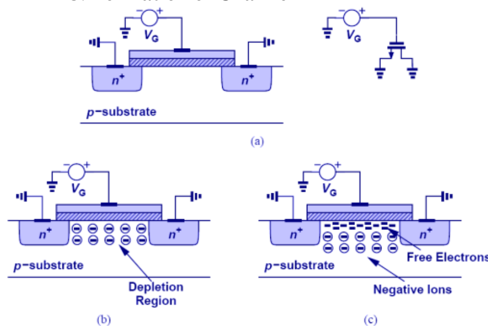

Fig.3

First, the holes are repelled by the positive gate voltage, leaving behind negative ions and forming a depletion region. Next, electrons are attracted to the interface, creating a channel ("inversion layer").

Voltage-Dependent Resistor

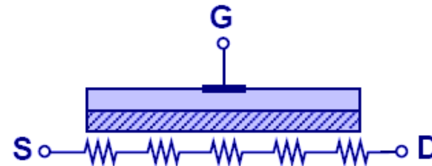

Fig.4

The inversion channel of a MOSFET can be seen as a resistor.

Since the charge density inside the channel depends on the gate voltage, this resistance is also voltage-dependent.

Voltage-Controlled Attenuator

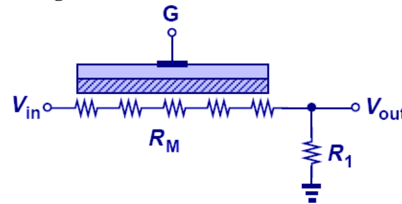

Fig.5

As the gate voltage decreases, the output drops because the channel resistance increases. This type of gain control finds application in cell phones to avoid saturation near base stations.

Breakdown of p-channel MOSFET performance enhancement components.

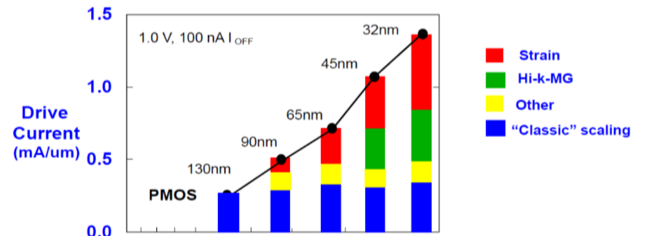

Fig.6

MOSFET Characteristics

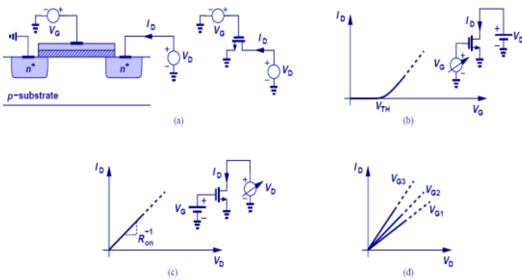

Fig.7

The MOS characteristics are measured by varying VG while keeping VD constant, and varying VD while keeping VG constant.(d) shows the voltage dependence of channel resistance.

L and tox Dependence

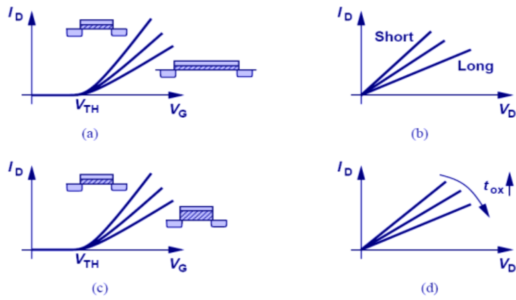

Fig.8

Small gate length and oxide thickness yield low channel resistance, which will increase the drain current.

Channel Potential Variation

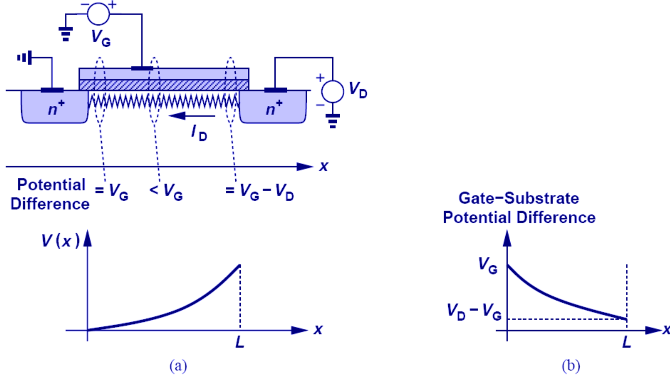

Fig.9

Since there's a channel resistance between drain and source, and if drain is biased higher than the source, channel potential increases from source to drain, and the potential between gate and channel will decrease from source to drain.

Channel Pinch-Off

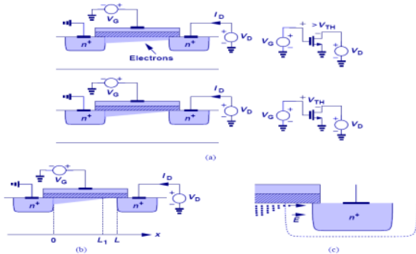

Fig.10

As the potential difference between drain and gate becomes more positive, the inversion layer beneath the interface starts to pinch off around drain. When VD –VG= Vth, the channel at drain totally pinches off, and when VD –VG> Vth, the channel length starts to decrease.

Parabolic ID-VDS Relationship

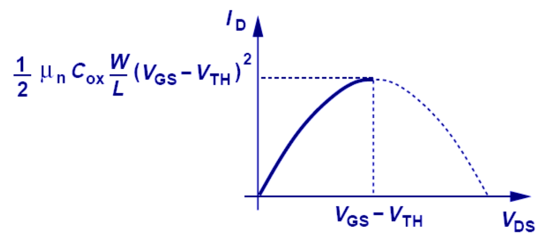

Fig.11

By keeping VG constant and varying VDS, we obtain a parabolic relationship. The maximum current occurs when VDS equals to VGS-VTH.

ID-VDS for Different Values of VGS

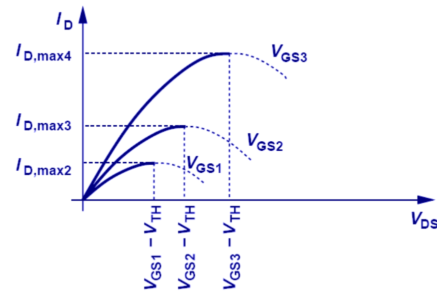

Fig.11

Different Regions of Operation

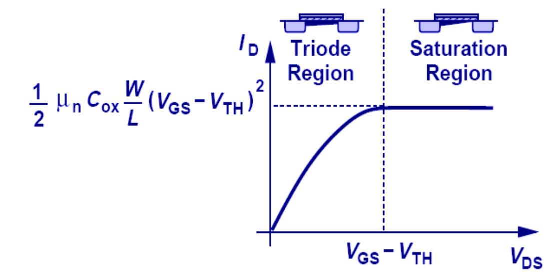

Fig.12

Channel-Length Modulation

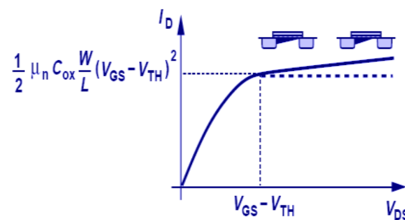

Fig.13

The original observation that the current is constant in the saturation region is not quite correct. The end point of the channel actually moves toward the source as VD increases, increasing ID. Therefore, the current in the saturation region is a weak function of the drain voltage.

III . MOS MODELLING

***MOS MODELLING*:**

Modeling can be defined as "The method of finding the parameter values for fixed simulator model equations".MOS modeling -Writing a set of equations that link voltages and currents. Behavior of the device can be simulated and predicted .Basic MOS model components.1. Equations describing Ids(Vds) and Ids(Vgs).

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Requirements of good MOS model

Good I-V characteristic accuracy. Meet charge conservation requirement. Correct values of small-signal quantities. Good prediction for white and 1/f noise .Ability to provide results even when device operation is quasi static. Ability to include all physical mechanisms for sub-micron devices.

Flowchart of the operation

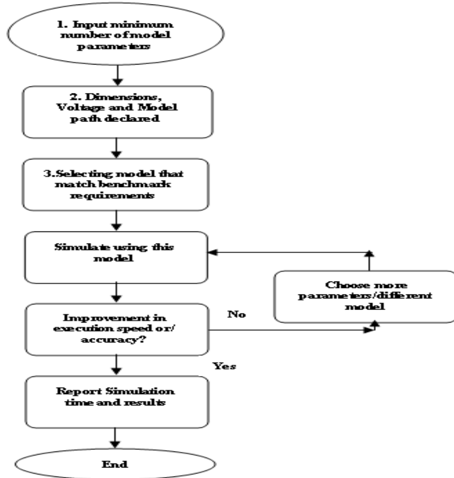

Fig.14 Flowchart for choosing the correct MOS model

The MOSFET Model AND MOSFET Description Lines Model and Element

Process and circuit parameters which apply to a particular class of MOSFETS with varying dimensions are described for that class of MOSFETS in a single .Modelling in which +is used to denote line continuation. The dimensions are given on the element description line. In both, it is critical to watch the units; they are basically illogical. The SPICE element description line for a MOSFET has the following form: Mxxxxxxx nd ng ns <nb> mname <L=val W=val AD=val + AS=val PD=val PS=val NRD=val OFF IC=vds, vgs, vbs TEMP=val>.All parameter value pairs between < and > are optional. Additional optional HSPICE parameters: <RDC=val RSC=val M=val DTEMP=val GEO=val >TEMP=val is not used on element line in HSPICE and not used for level 4 or 5 (BSIM) models.

MODELS AVAILABLE

LEVEL=1	Long channel model developed in 1968 by Shichman-Hodges, applicable for $L > 4$ μm
LEVEL=2	Short channel model, developed in 1980, applicable for $L > 2$ μm. Used by MOSIS program
LEVEL=3	Semi-empirical short channel model, developed in 1980, applicable for $L > 2$ μm (more sophisticated than Level 2)
LEVEL=4	BSIM (Berkeley Short channel IGFET Model), developed in 1985, applicable for $L > 1$ μm (one of the most popular MOSFET Spice models)
LEVEL=5	New BSIM (BSIM2) model
LEVEL=6	Simple empirical short channel model (developed by Sakurai and Newton in 1990))
LEVEL=7	Universal extrinsic short channel MOS model (described by Lee et al. (1993)), applicable for L > 0.1 μm. Allows to describe both subthreshold and above threshold regimes.

Table.1

SPICE Parameters for Parasitics

Parameter Name	Symbol	SPICE Name	Units	Default Value
Source resistance	R_S	RS	Ω	0
Drain resistance	R_D	RD	Ω	0
Sheet resistance (Source/Drain)	$R_\square$	RSH	Ω/□	0
Zero Bias Bulk Junction Cap	C_{j0}	CJ	F/m²	0
Bulk Junction Grading Coeff.	m	MJ	-	0.5
Zero Bias Side Wall Junction Cap	C_{jsw0}	CJSW	F/m	0
Side Wall Grading Coeff.	m_{sw}	MJSW	-	0.3
Gate-Bulk Overlap Capacitance	C_{gbO}	CGBO	F/m	0
Gate-Source Overlap Capacitance	C_{gsO}	CGSO	F/m	0
Gate-Drain Overlap Capacitance	C_{gdO}	CGDO	F/m	0
Bulk Junction Leakage Current	I_S	IS	A	0
Bulk Junction Leakage Current Density	J_S	JS	A/m²	1E-8
Bulk Junction Potential	ϕ_0	PB	V	0.8

Table.2

Hardware description languages (HDLs)

By definition "HDL is a programming language for developing executable simulation models of hardware systems". HDLs describe circuit's operation and design and also have tests to verify the circuit's functionality by simulation. HDLs can be used to design dedicated IC even before the actual circuit is built.

SCHEMATIC DIAGRAM ITRS ROAD MAP

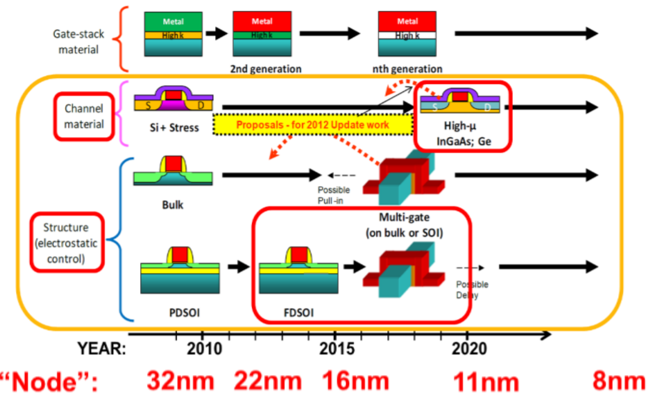

Fig.15

ITRS ROAD MAP

Constructing an integrated circuit, or any semiconductor device, requires a series of operations - photolithography, etching, metal deposition, and so on. As the industry evolved, each of these operations were typically performed by specialized machines built by a variety of commercial companies. This specialization may potentially make it difficult for the industry to advance, since in many cases it does no good for one company to introduce a new product if the other needed steps are not available around the same time. A technology roadmap can help this by giving an idea when a certain capability will be needed. Then each supplier can target this date for their piece of the puzzle.

With the progressive externalization of production tools to the suppliers of specialized equipment, the need arose for a clear roadmap to anticipate the evolution of the market and to plan and control the technological needs of IC production. For several years, the Semiconductor Industry Association (SIA) gave this responsibility of coordination to the United States, which led to the creation of an American style roadmap, the National Technology Roadmap for Semiconductors (NTRS)

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Characteristic	1992	1995	1998	2001	2004	2007
Feature size (microns)	0.50	0.35	0.25	0,18	0,12	0.10
Gates per chip (millions)	0.3	0.8	2.0	5.0	10.0	20.0
Bits per chip						
DRAM	16M	64M	256M	1G	4G	16G
SRAM	4M	16M	64M	256M	1G	4G
Wafer processing cost ($/cm^2)	$4.00	3.90	3.80	3.70	3.60	3.50
Chip size (mm^2)						
logic	250	400	600	800	1,000	1,250
memory	132	200	320	500	700	1,000
Wafer diameter (mm)	200	200	200-400	200-400	200-400	200-400
Defect density (defects/cm^2)	0.10	0.05	0.03	0.01	0.004	0.002
Levels of interconnect (for logic)	3	4-5	5	5-6	6	6-7
Maximum power (watts/die)						
high performance	10	15	30	40	40-120	40-200
portable	3	4	4	4	4	4
Power supply voltage						
desktop	5	3.3	2.2	2.2	1.5	1.5
portable	3.3	2.2	2.2	1.5	1.5	1.5

Table.3

ITRS WORKING GROUP MODELS

Roadmap modeling programs and tables are available to download for your use.**MASTAR** Model for Assessment of cmoS Technologies And Roadmaps (MASTAR) application allows the user to valuate immediately the impact of these technological parameters on the main transistor characteristics such as the threshold behavior, performance values or time delay. Moreover, the influence of “physical” secondary parameters such as mobility, poly depletion and dark space can be visualized giving a deep insight in the physics of CMOS devices.

GTX

GSRC Technology Extrapolation (GTX) provides a robust, portable framework for interactive specification and comparison of modeling choices, e.g., for predicting system cycle time, die size, and power dissipation The GTX provides an open, portable framework for specification and comparison of alternative modeling choices. The GTX paradigm is based on the concepts of "parameters" and "rules."

OVERALL ROADMAP PROCESS AND STRUCTURE

ROADMAPPING PROCESS

The ITRS process and content evolves to match the needs of the semiconductor industry. Collaboration of industry and research continues to be invaluable to understand and assess as well as possible the needs of future inventions and technical challenges in the various spectra of micro- and nano-electronics. Over the past few years, the ITRS teams have worked closely to assess emerging technologies. They indicate an approaching world of vast interconnectedness with humans and hardware, phrased as the internet of things (IOT), and the complex world of information processing known as big data. These examples are only part of the new frontier of invention and discovery. As these new focus topics emerge, the ITRS teams will continue to determine what this means for our global industry. The industry must define the new drivers to help it stay on a path of productivity and profitability, while promoting environmental health and encouraging areas of innovation for new scientists and technologists.

(ITWGs). As time went by the industry became more complex and the number of ITWGs increased to 17 in 2013. As we look forward to the 2015 ITRS it is clear that readjustments on how the ITWGs are configured and the addition of new subjects are necessary. As a result the drivers of the 2015 ITRS and the ITWGs will be redefined in 2014.

CONCLUSION

The foundations of scaling were laid out with the invention of the self-aligned silicon gate process in the late 1960s. Moore’s predictions of the rate of transistor bi-annual growth formulated in 1965 and in 1975 in conjunction with. This chapter provides the material research community with guidance on specific research challenges that must be addressed in a laboratory setting for an emerging family of candidate materials to warrant consideration as a viable ITRS solution. Each international technology working group (ITWG) has identified applications that need new materials with significantly improved properties to meet future technology requirements, enable increased density of devices, and increase energy efficiency for computing and reliability. Based on these requirements, the ERM has identified emerging materials that have properties that could potentially meet their needs for improved density, energy efficiency, and reliability.

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