A Survey of Low Voltage in a Circuit Using LDO Regulator

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***Abstract*— A low-voltage low-dropout (LDO) regulator that converts an input of 1 V to an output of 0.85–0.5 V, with 90-nm CMOS technology is proposed. A simple symmetric operational transconductance amplifier is used as the error amplifier (EA), with a current splitting technique adopted to boost the gain. This also enhances the closed-loop bandwidth of the LDO regulator. In the rail-to-rail output stage of the EA, a power noise cancellation mechanism is formed, minimizing the size of the power MOS transistor. Furthermore, a fast responding transient accelerator is designed through the reuse of parts of the EA. These advantages allow the proposed LDO regulator to operate over a wide range of operating conditions while achieving 99.94% current efficiency, a 28-mV output variation for a 0–100 mA load transient, and a power supply rejection of roughly 50 dB over 0–100 kHz. The area of the proposed LDO regulator is only 0.0041 mm^2, because of the compact architecture.**

***Index Terms*— Fast transient response, high power supply rejection, low-dropout (LDO) regulator, low-voltage, small area.**

I. Introduction

Low-dropout (LDO) regulators work in the same way as all linear voltage regulators. The main difference between LDO and non-LDO regulators is their schematic topology. Instead of an emitter follower topology, low-dropout regulators useopen collector or open drain topology. In this topology, the transistor may be easily driven into saturation with the voltages available to the regulator. This allows the voltage drop from the unregulated voltage to the regulated voltage to be as low as the saturation voltage across the transistorPower management unit with several integrated regula- tors is widely used in modern battery-powered portable devices.These power management schemes often use a pri-mary switching regulator and several postregulators [1], [2]. The primary switching regulator converts the high dc voltage level of the battery (e.g., 4.2–2.7 V) into a low dc voltage level (e.g., 1 V) with a high conversion efficiency (> 90%). The postregulators also generate several independent power sources for multiple voltage domains. The switching regulator inevitably generates voltage ripples over the range of the switching frequency. The switching frequency of the regulator often lies within a low-frequency band of a few 10–100 kHz to reduce switching power loss. The post-regulators should, therefore, be able to provide a good power supply rejec-tion (PSR) ability to suppress these unwanted low-frequency noises. To further maintain high power efficiency, minimize the impact on target load circuits, and reduce cost, these postregulators must operate at low voltage and low quiescent current (I_Q), achieve a fast transient response with a small out-put variation, and minimize their area. The low-dropout regulator has a simple architecture and a fast-responding loop, which makes it the.

A number of previous papers focused on enhancing the transient response [3]–[10] or the PSR [10], [11] or both of LDO regulators. The designs in [3] use either a large driving current or additional circuits, which consume a significant I_Q. The design in [6] consumes a small I_Q, yet has a large output variation during the load transient. The dynamic biasing technique is widely adopted by conducting a very small I_Q under a light load condition. This inevitably sacrifices the transient response during a light to heavy load current transition. The LDO regulators proposed in [2] and [11] achieved a high PSR over a very wide frequency range (up to 10 MHz). Using bipolar junction transistor process technology [11] or a complex ripple cancellation circuit [2] to achieve a PSR >10 MHz at the expense of a high I_Q is, however, unnecessary for the postregulator of a general purpose switching regulator. Further, a complex compensation circuit [6] or a high-gain cascode error amplifier (EA) [7] complicates the LDO regulator design and is not feasible for low-voltage systems (≤1 V) that are using advanced technology. All the previous regulators [2]–[11] are unable to achieve sub 1-V operation.

II. Design Challenges and Concepts of the Proposed Low-Voltage LDO Regulator

A basic LDO regulator is mainly composed of a biasing circuit, an EA, a power MOS transistor (M_P), and a feedback network, as shown in Fig. 1. Now, the transient accelerator (TA) is removed. An off-chip output capacitor (C_L) is used to mitigate the output variations during the load transient. The design challenges and concepts in designing a low-voltage LDO regulator are summarized briefly in the following sections.

A. Low Supply (Input) Voltage and Low I_Q

A high loop gain is mandatory in LDO regulator design to achieve optimum performance values such as accurate output (line/load regulation) and PSR. A low supply voltage and output-resistance reduction induced by a shrinking technology limit the achievable gain of the EA. Thus, there are many auxiliary circuits that consume considerable I_Q that are pro-posed to enhance performance. A M_P with a significant size is required for a specific load current when an LDO regulator sinks current from a low voltage power source. Thus, the EA requires a higher current slew rate to drive the M_P. To achieve low-voltage operation, an EA with not more than three stacked transistors between the supply voltage and ground is preferred;

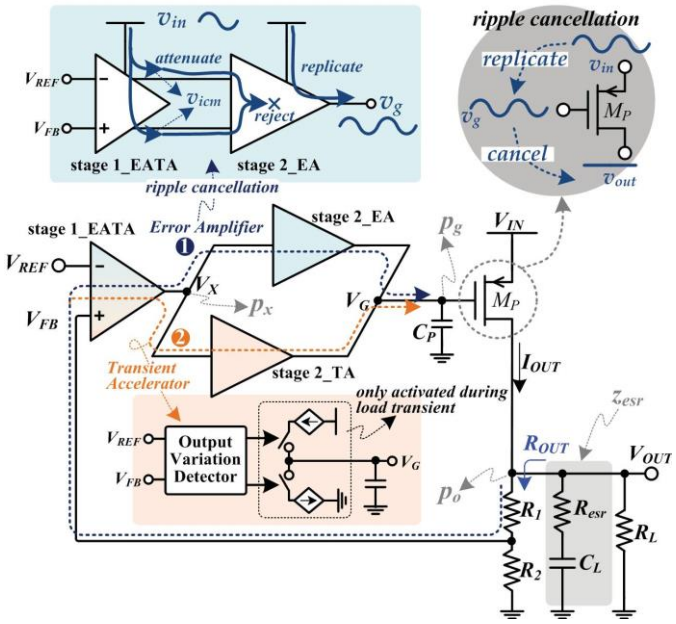

Fig. 1. Conceptual block diagram of the proposed LDO regulator.

each of the transistors, therefore, has more voltage space to stay in the saturation region. A possible candidate can be as simple as an operational transconductance amplifier (OTA) with a low-cost gain-boosting technique like current splitting [12]. The EA also requires a wide output swing to minimize the size of the M_P , and hence relieve the requirement on output current slew rate of the EA.

B. Fast Transient Response

The transient response, includes the voltage variation (spike) and recovery (settling) time during the load current transient. The voltage variation is more important than the recovery time, as even a small output-voltage variation (e.g., 50 mV) can cause severe performance degradation to the load circuit oper-ating at an ultralow supply voltage (e.g., 0.5 V). To reduce the output-voltage variation, both a large closed-loop bandwidth of the LDO regulator and a large output current slew rate of the EA are required [13]. Increasing the closed-loop bandwidth may, however, affect the pole/zero locations and the circuitry may become too complex, consuming more I_Q [4], [8]. The concept of the TA, shown in Fig. 1, is, therefore, adopted to conditionally provide extra charging/discharging current paths (slew current), depending on the status of the output variation detector.

C. Power Reduced

To provide a clean and accurate output voltage with a low voltage level (≤1 V), noise suppression is paramount. An *n*-type power MOS transistor or a cascoded power MOS transistor structure can achieve a high PSR; however, they are unfeasible for sub 1-V operations. As an LDO regulator adopts a *p*-type power MOS transistor, either a high loop gain or good noise cancellation at node V_G can achieve a high PSR. It is, however, difficult to achieve a high loop gain with a low supply voltage. In addition, the circuit for the power noise cancellation mechanism increases the design complexity and consumes extra I_Q [2]. The concept of resources sharing power noise cancellation mechanism as shown in Fig. 1 is thus proposed. The first stage (stage 1_EATA) of the EA attenuates the power noise, whereas the second stage (stage 2_EA) of the EA rejects the common mode noise (v_{icm}) at its inputs, and creates a replica of the supply noise at the output. The stage 1_EATA is shared by the EA and TA, saving the cost and I_Q .

D. Small Area

In a low-voltage LDO regulator design, several performance enhancing auxiliary circuits and a large M_P occupy consider-able space. A wide output swing EA can reduce the size of the M_P . To support a wide load current range (e.g., 0–100 mA) and a wide output-voltage range (e.g., 0.5–0.85 V), the M_P may enter the triode region when under a heavy load condition (large V_{SG}) with a low-dropout voltage (small V_{SD}). The M_P should, therefore, be large enough to make the intrinsic gain of the M_P close to one at the triode region and maintain a high loop gain in the LDO regulator. Similarly, the LDO regulator can respond to the load current transient in time for such a wide range of operating conditions.

E. Stability

The dominant pole for an off-chip capacitor (e.g., C_L = 1 μF) compensated LDO regulator, exists at the output node (p_O in Fig. 1). As a large M_P contributes the first nondominant pole (p_g) at a relative low frequency, a large equivalent series resistance of C_L (R_{esr}) is required to generate a low frequency zero (z_{esr}) to cancel p_g. Therefore, large output variations during the load transient are induced by the large R_{esr}. A wide output swing EA can reduce the size of the M_P implying that such pole-zero cancellation is taking place at a higher frequency with a related small R_{esr}. Therefore, a smaller output variation during the load transient can be achieved. The second nondominant pole (p_x) should be placed at a high frequency further, which implies a low resistance or low capacitance path at node V_X .

III. Circuit Realization and Simulation Results

To achieve the required goals of compact and low-voltage operation while achieving a fast transient response, low I_Q and high PSR, four aspects of the proposed LDO regulator are optimized. The circuit schematic is shown in Fig. 2. We first apply the simple symmetric OTA as the EA, composed of ^{M}EA1–^{M}EA9, where ^{g}mi|i = 1–9, ^{r}Oi|i = 1–9, and λi|i = 1–9 ^{rep}resent the corresponding transconductance, output resistance, and the channel length modulation coefficients, respectively. The OTA-type EA requires no compensation capacitor, and operates at a minimum supply voltage ($V_{DD,min}$) equal to one threshold voltage plus twice the overdrive voltage ($V_{DD,min}$ = V_T + 2 × V_{OV}). Thus, the EA can operate with a low supply voltage (≤1 V). The symmetric structure of the EA also has a low input offset voltage for the regulator to achieve an accurate output. Furthermore, the impedances at node v_x and v_y are low, LDO act as a variable resistor that is placed between input power source and the load in order to drop and

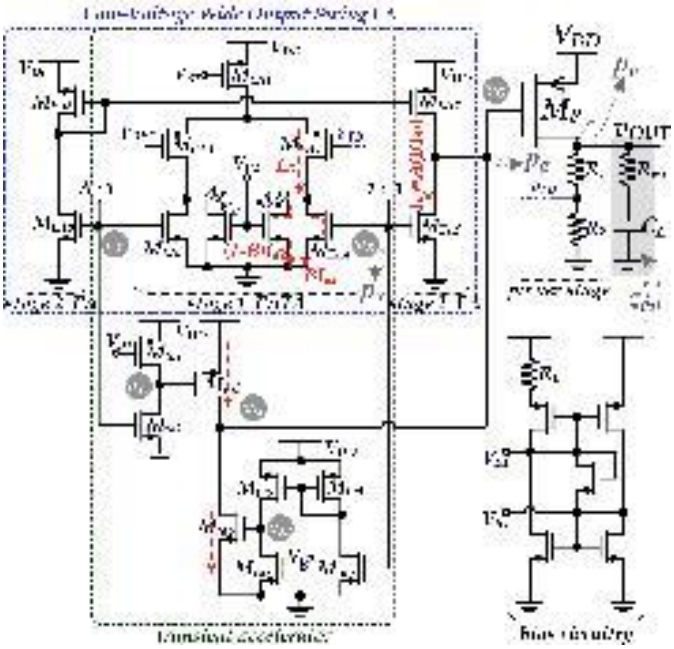

Fig. 2. Circuit schematic of the proposed LDO regulator.

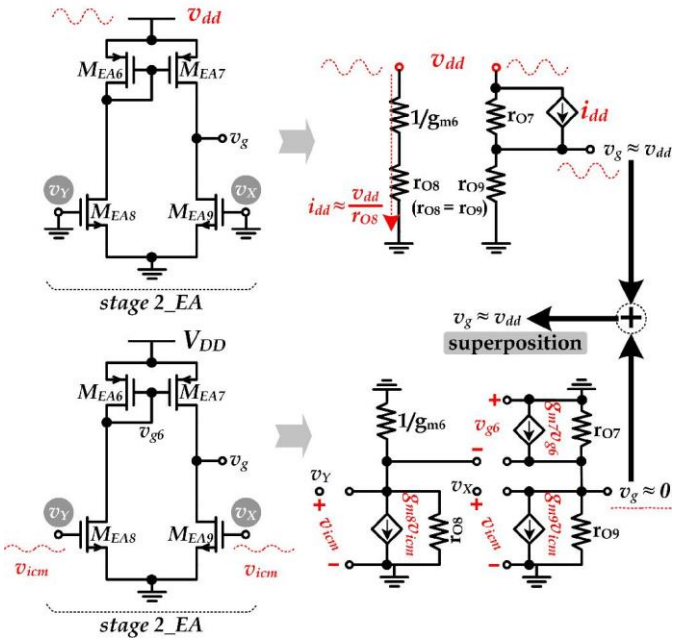

Fig. 3. Low-frequency, small-signal model of the EA output stage for ripple cancellation analysis.

enough to push the nondominant pole (p_X) to a sufficient high frequency so as not to affect the system stability.

The EA achieves a rail-to-rail output swing at node v_G by the output stage therefore, the size of the M_P can be minimized for a specific load current requirement. Reducing the size of the M_P significantly reduces the circuit area and contributes to a smaller gate capacitance. This allows the EA to drive the M_P by a large enough slew rate with a relatively low biasing current. The gain of the EA (A_{EAO}) is

where we assume (r_{O7} _ r_{O9}) and let {I_{d2}, V_{OV2}, A} represent the bias current, overdrive voltage of M_{EA2}, and current ratio between the first and second stages of the EA, respectively. The A_{EAO} in (1) is too low to achieve a fast transient response and high PSR. Therefore, we apply the current splitting technique [12] to boost the gain by maintaining g_{m2} and increasing r_{O9}. The transistors M_{gb1} and M_{gb2} can reduce the bias current being mirrored to the second stage of the EA. Thus, the gain of the modified EA (A_{EAM}) is boosted by a factor of 1/B as follows:

$$A_{EAM} \approx g_{m2} \times A \times r_{O9}$$

where B is the current splitting ratio and is <1.

A p-type device is chosen to construct the power MOS transistor M_P , because of the low supply voltage and low-dropout voltage requirements. The gain-boosted OTA-based EA improves the loop gain of the LDO regulator, which in turn enhances the PSR performance. In addition, we create a replica of the power noise at the gate terminal of the M_P to cancel out the power noise at the source terminal of M_P . This further improves the PSR performance. To reduce the area and I_Q , we use the existing EA to replicate the power noise instead of using an auxiliary circuit. The two equivalent resistors between the output nodes (v_X and v_Y) of the first stage of the EA (stage 1_EATA) and the ground have a low resistance value (1/g_{m4} and 1/g_{m5}); therefore, the power supply noise of stage 1_EATA can be attenuated at nodes v_X and v_Y. Only a small level of power supply noise can be coupled to nodes v_X and v_Y, as they appear in the form of a common mode input (v_{icm} in Fig. 3) to the output stage of the EA (stage 2_EA). This is due to the symmetric structure of stage 1_EATA. The common mode gain of stage 2_EA can be derived using the low-frequency small-signal model, shown at the bottom of Fig. 3, with an assumption of (r_{O6} _ 1/g_{m6}). We first assume that the power noise is propagated by stage 1_EATA through the common mode signal v_{icm} and causes a fluctuation on v_{g6}. The output v_g induced by v_{icm} is, therefore, given by

$$v_g = -g_{m7} v_{g6} - g_{m9} v_{icm} \cdot (r_{O7} \| r_{O9})$$

An LDO voltage regulator is just a DC linear voltage regulator which can be operated with a very small input-output voltage differential. This input output voltage differential is called dropout voltage. In simple words dropout voltage is the voltage dropped by the regulator circuitry alone for its working. For example, an LM2941 LDO voltage regulator has a dropout voltage of only around 0.5V, which means that in order to get 5 volts at the output you need to input only 5.5 volts where an ordinary 7805 linear voltage regulator has a dropout voltage of around 2V. This means that, in order to get 5V at the output of 7805 you need to input at least 7V. As I said above the working of a LDO voltage regulator is similar to the working of an ordinary linear voltage regulator and the only difference is in the schematic topology of their internal circuitry.

where we assume that M_{EA8} and M_{EA9} are matched devices ($g_{m8} = g_{m9}$), ($r_{O8} \_ 1/g_{m6}$), and ($g_{m6} \approx g_{m7}$). To cause g_{m6} to be close to g_{m7}, the channel length of M_{EA6} and M_{EA7} are selected to be five times the minimum length to reduce the effect of channel-length modulation. Then, we ground both the nodes v_x and v_y and input the power noise from the power supply (V_{DD}). The small-signal model shown at the top of Fig. 3 is used to show how the power noise is replicated to v_g. The result is given by the following:

Application of the superposition theorem by summing (3) and (4), we see that almost the entire power supply noise is replicated to the gate terminal of M_P (v_g). As the frequency of the power noise increases, the small-signal model shown in Fig. 3 is no longer valid as the equivalent impedance of the parasitic capacitance of M_P (C_{gs}/C_{gd}) becomes finite and can no longer be ignored. As C_{gs}/C_{gd} equals 1.4/0.5 pF in our design, the PSR is expected to fall when the frequency of the power noise goes >100 kHz.

The first stage of the EA and M_{ta1}–M_{ta8} constitutes the TA that reduces the slew time of the gate terminal of M_P by increasing the dynamic discharging/charging current during the load transient. The first stage of the EA is reused as a part of the output variation detector of the TA to reduce the circuit complexity. Furthermore, to avoid a significant increase in I_Q and to avoid the breaking of perfect replication of the power noise at the gate terminal of M_P, M_{ta3}, and M_{ta8} are biased at the cutoff region in the steady state. A large load change causes a variation in both the output voltage (v_{OUT}) and feedback voltage (v_{FB}).

The proposed LDO regulator shown in Fig. 2 has three poles (*p*o, *p*x, and *p*g) and one zero (zesr), and the simulated frequency response of the loop gain for different load currents (*I*OUT = 1 and 100 mA), output voltage (*V*OUT = 0.5 and 0.85 V), and *R*esr (1) conditions, are shown in Fig. 4. The dominant pole is *p*o (100–10 kHz) due to the large off-chip compensation capacitor *CL* (1 μF). The second dominant pole

(*p*g) is located at a relatively high frequency (~100 kHz) as the wide output swing of the EA reduces the size of the *MP* . Thus,*p*g can be easily cancelled by the zero (zesr) with a *R*esr of 1 . The third pole (*p*x) is far beyond the UGF because of the simple architecture of the OTA-based EA, and therefore does not affect the stability. Fig. 4 guarantees the stability of the proposed LDO regulator for a wide range of operating conditions.

The basic performances of CMOS linear regulators include output voltage accuracy, supply current, line regulation, load regulation, dropout voltage, and output voltage temperature characteristics. Because these parameters are fundamental characteristics of series regulators, there is no major difference between CMOS regulators and bipolar linear regulators.

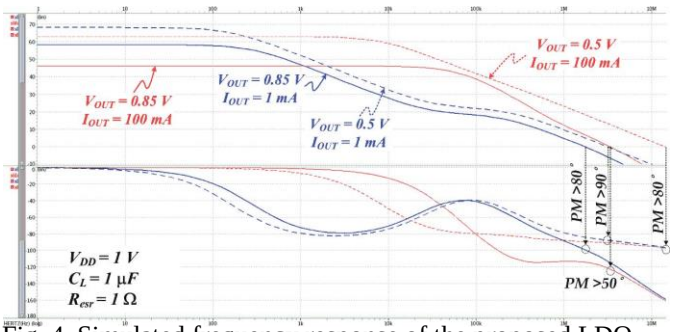

Fig. 4. Simulated frequency response of the proposed LDO regulator for load currents of (1 mA, 100 mA) and output voltages (0.5 V, 0.85 V). R_{esr} = 1 _.

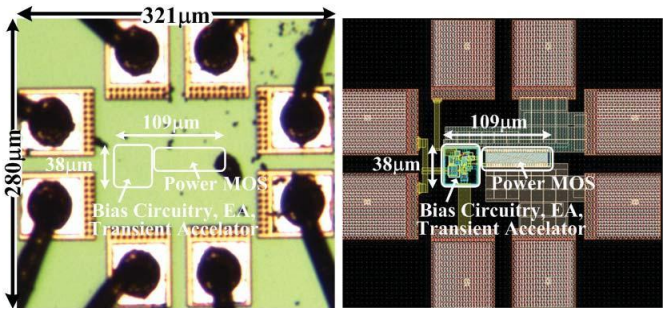

Fig. 5. Die micrograph (left) and layout (right) of the proposed LDO regulator.

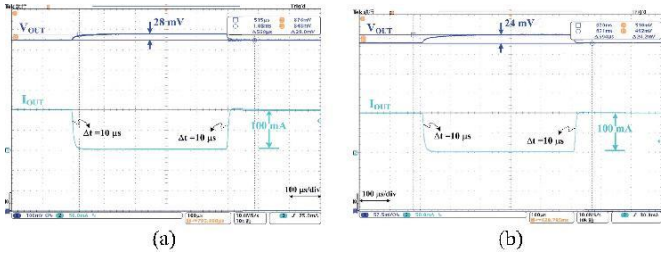

Fig. 6. Measured load transient response (I_{OUT} = 100–0 mA) for different V_{DD}/V_{OUT}. (a) 1.0/0.85 V, (b) 1.0/0.5 V. C_L = 1 μF, and R_{esr} = 1 _.

IV. EXPERIMENTAL RESULTS AND THE PERFORMANCE EVALUATIONS

The proposed LDO regulator is fabricated using a 90-nmCMOS process. The die micrograph and layout are shown in Fig. 5. The core area is only 0.0041 mm2 and the maximum load current is 100 mA. The input voltage is 1 V and the values of*R*1 and *R*2 can be adjusted to generate any regulated output level between 0.85 and 0.5 V. The maximum *IQ* is 60 μA, achieving a 99.94% current efficiency. The *CL* used for measurement is 1 μF with a *R*esr of 1 . Fig. 6 shows the measured waveforms of the load transient test where the load

TABLE I

PERFORMANCE EVALUATIONS

Design Parameters	[4] 2007	[5] 2008	[6] 2008	[7] 2010	[8] 2011	[9] 2011	This Work 2012	
Technology (CMOS)	0.35μm	0.35μm	0.35μm	0.5μm	0.18μm	0.35μm	90 nm	
V_{DD} /V_{OUT} (V)	2/1.8	1.05/0.9	2/1.8	1.4/1.21	2.1/1.8	3.3/3	1/0.85	1/0.5
Load capacitor C_L (μF)	1	1	1	0.1	1	1	1	
R_{ESR} ( )	n.a.	n.a.	n.a.	n.a.	0.2	n.a.	1	
Maximum I_Q (μA)	340	164	27	45	150	350	60	
Maximum I_{OUT} (mA)	200	50	150	100	150	100	100	
Current efficiency (%)	99.83	99.67	99.97	99.95	99.9	99.65	99.94	
Load regulation (mV/mA)	0.17	0.0614	n.a.	0.25	>0.3	>0.75	0.28	0.24
Output variation V_{OUT} (mV) @(I_{OUT1}–I_{OUT2} in mA)	54 (1–200)	6.6 (0–50)	>135 (0–100)	120 (0–100)	38 (0–100)	<150 (0–100)	28 (0–100)	24 (0–100)
Response time TR(μs)*	0.27	0.132	1.35	0.12	0.38	1.5	0.28	0.24
PSR@100 kHz (dB)	>45**	>50	>40**	n.a.	n.a.	n.a.	48.1	>50
Area (mm^2)	0.264	0.053	0.409	0.263	0.104	n.a.	0.0041	
FOM1*	0.459	0.432	0.243	0.054	0.38	5.25	0.168	0.144
FOM2#	0.1212	0.0229	0.0994	0.0142	0.0395	n.a.	0.00069	0.00059

Note: * Adopted from [3], ** 0–20 kHz, # FOM2 = FOM1 × area.

Fig. 7. Measured PSR performance. (V_{DD}/V_{OUT}/I_{OUT} = 1 V/0.85 V/ 50 mA).

current is switched between 0 and 100 mA within 10 μs. The input/output voltage V_{DD} and V_{OUT} is set to {1 V, 0.85 V} and {1 V, 0.5 V}, respectively. The output variations during load transient (V_{OUT}) are measured to be only 28 and 24 mV for V_{OUT} equal to 0.85 and 0.5 V, respectively. The rise/fall time (10 μs) of the load current transient is restricted by the limitation of our measurement instrument (Chroma Electronic Load System 6300 Series). The ac capability of the proposed LDO regulator is, therefore, not tested to its best condition and the resulting small output variations are from enough dc loop gain. As the output variation of 28 mV is far less than the value of (100 mA × R_{esr}), we can, however, speculate that the response time of the LDO regulator test chip is far <10 μs. The PSR performance is also measured when the test conditions are V_{DD} = 1 V, V_{OUT} = 0.85 V, and I_{OUT} = 50 mA; the measured result is shown in Fig. 7. The proposed LDO regulator achieves a PSR ~50 dB at low frequencies whereas the rolloff frequency is ~100 kHz. Table I lists the performance comparisons between the proposed LDO regulator and several previous papers. Although the consumed I_Q is larger than the design in [6], the proposed LDO regulator benefits from superior performance in output variations. In contrast, [5] produced the smallest output variation (0–50 mA), yet consumed a significant I_Q . To fairly evaluate the performance of the load transient response, the frequently used figure of merit (FOM1) proposed in [3] was adopted to include the dependence of the output capacitance. The design in [7] had a better FOM1 than the proposed design; however, it did not show the dominant ESR effects of output variation during the load transient. Further, [7] was unable to operate below 1-V input voltage, and does not report the PSR performance. We also use FOM2 that is (FOM1 × area) to show the area efficiency further. In summary, the proposed LDO regulator is compact in size, and achieves a high PSR, fast transient response, and high current efficiency for low-voltage operation.

inV. CONCLUSION

This paper presented an LDO regulator using a simple OTA-type EA plus an adaptive transient accelerator, which can achieve operation below 1 V, fast transient response, low I_Q , and high PSR under a wide range of operating conditions. The proposed LDO regulator was designed and fabricated using a 90-nm CMOS process to convert an input of 1 V to an output of 0.85–0.5 V, while achieving a PSR of ~50 dB with a 0–100-kHz frequency range. In addition, a 28-mV maximum output variation for a 0–100-mA load transient, and a 99.94% Current efficiency was achieved. The experimental results verified the feasibility of the proposed LDO regulator.

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