A New Approach Of Fault Current Mitigation By Using Dynamic Voltage Restorer

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***Abstract*— This paper introduces and evaluates an auxiliary con-trol strategy for downstream fault current interruption in a radial distribution line by means of a dynamic voltage restorer (DVR). The proposed controller supplements the voltage-sag compensation control of the DVR. It does not require phase-locked loop and independently controls the magnitude and phase angle of the injected voltage for each phase. Fast least error squares digital filters are used to estimate the magnitude and phase of the measured voltages and effectively reduce the impacts of noise, harmonics, and disturbances on the estimated phasor parameters, and this enables effective fault current interrupting even under arcing fault conditions. The results of the simulation studies performed in the PSCAD/EMTDC software environment indicate that the proposed control scheme: 1) can limit the fault current to less than the nominal load current and restore the point of common coupling voltage within 10 ms; 2) can interrupt the fault current in less than two cycles; 3) limits the dc-link voltage rise and, thus, has no restrictions on the duration of fault current interruption; 4) performs satisfactorily even under arcing fault conditions; and 5) can interrupt the fault current under low dc-link voltage conditions.**

***Index Terms*—Digital filters, dynamic voltage restorer (DVR), fault current interrupting, and multiloop control.**

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I. INTRODUCTION

The voltage restorer (DVR) is a custom power device utilized to counteract voltage sags [1], [2]. It injects controlled three-phase ac voltages in series with the supply voltage, subsequent to a voltage sag, to enhance voltage quality by adjusting the voltage magnitude, wave shape, and phase angle [3]–[6]. Fig. 1 shows the main components of a DVR (i.e., a series transformer T, a voltage- source converter (VSC), a harmonic filter, a dc-side capacitor C_{DC}, and an energy storage de-vice [7], [8]). The line -side harmonic filter [5] consists of the leakage inductance of the series transformer L_f and the filter capacitor C_f.

The DVR is conventionally bypassed during a downstream fault to prevent potential adverse impacts on the fault and to protect the DVR components against the fault current [9]–[11]. A technically elaborate approach to more efficient utilization of the DVR is to equip it with additional controls and enable it

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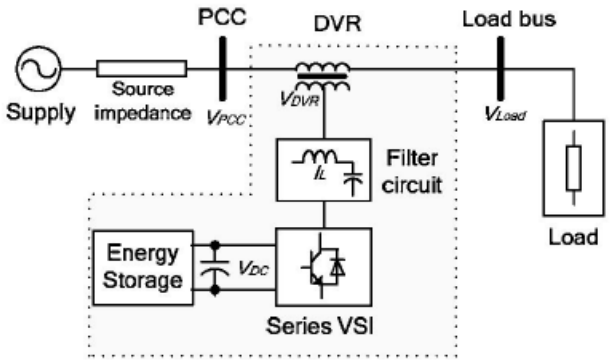

Fig. 1. Schematic diagram of a DVR with a line-side harmonic filter

also to limit or interrupt the downstream fault currents. A control approach to enable a DVR to serve as a fault current limiter is provided in [9]. The main drawback of this approach is that the dc- link voltage of the DVR increases due to real power absorption during fault current-limiting operation and necessitates a switch to bypass the DVR when the protective relays, depending on the fault conditions, do not rapidly clear the fault. The dc-link voltage increase can be mitigated at the cost of a slow-decaying dc fault current component using the methods introduced in [7] and [12].

To overcome the aforementioned limitations, this paper pro-poses an augmented control strategy for the DVR that provides: 1) voltage -sag compensation under balanced and unbalanced conditions and 2) a fault current interruption (FCI) function. The former function has been presented in [13] and the latter is described in this paper.

It should be noted that limiting the fault current by the DVR disables the main and the backup protection (e.g., the distance

and the over current relays). This can result in prolonging the fault duration. Thus, the DVR is preferred to reduce the fault current to zero and interrupt it and send a trip signal to the up-stream relay or the circuit breaker (CB).

It should be noted that the FCI function requires 100% voltage injection capability. Thus, the power ratings of the series transformer and the VSC would be about three times those of a conventional DVR with about 30%–40% voltage injection capability. This leads to a more expensive DVR system. Economic feasibility of such a DVR system depends on the importance of the sensitive load protected by the DVR and the cost of the DVR itself.

The performance of the proposed control scheme is evaluated through various simulation studies in the PSCAD/EMTDC platform. The study results indicate that the proposed control strategy: 1) limits the fault current to less than the nominal load current and restores the PCC voltage within less than 10 ms, and interrupts the fault current within two cycles; 2) it can be used in four- and three-wired distribution systems, and single-phase

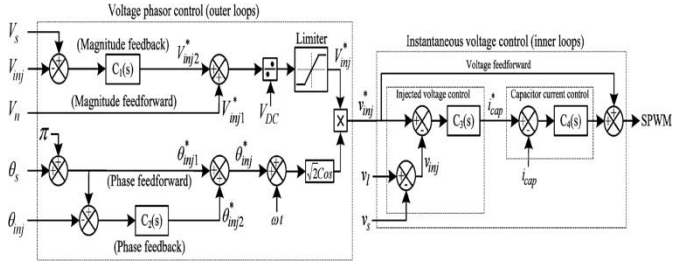

Fig. 2. Per-phase block diagram of the DVR control system in FCI mode.

configurations; 3) does not require phase-locked loops; 4) is not sensitive to noise, harmonics, and disturbances and provides effective fault current interruption even under arcing fault conditions; and 5) can interrupt the downstream fault current under low dc-link voltage conditions.

II. Proposed FCI Control Strategy

The adopted DVR converter is comprised of three indepen-dent H-bridge VSCs that are connected to a common dc -link capacitor. These VSCs are series connected to the supply grid, each through a single-phase transformer. The proposed FCI control system consists of three independent and identical controllers one for each single-phase VSC of the DVR.
Assume the fundamental frequency components of the supply voltage v_s, load voltage v_l, and the injected voltage V_{inj}

$$V_s = V_s\cos(\omega t+\Theta_s),$$
$$V_l = V_l\cos(\omega t+\Theta_l),$$
$$V_{inj} = V_l - V_s = V_{inj}*\cos(\omega t+\Theta_{inj}).$$

Two identical least error squares (LES) filters [14] are used to estimate the magnitudes and phase angles of the phasors

delay in the DVR response. Thus, a compromise between the voltage injection speed and disturbance attenuation is made. The designed LES filters utilize a data window length of 50 samples at the sampling rate of 10 kHz and, hence, estimate the voltage phasor parameters in 5ms. Fig. 3 depicts the frequency response of the LES filters and indicates significant attenuation of voltage noise, harmonics, and distortions at frequencies higher than 200 Hz and lower than 50 Hz. Reference [13] demonstrates the effectiveness of this filter in attenuating the noise, harmonics, and distortions for the sag compensation mode of operation as well. The next section shows that this filter also performs satisfactorily in the FCI operation mode, even under arcing fault conditions where the measured voltage and current signals are highly distorted.

Fig. 2 shows a per-phase block diagram of the proposed DVR control system corresponding to the FCI operation mode, where V_n is the nominal rms voltage. The control system of Fig. 2 utilizes Vs, V_l the dc-link voltage V_{dc}, and the harmonic filter capacitor current I_{cap} as the input signals. The reported studies in this paper are based on the over current fault detection method of of [7] and [12]. The fault detection mechanism for each phase is activated when the absolute value of the instantaneous current exceeds twice the load current. The proposed multiloop control corresponding to V_s and $V_{inj.}$

The FCI function requires a phasor parameter estimator (dig-ital filter) which attenuates the harmonic contents of the [3], [8], [9], [15]–[20] includes an outer control loop (voltage phasor control) and an inner control loop (instantaneous voltage control). The inner loop provides damping for the transients caused by the DVR harmonic filter [18] and [21], and improves the dynamic response and stability of the DVR. The inner loop is shared by the sag compensation and the FCI functions. When a downstream fault is detected, the outer loop controls the injected voltage magnitude and phase angle of the faulty phase(s) and reduces the load-side voltage to zero, to interrupt the fault current and restore the PCC voltage. The DVR "outer" voltage phasor control and "inner" instantaneous voltage control, corresponding to each phase, are described in the following two subsections.

A. Voltage Phasor Control System

In the FCI operation mode, the required injected voltage phasor is equal to the source voltage phasor, but in phase op-position [i.e., the injected phasor $V_{inj} = V^*_{inj} \angle\ \theta^*_{inj.}$ is controlled to be $V_s \angle\ (\theta_s+\pi)$] Performance of the voltage phasor control, in terms of transient response, speed, and steady-state error, is enhanced by independent control of voltage magnitude and phase, and incorporating feed forward signals to the feedback control system [17], [18], [21]–[27]. Fig. 2 shows two proportional-integral (PI) controllers (C_1 and C_2) that are used to eliminate the steady -state errors of the magnitude and phase of the injected voltage, respectively. Parameters of each controller are determined to achieve a fast response with zero steady-state error.

The output of the phasor control system is a reference phasor $V_{inj} = V^*_{inj} \angle\ \theta^*_{inj.}$ The output of the phasor control system is a reference phasor denoted by $V_{inj} = V^*_{inj} \angle\ \theta^*_{inj}$.

To eliminate the effects of the DC link voltage variations on the injected voltages, V^*_{inj} is normalized by V_{DC}. The magnitude and the phase angle of V^*_{inj} are independently calculated and the magnitude is passed through a limiter (Fig. 2). The resulting phasor magnitude and phase angle are converted to the sinusoidal signal V^*_{inj}, which is the reference signal for the instantaneous voltage control.

B. Instantaneous Voltage-Control System

Under ideal conditions, a voltage sag can be effectively compensated if the output of the phasor based controller V^*_{inj} is directly fed to the sinusoidal pulse width modulation (SPWM) unit. However, resonances of the harmonic filter cannot be eliminated under such conditions. Therefore, to improve the stability and dynamic response of the DVR, an instantaneous injected voltage controller and a harmonic filter capacitor current controller are used to attenuate resonances.

The generated reference signal for the injected voltage V^*_{inj} is compared with the measured injected voltage V_{inj}, and the error is fed to the voltage controller. As shown in Fig. 2, the output of the voltage controller i^*_{cap} is the reference signal for the filter capacitor current control loop. It is compared with the measured capacitor current $i_{cap,}$ and the error is fed to the current controller.

The steady-state error of the proposed control system is fully eliminated by the PI controllers in the outer control loop (i.e., C_1 and C_2), which track dc signals (magnitude and phase angle). Therefore, there is no need for higher order controllers in the inner control loop which are designed based on sinusoidal references. Thus, in Fig. 2, C_3 and C_4 are pure gains K_v and k_c, respectively.

A large k_v results in amplification of the DVR filter resonance and can adversely impact the system stability [18]. Thus, the transient response of the DVR is enhanced by a feedforward loop, and a small proportional gain is utilized as the voltage controller. A large k damps the harmonic filter resonance more effectively, but it is limited by practical considerations (e.g., amplification of capacitor current noise, measurement noise, and dc offset [18]). Therefore, the lowest value of the proportional gain which can effectively damp the resonances is utilized. The output of the current controller is added to the feedforward voltage to derive the signal for the PWM generator.

III. Study Results

Fig. 4 depicts a single- line diagram of a power system which is used to evaluate the performance of the proposed DVR control system under different fault scenarios, in the PSCAD/EMTDC software environment. A 525 kVA DVR system is installed on the 0.4-kV feeder, to protect a 500-kVA, 0.90 lagging power factor load against voltage sags. Parameters of the simulated power system and the DVR are given in Appendix A. In the reported studies, the base voltage for per-unit values is the nominal phase voltage.

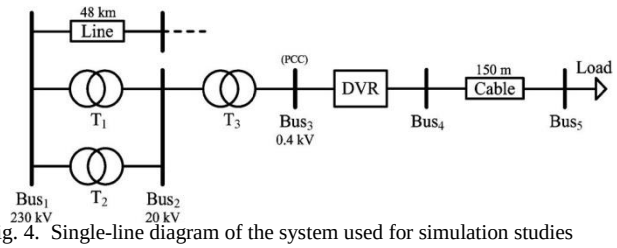

Fig. 4. Single-line diagram of the system used for simulation studies

IV. SIMULATION RESULTS

The presented simulation results have been obtained by using Matlab Simulink power system toolbox software. For the purpose of simulation a three phases 13.8KV, 50Hz ac supply has been considered. The proposed DVR with closed loop control has been simulated under three types of faults like L-G, L-L-G, and Three phase faults. The basic simulink block diagram is shown in Fig.5

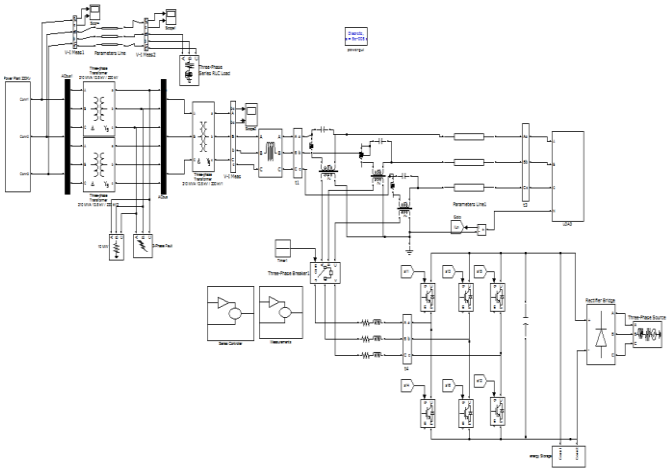

Fig. 5. Simulink model of DVR

The controlling of injected voltage by the DVR is done by using the series controller which is shown in below Fig.6.The series controller will controls the magnitude & phase angle of injected voltage independently to compensate the load voltage.The series controller will utilizes the four PI controllers to boost up the performance of the system.

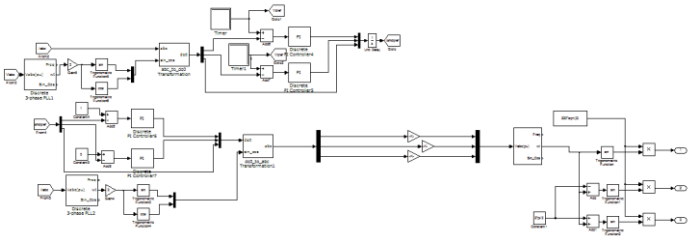

Fig.6. Control model of DVR

A. Three-Phase Downstream Fault

The system is subjected to a three- phase short circuit with a negligible fault resistance at $t=$ 20 ms at Bus_5 . Prior to the fault inception, the DVR is inactive (in standby mode) (i.e., the primary windings of the series transformers are shorted by the DVR). During the fault if the DVR is bypassed, the voltage at Bus3 drops to 0.77 p.u. and the fault current increases to about 17 times the rated load current

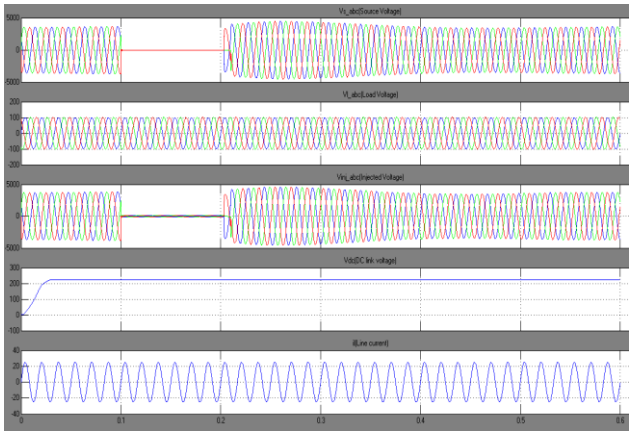

Fig.7. (a) Injected voltages. (b) Source voltages. (c) Load voltages. (d) dc link voltage. (e) Line current, during the three-phase downstream fault.

Fig. 7 shows FCI performance of the proposed DVR control system during the fault. Fig. 7(a)–(c), respectively, shows the three-phase injected voltages, the restored three-phase supply-side voltages, and the three-phase load -side voltages which are reduced to zero to interrupt the fault currents. The slightly injected voltage by the DVR before the fault initiation [Fig. 7(a)] is the voltage drop across the series impedance of the DVR series transformer secondary winding.

Fig. 7(d) shows the line currents (i.e., the currents passing through the DVR). Fig. 7(d) illustrates that the proposed FCI method limits the maximum fault current to about 2.5 times the nominal value of the load current and interrupts the fault cur-rents in less than 2 cycles. Fig. 7(e) depicts variations of the dc-link voltage during the FCI operation, and indicates that the dc-link voltage rise under the worst case (i.e., a severe three-phase fault) is about 15% and occurs during the first 5 ms after fault inception.

B. Phase-to-Phase Downstream Faults

The system of Fig. 8 is subjected to a phase-A to phase-C fault with the resistance of 0.05 Ω at 10% of the cable length connecting Bus_4 to Bus_5 , at $t=$ 20 ms. When the DVR is inactive (bypassed) during the fault (Fig. 8), the PCC voltage drops to 0.88 p.u., and the fault current increases to about 11 times the rated load current.

Fig. 8 illustrates that when the DVR is in service, the pro-posed FCI control successfully interrupts the fault current and restores the PCC voltage of the faulty phases within two cycles. Fig. 8(e) shows that the dc -link voltage rise is less

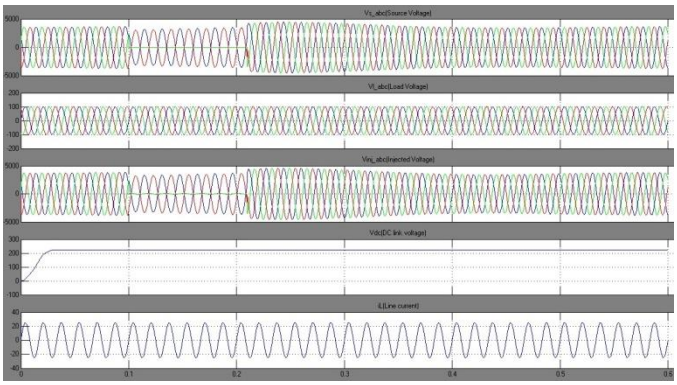

Fig.8. (a) Injected voltages. (b) Source voltages. (c) Load voltages. (d) dc link voltage. (e) Line current, during the three-phase downstream fault.

than 7%. Fig. 8 also shows that only the two faulty phases of the DVR react, and the healthy phase is not interrupted.

C. Single-Phase-to-Ground Downstream Fault

Phase-A of the system of Fig. 9 is subjected to a fault with the resistance of 0.2 Ω at 10% length of the cable connecting Bus_4 to Bus_5 , at $t=$ 20 ms. If the DVR is inactive (Fig. 9), the PCC voltage does not considerably drop and the fault current is about 2.5 p.u. It must be noted that although the PCC voltage drop is not considerable, the fault current must be interrupted by the DVR to prevent possible damages to the VSC before the fault is interrupted by the relays. The reason is that the operation time of the overcurrent relays is considerable for a fault current of about 2.5 p.u.

Fig. 9 illustrates that the proposed DVR control strategy successfully interrupts the fault current in the faulty phase in about two cycles. Fig. 9(e) shows that the dc-link voltage rises less than 1.8%. Fig. 9 shows that only the faulty phase of the DVR reacts to fault current, and the healthy phases are not interrupted. Simulation studies conclude that the dc-link voltage rise caused by the proposed FCI mode of operation is proportional to the fault current, and depends on the type of fault. The results also indicate that the maximum dc-link voltage rise occurs under the most severe three-phase fault which is about 15%, and can be tolerated based on DVR appropriate design.

It must be noted that to prevent operation of three -phase in-duction motors under unbalanced voltage conditions, they must be equipped with protective devices which detect such condi-tions and disconnect the load when any of the phases is de-en-ergized by the single-phase operation of the FCI function. Fur-thermore, disabling the single-phase fault current interruption capability can be provided as an operational option and the operator can be decide either to use or disable this function depending on the type of the load.

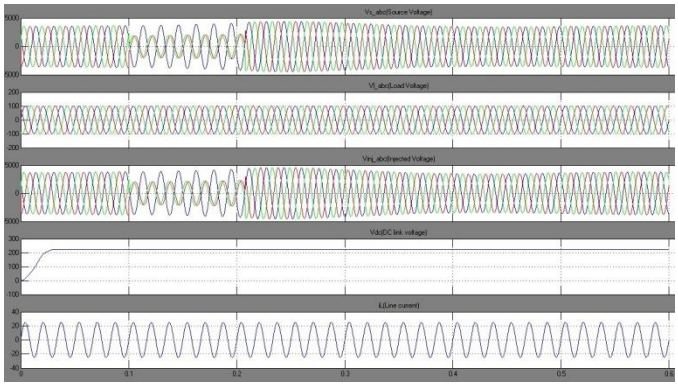

Fig.9. (a) Injected voltages. (b) Source voltages. (c) Load voltages. (d) dc link voltage. (e) Line current, during the three-phase downstream fault.

D. Simultaneous FCI Operation and Sag Compensation

The proposed DVR control system performs two different functions (i.e., sag compensation and FCI). Thus, the mutual effects of these modes on each other must be evaluated. At t= 15 ms, the system of Fig. 4 is subjected to a phase-A to phase-B fault with the resistance of 1Ω at 90% of the line length from Bus_1. The fault causes 87% voltage sag at the PCC. At t= 55ms, another fault with the resistance of 0.2Ω on phase A at 10% length of the cable connecting Bus_4 to Bus_5 occurs. The upstream fault is cleared by relays at t=93 ms.

Fig. 9 shows the performance of the proposed DVR control system under the aforementioned conditions (i.e., simultaneous FCI operation and sag compensation). Fig. 9 shows that when the downstream fault occurs in phase- A, the operation mode of the DVR in phase- A changes from sag compensation to FCI operation. However, the DVR continues to compensate the sag in phase-B to restore the load voltage in this phase. Consequently, phase -A and phase-B of the DVR operate in sag compensation mode during 15<t<55 ms. During 55<t<93 ms, phase-A is in FCI operation mode, and phase-B continues to compensate the sag. During t>93 ms , phase-B is in standby mode since the upstream fault is cleared and phase-A continues to interrupt the downstream fault current. During the entire process, phase-C is in standby mode.

Fig. 9(d) depicts variations of the dc-link voltage and indicates that the dc-link voltage drops during sag compensation, but the FCI operation maintains the dc-link voltage when it is lower than a certain value (the dc-link voltage, which is needed to reduce the load voltage to zero). This continues until the capacitor voltage approaches the aforementioned threshold. The reason is that when the capacitor voltage is lower than a certain value, the magnitude of the voltage injected by the DVR, which must be 180^0 out of phase with respect to the source voltage, is less than the source voltage magnitude. Thus, small current flows through the DVR until the capacitor is charged. This cur-rent results in active power absorption by the DVR.

Fig. 10 shows the effect of lower initial dc-link voltage on the FCI operation during a phase-A to ground fault with the resistance of 0.05 Ω at 10% length of the cable connecting Bus_4 to Bus_5 at t= 15 ms. If the DVR is inactive (bypassed) during the fault, the fault current increases to about 7 times the rated load current. Fig. 10 shows that even under very low dc-link voltage conditions, the FCI control limits the fault current to less than the nominal load current in about one cycle. Fig. 10

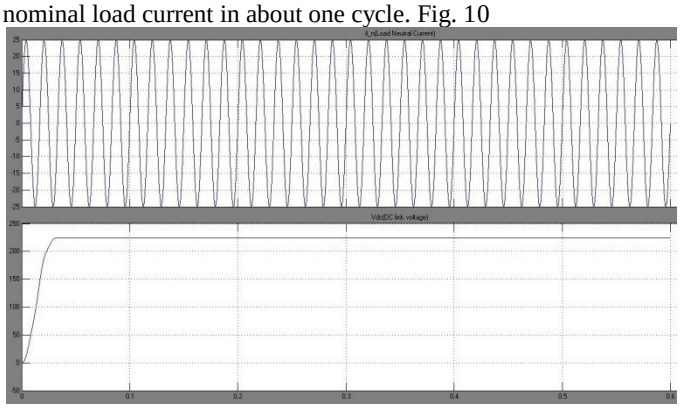

Fig.10 Line current of phase-A and dc-link voltage, for different initial values of the dc-link voltage, during downstream phase-A-to-ground fault.

shows that regardless of the initial dc-link voltage, the dc-link capacitor is charged up to a voltage which is adequate to inject a voltage equal to the supply voltage and fully interrupt the fault current.

V. CONCLUSION

This paper introduces an auxiliary control mechanism to enable the DVR to interrupt downstream fault currents in a radial distribution feeder. This control function is an addition to the voltage- sag compensation control of the DVR. The performance of the proposed controller, under different fault scenarios, including arcing fault conditions, is investigated based on time-domain simulation studies in the PSCAD/EMTDC environment. The study results conclude that

- The proposed multiloop control system provides a desirable transient response and steady-state performance and effectively damps the potential resonant oscillations caused by the DVR LC harmonic filter.
- The proposed control system detects and effectively interrupts the various downstream fault currents within two cycles (of 50 Hz).
- The proposed fault current interruption strategy limits the DVR dc link voltage raise caused by active power absorption, to less than 15% and enables the DVR to restore the PCC voltage without interruption; in addition, it interrupts the downstream fault currents even under low dc-link voltage conditions.
- The proposed control system also performs satisfactorily under downstream arcing fault conditions.

APPENDIX A
DVR MODEL PARAMETERS

Parameters of the studied power system and the DVR are as follows.
Short circuit current at Bus_1:31.5 KA, X/R at Bus_1:5.67;
$\Omega = 2\pi * 50$ rad/sec ;
transmission line (48 km):
$R_{Line} = 1.876\Omega$, $L_{Line} = 0.0774$ H;

TABLE I
TRANSFORMER PARAMETERS

Transformer	T_1, T_2	T_3	T_s
Rated Power (MVA)	90	2	0.175
No load losses (p.u.)	0.001	0.00205	0.003
Copper losses (p.u.)	0.0048	0.0097	0.02
Leakage reactance (p.u.)	0.237	0.06	0.05
Primary voltage rating (kV)	230	20	0.4
Secondary voltage rating (kV)	20	0.4	0.245
Winding connection type	YnD	DYn	---

TABLE III
VSC PARAMETERS

Parameter	Value
Switching frequency (unipolar SPWM)	3 kHz
DC-link rated voltage	560 V
DC-link capacitor	100 mF
Harmonic filter capacitor C_f	300 μF
Harmonic filter inductor L_f (leakage inductance of T_s)	56.82 μH

cable (150 m):
$R_{Cable} = 9.6$ mΩ, $L_{Cable} = 340$ mH.
Parameters of the step-down transformers T_1, T_2 and T_3, and the DVR series transformers T_S are given in table I.
Parameters of the VSC are given in table II.

In FCI operation mode, each single-phase series transformer should be able to inject 1-p.u. line-to- neutral voltage (231 V). Taking into account the voltage drop across its series branch impedance under the nominal load current of 721 A and the safety margin needed to prevent over modulation during transients, the secondary voltage rating of the series transformer is chosen to be 245 V. Therefore the power rating of T_S is 245 V* 721 A = 175 KVA, and the rating f DVR is 3* 175 =525 KVA.
The controller transfer functions are as follows:

$$C_1(s) = k_{p1} + \frac{k_{I1}}{s}, \quad k_{p1} = 0.2, \quad k_{I1} = 100$$
$$C_2(s) = k_{p2} + \frac{k_{I2}}{s}, \quad k_{p2} = 0.1, \quad k_{I2} = 500$$
$$C_3(s) = k_v = 0.1$$
$$C_4(s) = k_c = 0.7.$$

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