A Cascaded H-Bridge and Novel Multilevel Inverter Topology for Induction Motor Drive

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***Abstract*— Present day drive types are the Induction motor drives with voltage source inverters. Also the voltage waveforms of traditional two level inverter fed Induction motor shows that the voltage across the motor contains not only the required "fundamental" sinusoidal components, but also pulses of voltage i.e. "ripple" voltage. Moreover the voltage waveforms produced by the inverter has sharp edges. The rate of change of voltage with respect to time i.e. dv/dt is very high at these edges, of the order of 500–5000 V/µs.The two-level inverter topology has attracted attention in low power low voltage drive applications where as Three- Level inverter topology has attracted attention in high power High performances voltage drive applications. Single-phase VSI cover low-range power applications and three-phase VSI cover the medium- to high-power applications. The Main purpose of these three level inverter topologies is to provide a three phase voltage source, where the amplitude, phase, and frequency of the voltages should always be controllable. Although most of the applications require sinusoidal voltage waveforms The benefits are especially clear for medium-voltage drives in industrial applications and are being considered for future naval ship propulsion systems. The application of pulse width-modulated (PWM) voltages using two-level high-voltage inverters to a squirrel-cage induction motor (SQIM) can cause heating of rotor shaft, voltage spike across the motor terminals, etc. The increase in the number of steps of the motor voltage and hence decreasing the *dv/dt* applied to the machine terminals can be a solution to this problem. The existing topologies that generate this multistep voltage include cascading of a number of single-phase inverters or use of higher order multilevel inverters. In this paper, a topology with series connection of three-phase three-level inverters is proposed, which addresses the problems of medium-voltage drives.**

Keywords*— Medium-voltage ac drives, multilevel converter topologies.

Introduction

Power electronic inverters are widely used in various industrial drive applications. To overcome the problems of the limited voltage and current ratings of power semiconductors devices, some kinds of series and/or parallel connections are necessary. Recently, the multilevel inverters have received more attention in literature due to their ability to synthesize waveforms with a better harmonic spectrum and to attain higher voltages. They are applied in

many industrial applications such as ac power supplies, static VAr compensators, and drive system, etc.

Multilevel inverters have very important development for high power medium voltage AC drives. Quite a lot of topologies have found industrial approval; Neutral Point Clamped, flying capacitor, H-bridge, cascaded with separated DC source, several control and modulation strategies have been developed Pulse Width Modulation (PWM), Sinusoidal PWM, Space Vector PWM and Selective harmonic eliminations etc.

One of the significant advantages of multilevel configuration is the harmonics reduction in the output waveform without increasing switching frequency or decreasing the inverter power output[2,3]. These multilevel inverters, in case of *m*-level, can increase the capacity by (*m*-1) times than that of two-level inverter through the series connection of power semiconductor devices without additional circuit to have uniform voltage sharing. Comparing with two level inverter system having the same capacity, multilevel inverters have the advantages that the harmonic components of line-to-line voltages fed to load, switching frequency of the devices and EMI problem could be decreased [1].

The output voltage waveform of a multilevel inverter is composed of a number of levels of voltages starting form three levels and reaching infinity depending upon the number of the dc sources. The main function of a multilevel inverter is to produce a desired ac voltage waveform from several levels of dc voltage sources. These dc voltages may or may not be equal to one another. These dc sources can be obtained from batteries, fuel cells, or solar cells. Conventionally, each phase of a cascaded multilevel converter requires '*n*' dc sources for 2*n* + 1 levels in applications that involve real power transfer. These dc sources are assumed to have identical amplitudes.

Similar voltage profiles can also be obtained by using higher order neutral-point-clamped (NPC) multilevel inverters or by cascading a number of two-level inverters. However, the multilevel NPC inverters suffer from dc-bus imbalance, device underutilization problems and unequal ratings of the clamped diodes, etc., which are not very serious problems for inverters with three levels or lower. The capacitor voltage imbalance for a five-level one is presented in which suggest the need of extra hardware in the form of dc choppers or a back-to-back connection of multilevel converters. The cascaded H-bridge topology suffers from the drawbacks of the usage of huge dc-bus capacitors and complex input transformers for isolated dc bus for each module. These drawbacks are addressed in the proposed topology. Furthermore, the power circuit is modular in structure, and hence, the number of modules to be connected in series depends on the power of the drive.

PROPOSED CONVERTER TOPOLOGY

The proposed general configuration of "*n*" number of three level inverters connected in series is shown in Fig. 1. Each inverter module is a three-phase NPC three-level inverter. At the output stage, transformers are used to have the series connection of three-level inverters, as shown in Fig. 1. If "*V*dc" is the dc-bus voltage of each inverter module, then "α" is the turns ratio of each transformer and "*n*" is the number of inverter modules then for sine PWM (SPWM) strategy; the motor rms phase voltage (*V*Ph_motor) can be expressed as follows

$$\text{rms of } V_{\text{Ph\_motor}} = \sqrt{3}\alpha m n \frac{V_{\text{dc}}}{2\sqrt{2}}$$

Where *m* is the modulation index of the inverter topology defined as follows

$$m = \frac{\text{peak of } V_{\text{ph\_inverter}}}{n\frac{V_{\text{dc}}}{2}}.$$

*V*ph_inverter is the total phase voltage reference of the inverter topology. For the given peak of *V*Ph_motor, peak of *V*ph_inverter can be computed as follows The generation of individual reference voltage signal of each inverter is discussed as follows.

$$\text{peak of } V_{\text{ph\_inverter}} = \frac{\text{peak of } V_{\text{ph\_motor}}}{\sqrt{3}\alpha}.$$

The generation of individual reference voltage signal of each inverter is discussed as follows. The gate pulses for each three-level inverter module can be derived using two carrier signals.

Thus, "*n*" numbers of such three-level inverter modules require "2*n*" number of carriers [10], [13]. The three-phase voltage reference signals are then compared with these carrier waves to produce the gate pulses for the inverters. For example, the carrier waves and the sinusoidal modulating voltage signal (SPWM technique) for *R* phase is shown in Fig. 2 for four series- connected three-level inverters. The carrier waves 1 and 1_ (Fig. 2) with *R*-phase voltage reference controls the inverter module 1. Similarly, 2 2_, 3–3_, and 4–4_ carrier waves with *R*-phase voltage reference generate the gate pulses for the three-level inverter modules 2, 3, and 4, respectively. Thus, each inverter module produces the voltage proportional to a part of the reference phase voltage signals. It is important to note that no two three-level inverter modules switch simultaneously. Thus, the maximum *dv/dt* rate of the output voltage of this topology is limited to that of a single three-level inverter module. The references of each inverter are shown in Fig. 3. The corresponding output line voltages of each inverter are shown in Fig. 4. The four windings, one from each transformer, are connected in series and produced the net *R*-phase voltage, as shown in Fig. 5 Similarly, the other two phase voltages are generated.

The line voltage spectra of individual inverters are shown in Fig. 4 for switching frequency of 2.5 kHz. These line voltages get added to produce the net phase voltage of the topology. The voltage spectra are expressed as a percentage of the maximum total fundamental (*V*peak) that can be produced by the topology.

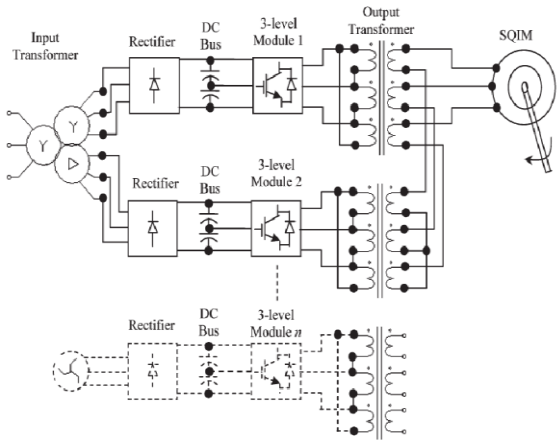


Figure.1 Block diagram of three-phase three-level inverter modules connected in series driving an SQIM.

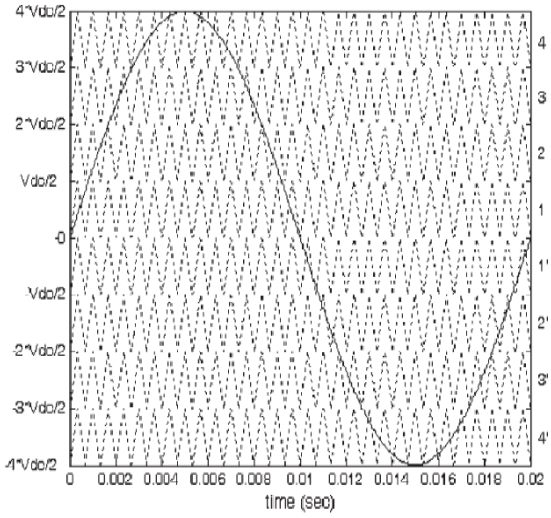


Figure.2 Carrier waves and the sinusoidal modulating voltage signal for *R* phase in SPWM technique

These spectra also suggest that the line voltages of all these inverters contain additional small amount of the 5^{th}, 7th-, 11th-, 13th-, and higher order harmonics besides the normal switching harmonics. However, the net phase voltage and line voltage of this topology do not contain any of these harmonics, as suggested by the spectra shown in Fig. 5. These harmonics get canceled when the line voltages of the individual inverters are added by the transformers to produce the net phase voltages. The increased number of steps in the motor terminal voltage reduces the *dv/dt* as that compared with a conventional two-level inverter.

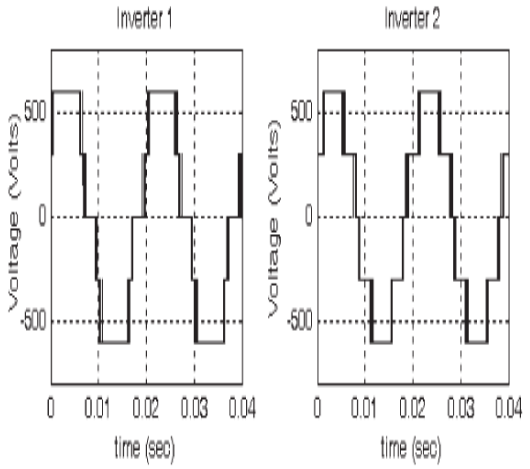


Figure.3: Four series connected Inverters Individual voltages

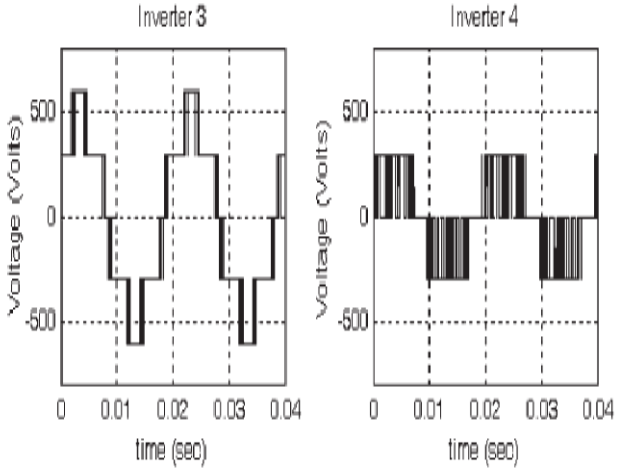


Figure.3: Four series connected Inverters Individual voltages

Dynamic model of Induction motor

The induction machine d-q or dynamic equivalent circuit is shown in Fig. 1 and 2. One of the most popular induction motor models derived from this equivalent circuit is Krause's model detailed in [5]. According to his model, the modeling equations in flux linkage form are as
follows:

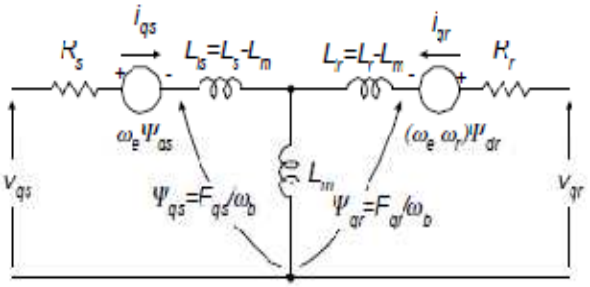


Figure. 4 Dynamic q-axis model

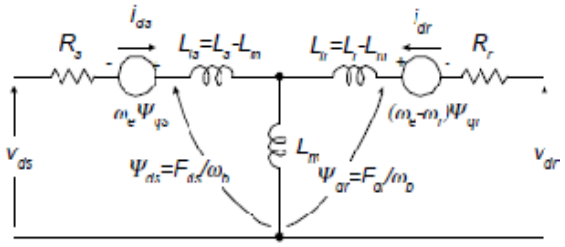


Figure. 5 Dynamic d-axis model

$$\frac{dF_{qs}}{dt}=\omega_b\left[v_{qs}-\frac{\omega_e}{\omega_b}F_{ds}+\frac{R_s}{X_{ls}}\left(F_{mq}+F_{qs}\right)\right] \quad (1)$$

$$\frac{dF_{ds}}{dt}=\omega_b\left[v_{ds}+\frac{\omega_e}{\omega_b}F_{qs}+\frac{R_s}{X_{ls}}\left(F_{md}+F_{ds}\right)\right] \quad (2)$$

$$\frac{dF_{qr}}{dt}=\omega_b\left[v_{qr}-\frac{(\omega_e-\omega_r)}{\omega_b}F_{dr}+\frac{R_r}{X_{lr}}\left(F_{mq}-F_{qr}\right)\right] \quad (3)$$

$$\frac{dF_{dr}}{dt}=\omega_b\left[v_{dr}+\frac{(\omega_e-\omega_r)}{\omega_b}F_{qr}+\frac{R_r}{X_{lr}}\left(F_{md}-F_{dr}\right)\right] \quad (4)$$

$$F_{mq}=X_{mi}^{*}\left[\frac{F_{qs}}{X_{ls}}+\frac{F_{qr}}{X_{lr}}\right] \quad (5)$$

$$F_{md}=X_{mi}^{*}\left[\frac{F_{ds}}{X_{ls}}+\frac{F_{dr}}{X_{lr}}\right] \quad (6)$$

$$i_{qs}=\frac{1}{X_{ls}}\left(F_{qs}-F_{mq}\right) \quad (7)$$

$$i_{ds}=\frac{1}{X_{ls}}\left(F_{ds}-F_{md}\right) \quad (8)$$

$$i_{qr}=\frac{1}{X_{lr}}\left(F_{qr}-F_{mq}\right) \quad (9)$$

$$i_{dr}=\frac{1}{X_{lr}}\left(F_{dr}-F_{md}\right) \quad (10)$$

$$T_e=\frac{3}{2}\left(\frac{p}{2}\right)\frac{1}{\omega_b}\left(F_{ds}i_{qs}-F_{qs}i_{ds}\right) \quad (11)$$

$$T_e-T_L=J\left(\frac{2}{p}\right)\frac{d\omega_r}{dt} \quad (12)$$

Voltage Source converter (VSC)

where d : direct axis,
q : quadrature axis,
s : stator variable,
r : rotor variable,
F_{ij} is the flux linkage (i=q or d and j=s or r),
v_{qs}, v_{ds} : q and d–axis stator voltages,
v_{qr}, v_{dr} : q and d–axis rotor voltages,
F_{mq},F_{md} : q and d axis magnetizing flux linkages,
Rr : rotor resistance,
Rs : stator resistance,
X_{ls} : stator leakage reactance ($\omega_e L_{ls}$),
X_{lr} : rotor leakage reactance ($\omega_e L_{lr}$),
X_{mi}^{*} : $1\Big/\left(\frac{1}{x_m}+\frac{1}{x_{ls}}+\frac{1}{x_{lr}}\right)$,
i_{qs}, i_{ds} : q and d–axis stator currents,
i_{qr}, i_{dr} : q and d–axis rotor currents,
p : number of poles,
J : moment of inertia,
T_e : electrical output torque,
T_L(or T_l) : load torque,
ω_e : stator angular electrical frequency,
ω_b : motor angular electrical base frequency,
ω_r : rotor angular electrical speed.

For a squirrel cage induction machine, as in the case of this paper, *vqr* and *vdr* in (3) and (4) are set to zero. An induction machine model can be represented with five differential equations as shown. To solve these equations, they have to be rearranged in the state-space form, In this case, state-space form can be achieved by inserting (5) and (6) in (1–4) and collecting the similar terms together so that each state derivative is a function of only other state variables and model inputs. Then, the modeling equations (1-4) of a squirrel cage induction motor in state-space become

$$\frac{dF_{qs}}{dt} = \omega_b \left[v_{qs} - \frac{\omega_e}{\omega_b} F_{ds} + \frac{R_s}{x_{ls}} \left(\frac{x^*_{ml}}{x_{lr}} F_{qr} + \left(\frac{x^*_{ml}}{x_{ls}} - 1 \right) F_{qs} \right) \right] \quad (13)$$

$$\frac{dF_{ds}}{dt} = \omega_b \left[v_{ds} + \frac{\omega_e}{\omega_b} F_{qs} + \frac{R_s}{x_{ls}} \left(\frac{x^*_{ml}}{x_{lr}} F_{dr} + \left(\frac{x^*_{ml}}{x_{ls}} - 1 \right) F_{ds} \right) \right] \quad (14)$$

$$\frac{dF_{qr}}{dt} = \omega_b \left[v_{qr} - \frac{(\omega_e - \omega_r)}{\omega_b} F_{dr} + \frac{R_r}{x_{lr}} \left(\frac{x^*_{ml}}{x_{ls}} F_{qs} + \left(\frac{x^*_{ml}}{x_{lr}} - 1 \right) F_{qr} \right) \right] \quad (15)$$

$$\frac{dF_{dr}}{dt} = \omega_b \left[v_{dr} + \frac{(\omega_e - \omega_r)}{\omega_b} F_{qr} + \frac{R_r}{x_{lr}} \left(\frac{x^*_{ml}}{x_{ls}} F_{ds} + \left(\frac{x^*_{ml}}{x_{lr}} - 1 \right) F_{dr} \right) \right] \quad (16)$$

MATLAB/SIMULINK MODEL & SIMULATION RESULTS

Here simulation is carried out for two cases. In case I conventional three phase three level induction motor is simulated and in case II proposed multilevel drive is simulated.

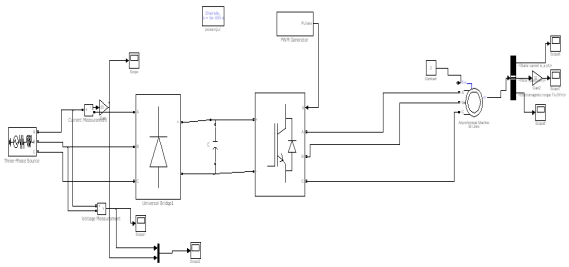


Fig. 6 Matlab/Simulink Model of Convention IM Drive

Fig. 6 shows the Matlab/Simulink model of conventional three phase three level induction motor drive. It consists of front end rectifier followed by three phase inverter.

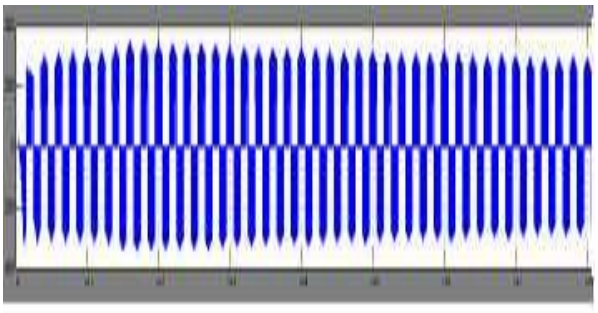


Fig. 7 Three Level output

Fig. 7 shows the three level output of the conventional inverter. Her switching frequency is taken as 1050 hz

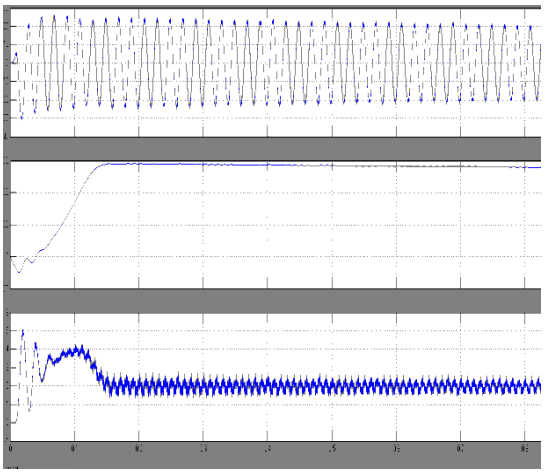


Fig.8 Stator Current, Speed and Motor Torque

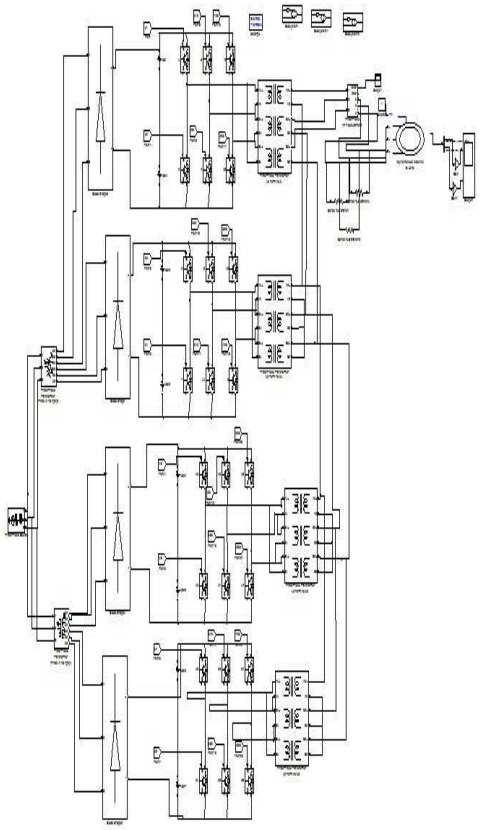


Figure.9 Block diagram of proposed circuit

Fig. 9 shows the block diagram of proposed series connected multilevel inverter fed induction motor drive. It consists of four inverters. Here we are using phase shifted carrier PWM.

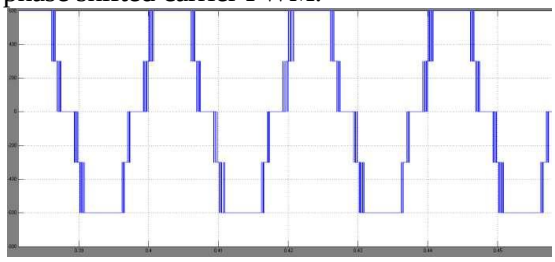


Fig. 10 Three Level output Inverter 1

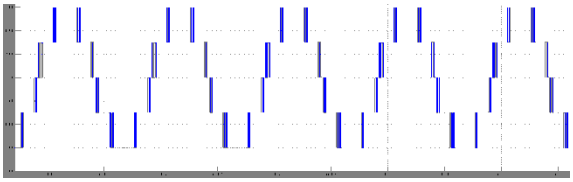


Fig. 11 Three Level output Inverter2

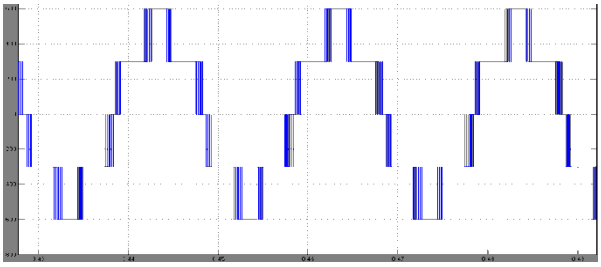


Fig. 12 Three Level output Inverter3

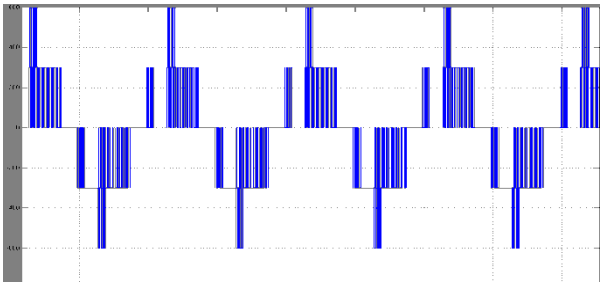
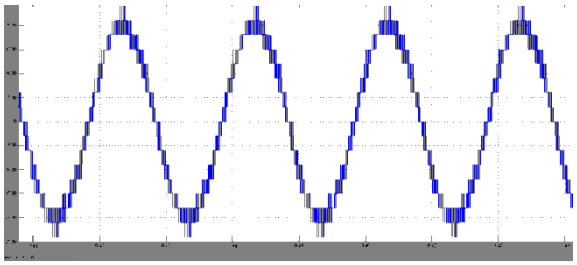


Fig. 13 Three Level output Inverter4

Fig10 to 13 shows the individual inverter outputs. From the figures it is clear that each output consists of only three levels.



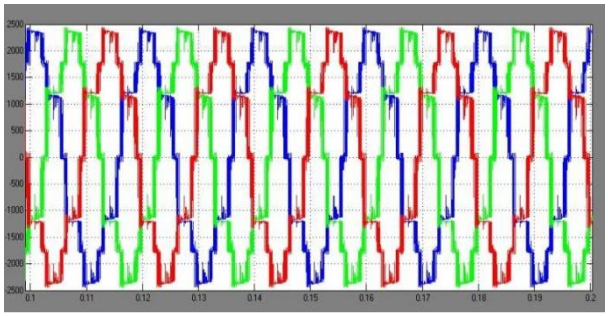


Figure.15.Multilevel output three phase

This waveform represents the output voltage of the three phase multilevel inverter.

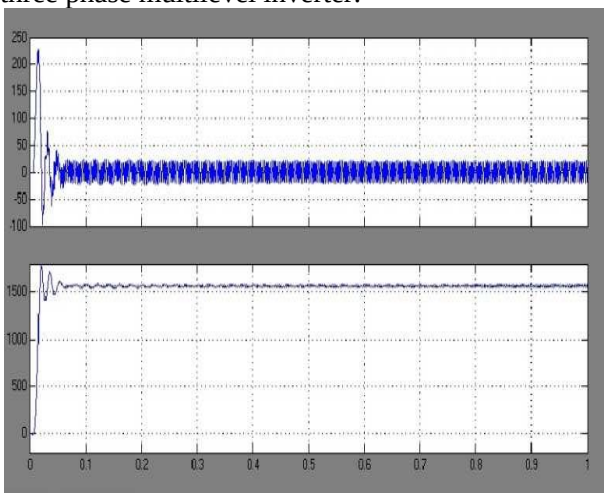


Fig.16: Electromagnetic Torque and Speed curves of SQCIM

The first waveform represents the Electromagnetic Torque and rotor speed characteristics of the Squirrel cage Induction motor.

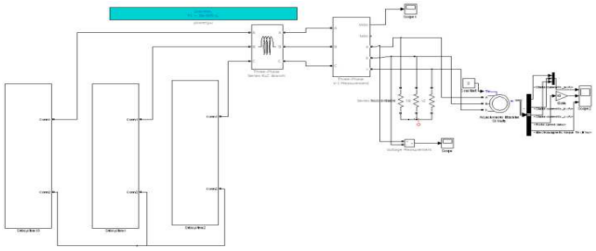


Fig.17 Simulink model of Cascaded multilevel inverter fed induction motor

Fig.17 shows the simulink model of the Cascaded multilevel inverter fed to an induction motor.

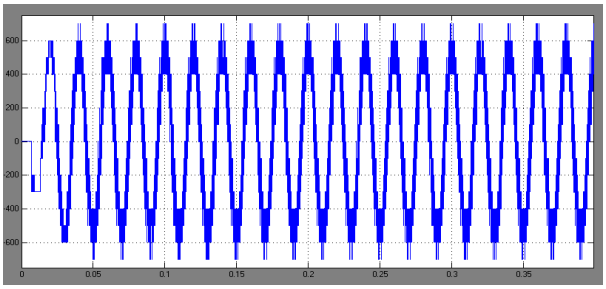


Fig.18 Line voltages of inverter

Fig.18 shows the line-line voltages of the CMLI

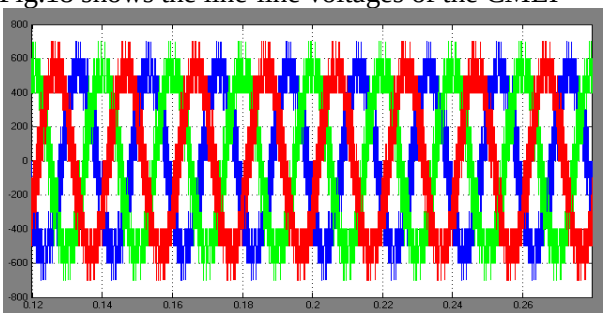


Fig.19 Three phase voltage of inverter

Fig.19 shows the three phase voltages of the CMLI

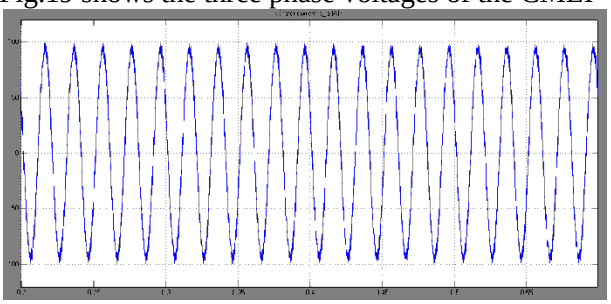


Fig.20 Stator current

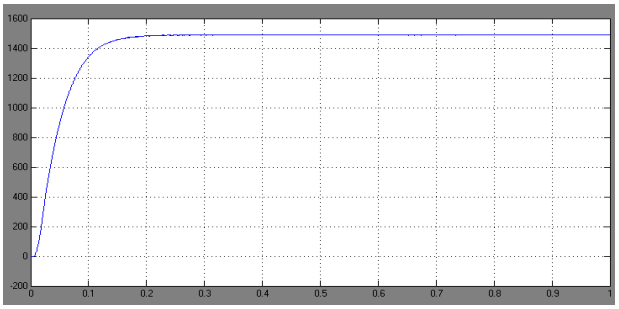


Fig. 21Speed of the motor

Fig.21shows the speed curve of the induction motor. It is having the speed of 1450 r.p.m.

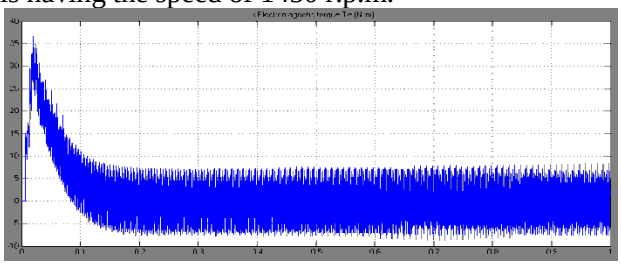


Fig.22 Electromagnetic Torque

Fig.22 shows the electromagnetic torque characteristics of the induction motor

CONCLUSION

A series connection of three-level inverters has been proposed for a medium-voltage SQIM drive with increased voltage capacity. The topology ensured high-power operations with medium-voltage output having several voltage levels. The reduction in the ratings of the dc bus capacitor and reduced imbalance problems in the dc bus are some of the advantages of the proposed topology over the existing topologies. The disadvantage of the proposed topology is that it requires additional output transformers which introduce additional cost and losses. However, these transformers do not have complex underutilized windings like that required in cascaded H-bridge topologies. In this paper conventional and the cascaded multilevel inverter topologies were discussed and results were placed. Finally a Matlab/Simulink model is developed and simulation results are presented.

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