A Novel Low Power, Low Area Multiplier

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Abstract: *Now a days the each and every computer applications are used to process by digital signal processing only. Multiplication, one of the basic arithmetic operations are playing a vital role in such DSP applications like filtering and fast Fourier transforms (FFT). Basically this multiplication is used to achieve high execution speed, parallel array multipliers are widely used. This paper proposes a low power and low are occupying multiplier with a carry saving adder circuit. The main advantage with this proposed approach is it eliminates the final stage of the multiplier where as in the conventional array multiplier it is included, so that it consumes more power as well as more area to process even a 4X4 multiplication. In this approach for a 4x4 multiplier to add carry bits without using Ripple Carry Adder (RCA) in the final stage, the carries given to the input of the next left column input. Due to this the proposed approach gains more efficiency than the conventional approach.*

Keywords *–DSP, array multiplier, carry save addition, RCA, PTM, power consumption*

I. INTRODUCTION

In recent days to process any computer applications digital signal processing is playing a vital role. In those digital processing applications such as filtering, fast Fourier transform, wavelet transform, etc., multiplication of the data with some high frequency components is the main operation has to be done. As the array sizes of the input data or carrier data increased the multiplication also becomes complex and also time consuming process. So to overcome this as well as to achieve high execution speed parallel array multipliers are introduced which performs the array multiplication of multiuser data simultaneously. But these multipliers consume more power. Power consumption has become a critical concern in today's VLSI system design. Hence the designers are needed to concentrate power efficient multipliers for the design of low-power DSP systems.

In recent years, several power reduction techniques have been proposed for low-power digital design, including the reduction of supply voltage, multi threshold logic and clock speed, the use of signed magnitude arithmetic and differential data encoding, the parallelization or pipelining of operations, and the tuning of input bit-patterns to reduce switching activity [1].

A basic multiplier can be divided into three parts i) partial product generation ii) partial product addition and iii) final addition. In this paper we present a low power design methodology for parallel array multiplier using Carry Save Adder (CSA). The rest of this paper is organized as follows. Section-II presents the total power consumption in CMOS circuits with mathematical expression. Section-III explains the basic structure of an array multiplier with mathematical expression. The methodology of the proposed multiplier with conventional array multiplier is presented in Section-IV. Results of total power, worse case delay and EDP with different technologies is discussed in Section-V. Section-VI is the conclusion of the work.

II. POWER CONSUMPTION IN CMOS VLSI CIRCUITS

There are three main components of power consumption in digital CMOS VLSI circuits. 1) Switching Power: consumed in charging and discharging of the circuit capacitances during transistor switching. 2) Short-Circuit Power: consumed due to short-circuit current flowing from power supply to ground during transistor switching. This power more dominates in Deep Sub Micron (DSM) technology. 3) Static Power: consumed due to static and leakage currents flowing while the circuit is in a stable state. The first two components are referred to as dynamic power, since power is consumed dynamically while the circuit is changing states. Dynamic power accounts for the majority of the total power consumption in digital CMOS VLSI circuits at micron technology [2], [3].

$$P = \sum iV_{DD}V_{swing}C_{load}fp_i + V_{DD}\sum iI_{isc} \sum V_{DD}I_l$$

Where
V_{DD} -power supply voltage;
V_{swing} - voltage swing of the output which is ideally equal to VDD;
C_{load} -load capacitance at node i;
f -system clock frequency;
Pi -switching activity at node I;
l_{ise} - short-circuit current at node;
I_l -leakage current.
As designing a low power CMOS I-bit full adder, the emphasis will be on these areas

i) to reduce the total number of transistors and the total number of parasitic capacitances in internal nodes to reduce the load capacitance.
ii) to lower the switching activity to save the dynamic power consumption.
iii) to remove some direct paths from power supply to ground to save the short-circuit power dissipation.
iv) to balance each path in the full adder to avoid the appearance of glitches since glitches not only cause a unnecessary power dissipation hut may even lead to a fault circuit operation due to spurious transitions, especially in a low voltage operation system.
v) in order to build a low-voltage full adder, all the nodes in the circuit must possess full voltage swing.
vi) to build the low-voltage full adder design because the power supply voltage is the crucial factor in reducing power dissipation.
In Nanometer scale leakage power dominates the dynamic power and static power due to hot electrons. So the concentration is on to trade off power in parallel multipliers.

III.PARLLEL MULTIPLIER

Consider the multiplication of two unsigned n-bit numbers, where X = X_{n-1}, X_{n-2}, ... X_o is the multiplicand and Y =Y_{n-1},Y_{n-2}----- Y_O is the multiplier. The product of these two bits can be written as [4]. In this X is considered as a multiplicand and Y is considered as multiplier

$$P = (\sum_{i=1}^{n-1} X_i \sum_{j=1}^{n-1} Y_j) 2^{i+j}$$

In the given example, we have 4-bit multiplier and 4-bit multiplicand. By using the above equation (2) we can generate 4-rows of partial products as shown in the "Fig. (1)". The hardware required for the generation of these partial products is AND gates. Using any adder like Carry Save Adder (CSA), Carry Propagate Adder (CPA) we can add the partial products. In this method we are following Carry Save Addition to add the products.

$$\begin{array}{cccccccc}
 & & X_3 & X_2 & X_1 & X_0 & & \\
 & & Y_3 & Y_2 & Y_1 & Y_0 & & \\
\hline
 & & & & X_0Y_3 & X_0Y_2 & X_0Y_1 & X_0Y_0 \\
 & & & X_1Y_3 & X_1Y_2 & X_1Y_1 & X_1Y_0 & \\
 & & X_2Y_3 & X_2Y_2 & X_2Y_1 & X_2Y_0 & & \\
 & X_3Y_3 & X_3Y_2 & X_3Y_1 & X_3Y_0 & & & \\
\hline
P7 & P6 & P5 & P4 & P3 & P2 & P1 & P0
\end{array}$$

Fig.1:4X4 multiplication

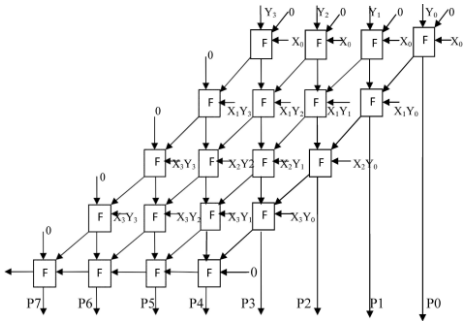

Fig. 2. Conventional Array Multiplier with CSA.

IV. METHODOLOGY

In the Carry Save Addition method, the first row will be either Half-Adders or Full-Adders. If the first row of the partial products is implemented with Full-Adders, C_{in} will be considered '0'. Then the carries of each Full-Adder can be diagonally forwarded to the next row of the adder. The resulting multiplier is said to be Carry Save Multiplier, because the carry bits are not immediately added, but rather are saved for the next stage. In the design if the full adders have two input data the third input is considered as zero. In the final stage, carries and sums are merged in a fast carry propagate (e.g. ripple carry or carry-look ahead) adder stage [5]. This is the conventional array multiplier with CSA as shown in "Fig. (2)".

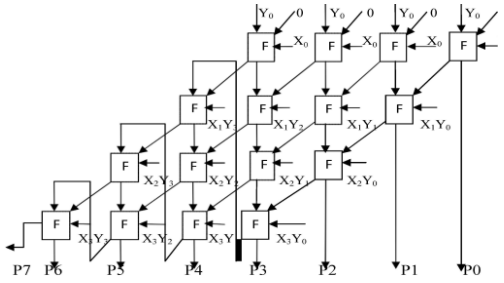

Fig .3. Proposed Array Multiplier with CSA.

In the proposed method, we implement all the partial product rows of the multiplier as same as that of the conventional adder (explained above).The final adder which is used to add carries and sums of the multiplier is removed in this method. Then the carries of the multiplier at the final stage is carefully added to the inputs of the multiplier as shown in the "Fig (3)". The carry of the fourth column of the multiplier is given to the input of the fifth column instead of zero. Then the carry of the fifth column is forwarded to the input of the sixth column so on. In this multiplier the carry of the seventh column of the adder is not neglected, it is considered as Most Significant Bit (MSB) of the multiplier. Due to elimination of four full adders in the final stage power and area can be trade off in the proposed design than that of the conventional array multiplier.

V. RESULTS AND DISCUSSION

To show the proposed design very good performance, the design is synthesized with 16-Transistor Full Adder design. Among the Transmission Gate CMOS, Transmission Function Full Adder (TFA), 14-T adders this shows good efficiency in terms of power and delay [6]. The results of the 16-T full adder are as shown in the Table. (1).

The results are carried out with the use of Tanner EDA tool and H-Spice. Among the four types of full adders [6] 16-T full adder shows good efficiency in energy delay product. Though it shows good efficiency due to less transistor count 14-T full adder (which also has less power consumption little bit more than 16-T) is used to design the multiplier. The comparison of CSA and CSA without RCA in power, delay and energy delay product is given in the "Table 2". Due to 56 less transistors CSA without RCA shows less power consumption, delay efficient and also occupy less area. The proposed method also applied to column bypassing multiplier and the results are discussed below.

i) Total Power

The bypassing method should reduce the dynamic power from the total power of the multiplier. The total power of 4x4, bypassing multipliers conventional and proposed are given in the "Table 2". 0.18um technology is the standard one, the other are the Predictive Technology Model (PTM) files downloaded from Berkeley website. For a 4x4 Braun multiplier the proposed multiplier has shown 13.91% less power consumption than that of the conventional for TSMC 0.18um. For the same technology the 4x4 PCBM shows 23.38% less power consumption than CBM. Due to removal of RCA 56 transistors are saved which leads to save power consumption. For high order multipliers the PCBM shows less power consumption. All the data is calculated at a supply voltage 2.0V and the temperature of 25^0C.

Table 1: Adder results

Adder Type	Power	delay	PDP	EDP(js)
TG-CMOS	5.07E-05	9.36E-10	4.74552E-14	4.44181E-23
TFA	3.05E-05	2.51E-09	7.6555E-14	1.92153E-22
14-T	2.33E-05	8.97E-10	2.09001E-14	1.87474E-23
16-T	1.36E-05	5.07E-10	6.8952E-15	3.49587E-24

ii)Propagation Delay

The propagation delays of the two multipliers are calculated for all inputs and outs. Longest propagation delay is considered as worst case delay. The proposed multiplier shows more efficient than the convention. For 180nm the proposed shows 34.09% more efficiency than the conventional and PCBM have 92.85% efficiency.

III).Energy Delay Product

Energy = Power x Delay or Power Delay Product. Energy x Delay is the Energy Delay Product. The proposed array multiplier shows efficiency in energy delay product. It shows for 180nm – 59.91%, 90nm – 9.35% and 65nm – 29.21% improvement in the EDP.

In 4x4 proposed multiplier we can save 4 full adders, for 8x8 multiplier 8 full adders and 16x16 multiplier we can save 16 full adders. Then the proposed multipliers occupy less area on chip.

Table 2 4x4 Array Multiplier

Technology (um)	Total Power (Watts)	Delay (Sec)	(PDP)	(EDP)	Max Power
0.18	2.46E-04	1.65E-09	4.0611 6E-13	6.6968 5E-22	2.23E-02
0.18	2.12E-04	1.09E-09	2.3038E-13	2.5035 4E-22	2.27E-02
90nm	3.81E-04	8.39E-10	3.1974 6E-13	2.6841 7E-22	4.31E-02
90nm	3.29E-04	9.30E-10	3.0578E-13	2.8451E-22	4.14E-02
65nm	2.05E-04	1.10E-09	2.2647 5E-13	2.5002 8E-22	1.98E-02
65nm	1.67E-04	1.10E-09	1.8338 8E-13	2.0139 7E-22	1.92E-02

VI. CONCLUSION

This paper proposes an array multiplier based on RCA having high performance, low area occupying and also low power consumer. It shows the same functionality than the CSA method. For higher bit multiplication it shows better power and area saving. For example, in the proposed 4x4 multiplier it saves 56 transistors. For TSMC 0.18um it saves 13.91% of total power, 34.09% of more speed and 59.91 % less energy consumption. To study the

performance of the multiplier, it is synthesized with different technologies.

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