Development of Data Communication and Acquisition System

K. S. Padmaja[1], A. Naresh[2], M. Nageswar Rao [3], Manikanta Prahlad M[4]

[1] Scientist-'F', NSTL, Defence Research & Development Oraganisation, Visakhapatnam, A.P., India
[2] Scientist-'D', NSTL, Defence Research & Development Oraganisation, Visakhapatnam, A.P., India
[3] Scientist-'C', NSTL, Defence Research & Development Oraganisation, Visakhapatnam, A.P., India
[4]Research Scholar, Dept of ECE, University College of Engineering, JNTUK, Kakinada, A.P, India

Abstract— **The main aim of this project is to implement communication protocol between the base station and under water vehicle and also acquire the data with various sensors. Data communication and acquisition system designs with PowerPC440EP Microprocessor. The system receives information from the base station and sends to sub systems in the vehicle. It receives information from the sub systems in the vehicle and sends to the base station. Software is developed to acquire, record the data and monitor the health of the system when system is online, and communication with base station. The software is developed using high level language 'C' and GREEN HILLS compiler.**

Keywords—PowerPC440EP; Communication system; Data acquisition system; High level language 'C'; GREEN HILLS compiler.

I. INTRODUCTION

An on board Data Communication and Acquisition system requires a system controller. It has to interface with various sensors. Also it has to communicate with base station. Data Communication and Acquisition system is developed with PowerPC 440 Embedded Processor for under water vehicles. RS232 communication is used to interface with MODEMs and subsystems in under water vehicle. Data can be transferred between multiple subsystem units over a single transmission media, with the communications between the different subsystems in under water vehicle taking place at different moments in time. The system accepts 18 analog inputs with 12 bit resolution. The acquired data is transmitted to substation using RS232 communication.

The PPC440EP provides high performance and low power consumption with CPU executing at sustained speeds approaching two instructions per cycle. On-chip peripherals reduce chip count and design complexity in systems and improve system throughput. It has six Hardware interrupt lines for peripherals.

Software is developed in High level language 'C' for acquiring data from various subsystems in under water vehicle and communication with base station.

In order to process acquired data from various sensors transmitted through serial communication, Graphical User Interface (GUI) is provided at base station and GUI is developed in Visual Basic Programming Language.

II. SYSTEM DEVELOPMENT

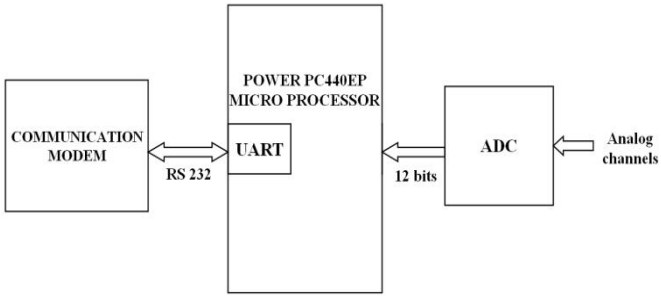

Figure1: Block Diagram of Data Communication and Acquisition System

Major subsystems are

A. RS232 (serial communication)

RS232 provides physical interface and protocol for relatively low speed serial data communication between computer and related device. RS232 is an asynchronous serial communication. Special bits will be added to each word in order to synchronize the sending and receiving of the data.

B. Power pc440EP microprocessor

The POWER PC440EP contains of five internal buses, two processor local buses(PLBs), two on-chip peripheral buses(OPBs) and one device control register bus(DCR).

The DCR bus provides a mechanism for the PPC440EP to setup other on chip facilities. It also allows the PPC440EP CPU to communicate with peripheral devices without using the PLB interface

All serial data transmissions are controlled by the Universal asynchronous receiver and transmitter (UART). PPC440EP provides four serial ports with selectable internal or external serial clock to allow wide range of baud rates. Serial peripheral interface (SPI) provides full duplex, synchronous, character-oriented port that allows the exchange of data with serial devices. External peripheral Bus Controller (EBC) support SRAM, Flash memory, EPROM and slave peripheral I/O banks. PCI interface allows connection of PCI devices to PPC processor and local memory.

NAND flash controller provide interface between the EBC and up to four separate external NAND flashes. NAND flashes are used in code dumping for PPC440EP.

The PPC440EP provides two Ethernet media access controllers (EMACs) that are generic implementations of the Ethernet Media Access Control (MAC) protocol complying with ANSI/IEEE Std 802.3 and IEEE 802.3u supplement. Both EMACs support half-duplex (CSMA/CD) and full-duplex operation for 10-Mbps and 100-Mbps operations.

The PPC440EP contains two universal interrupt controllers (UIC0 and UIC1) that provide all necessary control, status, and communication between the various internal and external interrupt sources and the processor core.

C. DATA ACQUISITION SYSTEM

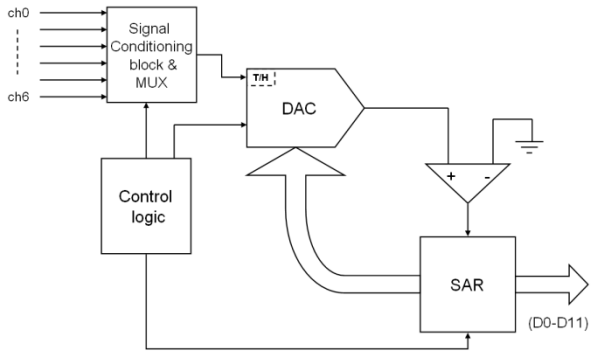

Figure2: Data Acquisition System

Analog data from various sensors is acquired and converted into digital data using data acquisition system. Each acquisition system contain six analog inputs and channels are selected (at a time one) by control logic through multiplexer.

DAS operate at +5v supply with 12 bit resolution and ½ LSB linearity. DAS provides sampling rate of 100ksps with 6us conversion time. Internal or External Acquisition mode of Control is used to acquire data from various sensors. Clock will be given internally or externally. The converted data is in unipolar mode or bipolar mode and is selected by writing control byte to DAS.

III. IMPLEMENTATION

A. DATA ACQUISITION

DAS acquires data from various sensors .The control byte is latched into the device, on pins D7–D0, during a write cycle. Conversions are initiated with a write operation, which selects the MUX channel and configures the DAS for either a unipolar or bipolar input range. A write pulse (WR + CS) can either start an acquisition interval or initiate a combined acquisition plus conversion. The sampling interval occurs at the end of the acquisition interval. The ACQMOD bit in the input control byte offers two options for acquiring the signal: internal or external. The conversion period lasts for 12 clock cycles in either internal or external clock or acquisition mode. Writing a new control byte during a conversion cycle will abort the conversion and start a new acquisition interval.

Internal Acquisition:

Select internal acquisition by writing the control byte with the ACQMOD bit cleared (ACQMOD = 0). This causes the write pulse to initiate an acquisition interval whose duration is internally timed. Conversion starts when this six-clock-cycle acquisition interval (3µs with f=2MHz) ends.

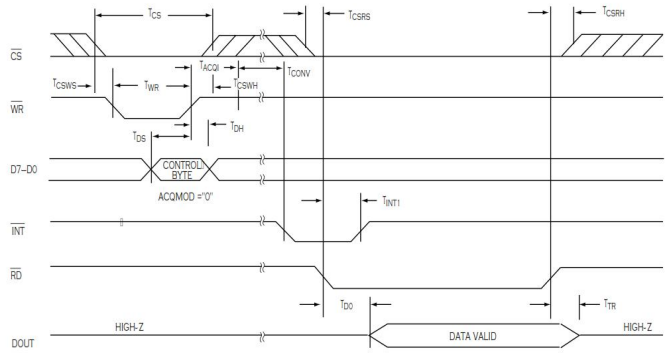

Figure3: Timing diagram for internal acquisition

External Acquisition:

Use the external acquisition timing mode for precise control of the sampling aperture and/or independent control of acquisition and conversion times. The user controls acquisition and start-of-conversion with two separate write pulses. The first pulse, written with ACQMOD = 1, starts an acquisition interval of indeterminate length. The second write pulse, written with ACQMOD = 0, terminates acquisition and starts conversion on WR's rising edge. However, if the second control byte contains ACQMOD = 1, an indefinite acquisition interval is restarted.

The address bits for the input MUX must have the same values on the first and second write pulses. Power-down mode bits (PD0, PD1) can assume new values on the second write pulse.

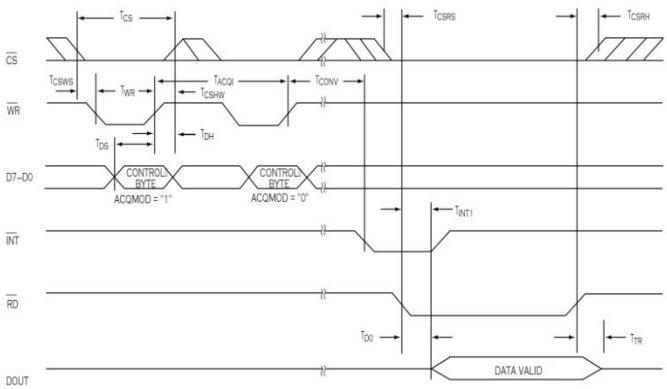

Figure4: Timing diagram for external acquisition

A standard interrupt signal, INT, is provided to allow the device to flag the µP when the conversion has ended and a valid result is available. INT goes low when conversion is complete and the output data is ready. It returns high on the first read cycle or if a new control byte is written.

Three data acquisition systems are interfaced to PPC 440EP processor to acquire data through 18 analog channels. The acquired data is recorded in memory when the system is in online.

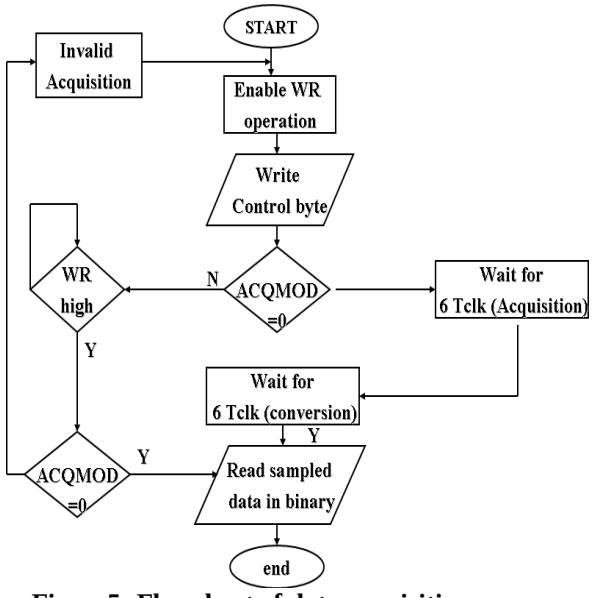

Figure5: Flowchart of data acquisition process

B. COMMUNICATION:

Serial communication:

The acquired data from various sensors is transmitted using RS232 serial communication. UARTs establish communication between PPC 440EP and serial communication port. Internally PPC 440EP provide four channel UART. In order to access more channels from DAS, external UARTs(two/four/eight channel) are connected via external peripheral connector of PPC 440EP.By configuring the UART registers Baud rate settings and start bit, stop bit and parity bit setting are made in PPC 440EP. Hyper Terminal initializes serial communication settings in personnel computer.

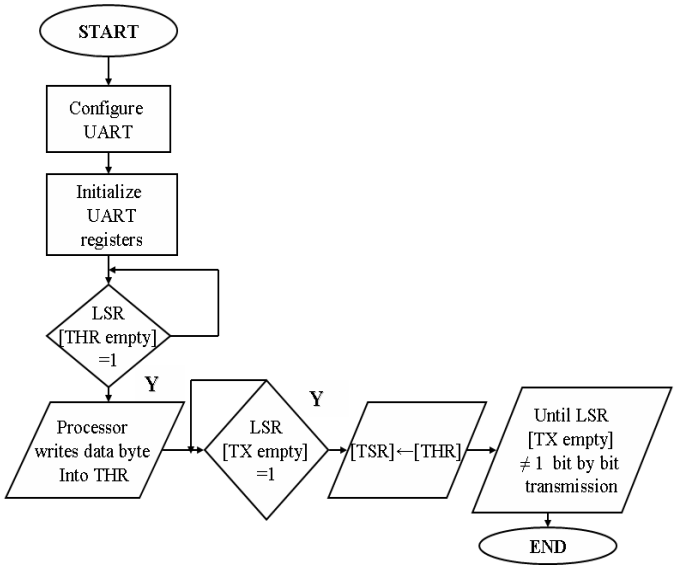

Figure6: Flowchart of serial data transmission in UART

Transmitter:

The host loads transmit data to THR one character at a time. The THR empty flag (LSR) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR) when it is enabled by IER. The TSR flag (LSR) is set when TSR becomes completely empty.

Receiver:

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR.

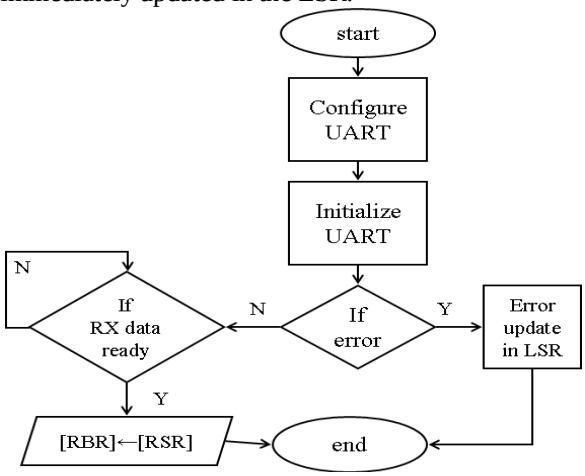

Figure7: Flowchart of serial data receiver operation in UART

Interfacing Octal UART to Data Communication and Acquisition System through PPC 440EP processor provides eight serial communication channels. Octal UART provides serial communication between various subsystems of under water vehicle and PPC 440EP processor.

IV. SOFTWARE DEVELOPMENT

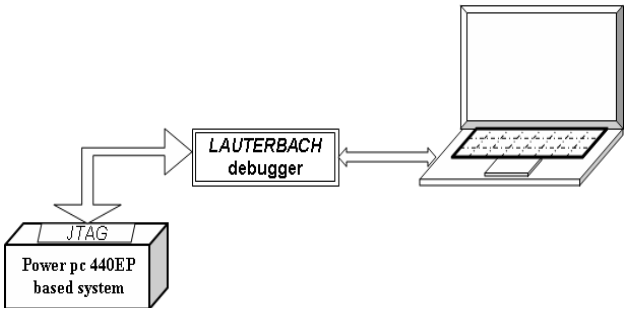

Figure10: Block Diagram of Software Development

The software for this application is developed in 'C' language using Green Hills compiler, TRACE32 tools and Lauterbach debugger. The complete development system comprising a PC with the Green Hills installed, Lauterbach debugger connected to the PC parallel port, JTAG and target board are shown in Figure 10.

V. RESULTS AND CONCLUSION

18 channel DAS, acquire data from various sensors at a sampling rate of 100kbps and converted into 12 bit digital data. Converted data from DAS is loaded into NVRAM and will be monitored through TRACE32 tool shown in figure11.

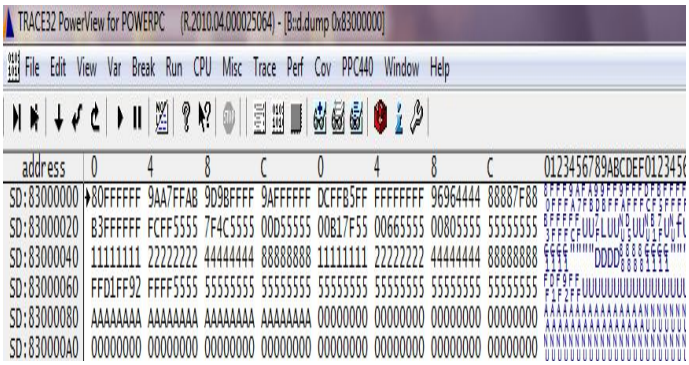

Figure11: Acquired Data from DAS stored in NVRAM

Data downloaded from NVRAM is transmitted to base station at a baud rate of 9600 bps using RS232 serial communication .Code is developed in visual basic programming language to monitor, received data at base station and received data at base station is shown in figure12.

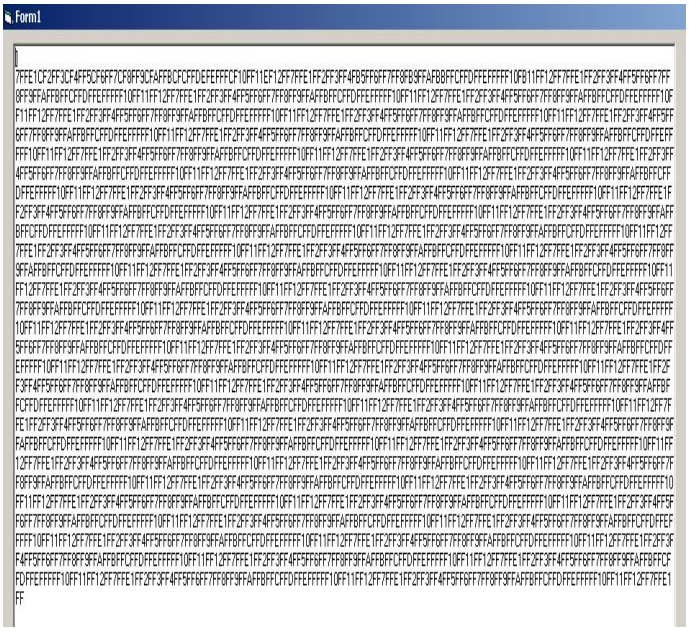

Figure12: Serial Data received at base station

The development brought out from the Data Acquisition System is to acquire the phisical parameters very rapidly, accurately and in recorded form.

A High performance with sustained speeds is achieved through power PC 440EP processor.

VI. References

- PPC 440EP Embedded processor user's manual by AMCC, Revision 1.27, 2008 [1]
- PPC 440EP processor data sheet by AMCC, Revision 1.29, 2008 [2]
- Embedded System Design, A unified Hardware/ Software introduction, Frank Vahid/ Tony Givargis.
- DAS (MAX 196) reference manual [3]
- GREEN HILLS cross compiler reference books [4]
- Richard Grier, Serial Communication Handbook[5]
- Let us 'C' by Yaswanth Kanetkar [6]
- www,dataarchive.com [7]
- http://www.vbtutor.net/ [8]
- http://www.vb6.co.uk/ [9]

