Simulation of Buck-Boost Type Unity Power Factor Rectifier with and without controlled switch

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Abstract— **A buck–boost-type unity power factor rectifier with and without controlled switch is proposed in this paper. The main advantage of the proposed rectifier without controlled switch over the conventional buck–boost type is that it can perform input power factor correction (PFC) over a wider voltage conversion range. With a single switch, a fast well-regulated output voltage is achieved with a zero-current switch at turn-on. Moreover, the switch voltage stress is independent of converter load variation. The proposed converter without controlled switch is well suited for universal offline PFC applications for a low power range (<150 W). But if there is any requirement for the control of the switch according to the load variation, then we go for the Buck-Boost type UPF rectifier with control switch. The feasibility of the converters is confirmed with results obtained from a computer simulation and from experimental prototypes.**

Keywords— **Low harmonic rectifier, power factor correction (PFC), single-stage single-switch rectifier, unity power factor (UPF).**

I. INTRODUCTION

Many single-stage power factor correction (PFC) topologies have been recently proposed as a cost-effective approach for achieving both the function of high PFC and fast output voltage regulation by using one (or one set of synchronized) active switch(es) under a single control loop. Unfortunately, unlike the two-stage approach, single-stage converters have relatively high-voltage stress suffered by their switching components due to unregulated dc voltage on the intermediate energy storage capacitor, which generally depends on both the line and load characteristics [1]–[3]. This condition will limit the single-stage approach, particularly when it requires an operation with a universal input voltage since the storage capacitor voltage would easily rise beyond 450 V. Therefore, a bulky capacitor and high-voltage-rating semiconductors have to be used; this increases both the size and cost, and will result in lower efficiency as well as reduced holdup time.

In an effort to reduce the DC voltage on the energy storage capacitor, a number of techniques have been introduced [4]-[29]. However, most of the proposed techniques usually comprise a boost converter for PFC, followed by a dc-dc converter for output voltage regulation. Hence, low-output-voltage applications, a high step down transformer topology

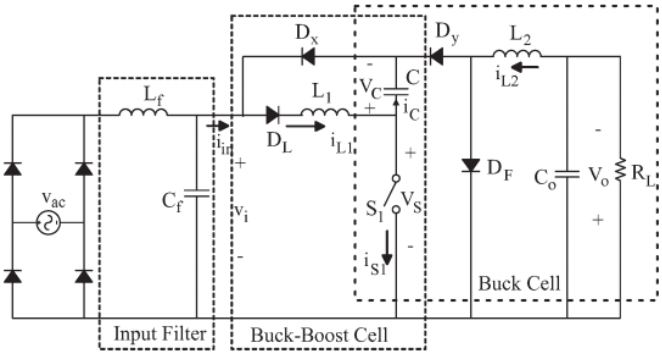

Fig. 1 Proposed single-stage PFC converter without controlled switch

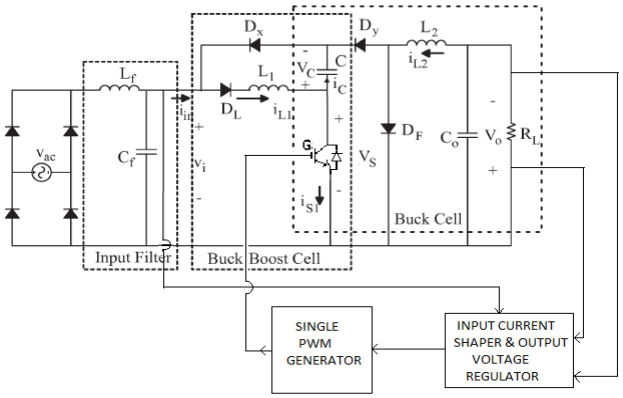

Fig. 2 Proposed single-stage PFC converter with controlled switch

would be needed for the output dc-dc stage even when galvanic isolation is not required.

On the other hand, conventional single-switch buck–boost topologies, including the plain buck–boost, flyback, SEPIC, and Cuk converters [30], [31], have the potential of both PFC and step-down conversion capability. However, they incur penalties of reduced efficiencies and increase component stresses, compared to the boost converter. Moreover, the buck–boost topologies suffer from providing low output voltage over a large range of input voltages since it requires an extremely low duty ratio (short switch-on time) operation. A high-switching frequency operation reduces the switch-on time even shorter and gives rise to an objectionable increase in switching losses. Thus, not only does it degrade the efficiency

of the converter but it also limits the ability to increase the switching frequency. Moreover, considering, for example, a buck–boost converter with V_{IN} = 370 V and V_{OUT} = 5 V operating at 100 kHz would require a switch-on time of 133 ns, which is close to the physical limitation of some of the low-cost pulse width modulation controller's minimum on-time. Last but not the least, conventional buck–boost topologies operating with extremely low or high duty ratio utilize the active switch very poorly [32].

The motivation and main objective of this paper have been established from the result of previous literature research on buck-boost type unity power factor rectifier with extended voltage conversion ratio [34].

We approach this task by cascading a front-end buck-boost converter with an output buck converter, as shown in Fig.1. The buck boost converter is selected due to its capability of providing a step-down voltage conversion and a high power factor when it is operating in the discontinuous conduction mode (DCM). On the other hand, the buck converter is selected due to its step-down capability. Hence, a high step-down ratio is achieved. In addition, the related characteristics of the proposed converter in Fig.1 also include the absence of inrush current problem and the ability to protect against over load current.

It should be mentioned here that the proposed converter in Fig. 1 is a modified version of its dc–dc version presented in [33], by adding an additional diode D_L in series with L_1. Moreover, the operation of the buck output cell in Fig. 1, in either the continuous conduction mode (CCM) or DCM, has no effect on the quality of the input current. However, it is found that operating the buck cell in the DCM gives several desirable advantages include the following:

1) zero-current switch turn-on;
2) reduction of the reverse recovery problem of the fast diodes in the circuit;
3) low-voltage stress on both the energy storage capacitor C and the active switch S_1, and independent of the output load current;
4) well and fast regulation of the output voltage.

The aforementioned advantages are obtained at the expense of drawing higher peak currents by the converter. By using a high speed and a higher current density switch, the peak currents and their impact become less significant when compared to the gained advantages. Furthermore, the converter efficiency can be improved if buck cell inductor L_2 is operated in the boundary conduction mode (BCM) since the peak currents in the converter will be relatively reduced. This will also reduce the ac core losses as well as the current ripple in output capacitor C_0.

The proposed converter in Fig.2 is well suited for automatic control of the switch according to the load variations. For this, the output voltage and the input current are given to the input current shaper and output voltage regulator, and the output of this is given to the single PWM generator. This single PWM generates the controlled gate pulses according to the load variations.

Section II presents the principle of operation of the proposed converters along with the important circuit equations. A low-frequency averaged model of the proposed converters and the steady-state characteristics is presented in Section III. Simulation results are presented in Section IV to verify the validity of the proposed concepts. Finally, a conclusion will be given in Section V.

II. Converters Operation Principle

The proposed converter shown in Fig. 1 is analysed with six assumptions in this section.

1. Input voltage V_{ac} is considered to be an ideal rectified sine wave, i.e., $v_i = V_m|sin(\omega_L t)|$, where V_m is the peak amplitude and ω_L is the line angular frequency.
2. All components are ideal; thus, the efficiency is 100%.
3. Switching frequency f_s is much higher than ac line frequency f_L, so that the input voltage can be considered constant during one switching period T_s.
4. Capacitor C is big enough such that voltage V_c can be considered constant during T_s. Furthermore, output voltage V_0 is pure dc without twice the line frequency ripple.
5. Both inductors L_1 and L_2 operate in the DCM. Furthermore, the current in inductor $L_1(i_{L1})$ reaches zero level prior to the current in $L_2(i_{L2})$.
6. The phase shift of the input line current introduced by the input filter is minimal and can be neglected.

With these assumptions, the circuit operation over one switching period T_s can be described in three operating stages, as shown in Fig. 3.

Stage 1 [t_0, t_1]: Prior to this interval, the currents through $L_1$and L_2 are at ground level. When switch S_1 is turned on at t=0, diode D_y becomes forward biased, and currents i_{L1} and i_{L2} begin to linearly increase. This interval ends when switch S_1 is turned off, initiating the next stage.

Stage 2 [t_1, t_2]: When the switch is turned off, diode D_y becomes reverse biased. Thus, current i_{L1} linearly decreases through diode D_x, whereas current i_{L2} linearly decreases at a rate proportional to output voltage V_0 through the freewheeling diode D_F. This stage ends when current i_{L1} reaches the ground level. Diode D_L prevents current i_{L1} from becoming negative.

Stage 3 [t_2, t_3]: In this stage, current i_{L2} continues to decrease through the freewheeling diode D_F until it becomes zero. The converter stays in this stage until the switch is turned on again. To improve the overall efficiency, it is preferred to turn on the switch at t=t_3, which will reduce the current stresses through the semiconductor devices.

The operation of the proposed converter shown in Fig.2 is almost similar to the operation of the converter shown in Fig.1, but the only difference is that the operation of the switch in Fig.2 is according to the load variation.

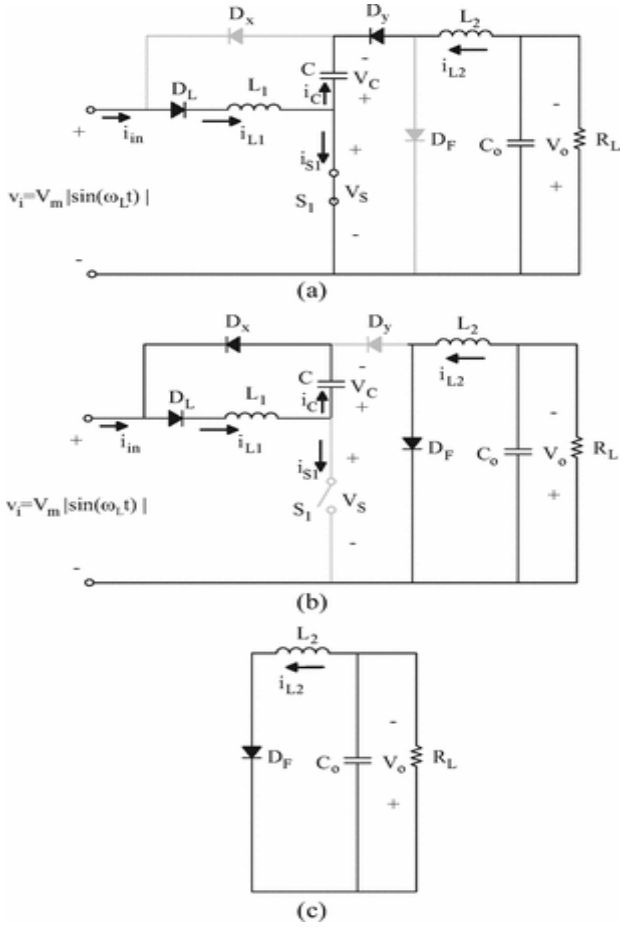

Fig. 3 Operating stages of the proposed single-stage PFC converter without controlled switch (a) Stage 1. (b) Stage 2. (c) Stage 3.

The characteristics of the ideal circuit waveforms are shown in Fig. 4. These characteristics are taken for one switching period T_s. The currents flowing in inductors L_1 and L_2 are also shown. The current in the capacitor and the current in the switch S_1 are also shown according to the switch operation. But the switch is not opperated according to the load variation.

III. Theoretical Analysis

A. Conditions for DCM

The normalized switch-off time defined by D_2 and D_3 can be found in terms of switch duty cycle D_1 by applying voltage-second to both L_1 and L_2, respectively, which gives The normalized switch-off time defined by D_2 and D_3 can be found in terms of switch duty cycle D_1 by applying voltage second to both L_1 and L_2, respectively, which gives

$$D_2 = D_1 \frac{v_i}{V_C} \quad (1)$$

$$D_2 + D_3 = \left(\frac{V_C - V_O}{V_O}\right) D_1 \quad (2)$$

To maintain a sinusoidal input current, L_1 must operate in DCM over the entire ac line cycle. For inductor L_1 to operate in DCM, the following condition must be held:

$$D_2 \leq 1 - D_1 \quad (3)$$

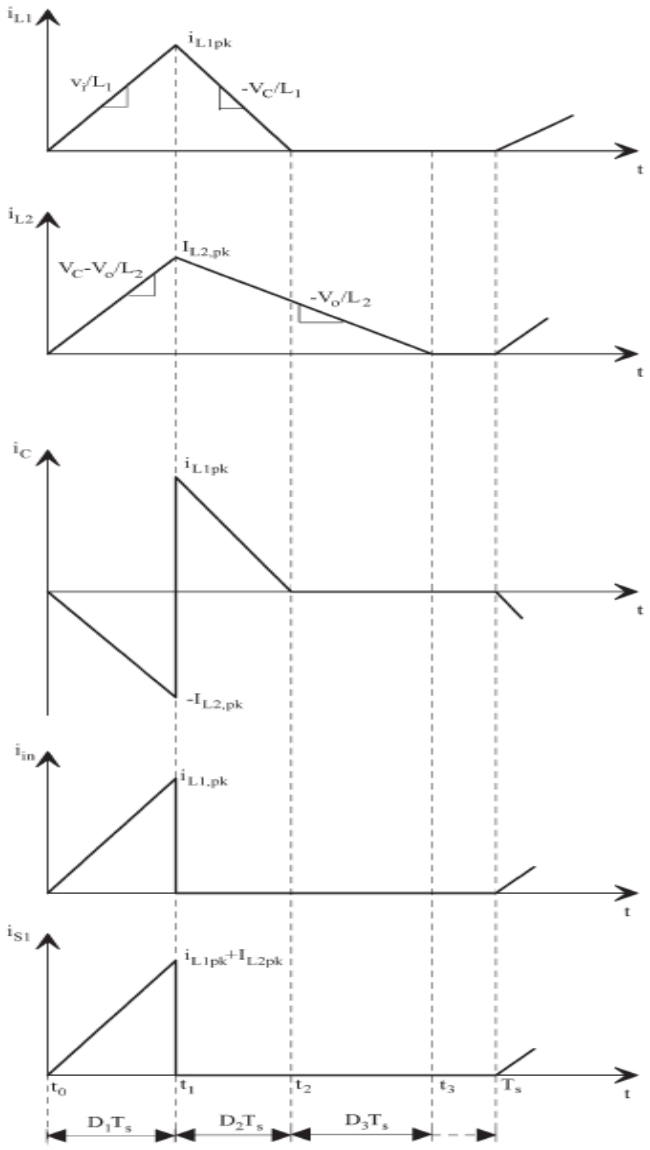

Fig. 4 Idealized waveforms

The condition for inductor L_2 to be in DCM is satisfied if

$$D_2 + D_3 \leq 1 - D_1 \quad (4)$$

Simplifying (3) and (4) by using (1) and (2) gives the following results:

$$\frac{v_i}{V_o} \leq \frac{1 - D_1}{D_1^2} \quad (5)$$

$$D_1 \leq \frac{V_0}{V_C} \quad (6)$$

Note that, from (5), the condition for L_1 to be in DCM can be always satisfied over the entire ac line period, while the worst case must be satisfied when $v_i = V_m$. Moreover, the assumption is that the current in L_2 reaches zero level after the current in L_1 is also satisfied since $D_1 + D_2 \leq D_1 + D_2 + D_3$.

Operating L_2 in BCM requires the sum of the normalized subintervals length to be unity, i.e., $D_1+D_2+D_3=1$; hence, the inequality in (6) will be modified to $V_0=D_1V_C$. It is important for L_2 to be in BCM in order to reduce the current stress on

the semiconductor devices, leading to better overall efficiency improvement.

B. DC Capacitor Voltage V_C

The dc capacitor voltage V_C determines the voltage stress across switch S_1 and diodes D_x and D_y. Therefore, it is an important design factor. Voltage V_C can be found by applying charge balance on C in a half-line cycle $T_L/2$. The average capacitor current over $T_L/2$ is

$$\langle i_C(t)\rangle_{T_L/2} = \frac{2}{T_L}\int_0^{T_L/2} \langle i_C(t)\rangle_{T_S} dt \tag{7}$$

The averaged value of the capacitor current over one switching period T_s, i.e.,$\langle i_C(t)\rangle_{T_s}$, can be found from Fig.1 as

$$\langle i_C(t)\rangle_{T_s} = \frac{1}{2}\left[D_2 i_{L1pk}(t) - D_1 I_{L2pk}\right] \tag{8}$$

Equation (7) must be equal to zero at steady state. Substituting (8) into (7) and solving for V_C give

$$V_C = \frac{V_O}{2}\left[\sqrt{1+\frac{2L_2}{L_1M^2}}+1\right] \tag{9}$$

Where $M=V_0/V_m$ is the voltage conversion ratio. Thus, for a given value of M, capacitor voltage V_C is independent of load current variation, and it is a function of inductance ratio L_1/L_2. This effect was first reported in [4]. Since then, several studies about this effect have been reported in the literature [6], [7], [19], and [24].

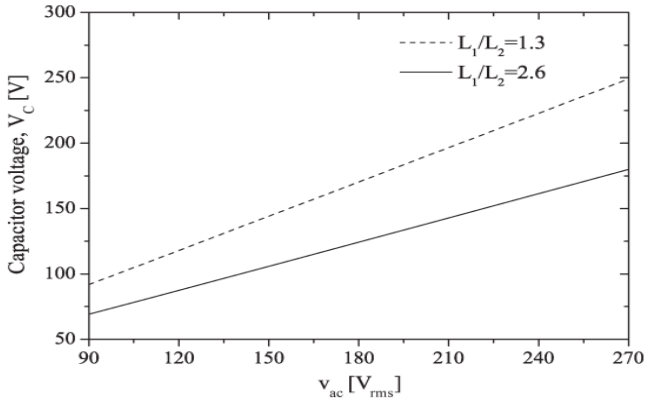

Fig. 5 Capacitor voltage V_C as a function of ac line voltage v_{ac} (V_0=24, and L_1 and L_2 are in DCM).

Fig. 5 shows the variation in capacitor voltage V_C as a function of line voltage v_{ac}, with the ratio L_1/L_2 as a parameter. It is clear from Fig. 5 that higher values of inductance ratio L_1/L_2 tend to reduce the voltage stress on capacitor C and, hence, on power switch S_1. This is true since the capacitor charging and discharging currents are inversely proportional to L_1 and L_2, respectively. Moreover, from Fig. 5, when L_1/L_2=2.6, voltage V_C is about 69 V at low-line input voltage and about 177 V at high-line input voltage. Therefore, a 600V power metal–oxide–semiconductor field-effect transistor switch suffices.

However, increasing the value of L_1/L_2 beyond a certain value will force L_1 to leave the DCM region, which will degrade the quality of the input line current. Thus, there is an upper bound limit for ratio L_1/L_2, which can be found from (5), (6), and (9) as

$$\frac{L_1}{L_2} \le \frac{1}{2M} \tag{10}$$

From (10), the upper bound limit of L_1/L_2 is determined by the output voltage and low-line ac voltage.

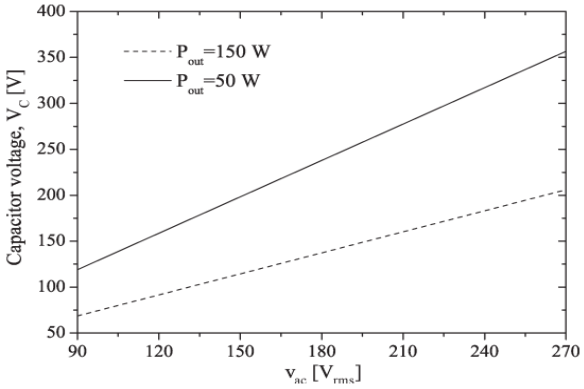

Fig. 6 Capacitor voltage V_C as a function of ac line voltage v_{ac} (V_0=24V, f_s=50KHz, L_1 =66µH, and L_1 in DCM and L_2 in CCM).

For the sake of comparison, when L_2 operates in CCM, then V_C depends on both line voltage v_{ac} and load power P_{out}, and is given by

$$V_C = \frac{V_m}{2}\sqrt{\frac{R_L}{f_s L_1}} \tag{11}$$

A plot of (11) for two different output power levels is shown in Fig. 6. Nevertheless, the voltage stress on capacitor C is still below 450 V for load variation from full load to one third of full load. Furthermore, when L_2 is in BCM, then duty cycle D_1can be obtained from (6) and (9) as

$$D_1 = \frac{V_0}{V_C} = \frac{L_1M^2}{L_2}\left[\sqrt{1+\frac{2L_2}{L_1M^2}}-1\right] \tag{12}$$

Equation (12) shows that D_1 is independent of load current variation, yet it must be kept constant for a given value of M.

This implies that the switching frequency must vary in order to compensate for load current variation. Fig. 7 shows the variation of duty cycle D_1 as a function of ac line voltage for different values of inductance ratio L_1/L_2.

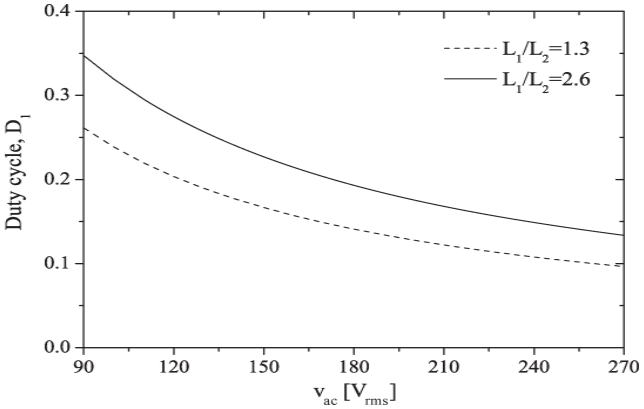

Fig. 7 Variation of duty cycle D_1 as a function of ac line voltage v_{ac} (V_0=24V, L_1 in DCM and L_2 in BCM).

C. Voltage Conversion Ratio M

The voltage conversion ratio $M=V_0/V_m$ in terms of circuit parameters can be found by applying the input–output power balance principle to the circuit in Fig. 1. The average input power during one half-cycle of the line voltage is

$$\langle P_{in}(t)\rangle_{T_L/2} = \frac{2}{T_L}\int_0^{T_L/2} v_i \langle i_{in}(t)\rangle_{T_S} dt \qquad (13)$$

From Fig. 4, the average input line current over one switching period $\langle i_{in}(t)\rangle_{T_s}$ is

$$\langle i_{in}\rangle_{T_s} = \frac{1}{2} D_1 i_{L1pk}(t) = \frac{v_i}{R_e} \qquad (14)$$

where R_e is the emulated input resistance of the converter, and it is equal to

$$R_e = \frac{2L_1}{D_1^2 T_s} \qquad (15)$$

For a given operating point (M,R_L), the emulated input resistance in (15) is constant if both D_1 and T_s are kept constant. Thus, the converter presents a linear resistive load to the ac power main, which is the perfect condition for unity power factor (UPF) operation. Evaluating (13) and applying the power balance between the input–output ports, the desired voltage conversion ratio M is

$$M = \sqrt{\frac{\eta}{2K}} D_1 \qquad (16)$$

where η is the converter efficiency, and the dimensionless parameter K is defined by

$$K = \frac{2L_1}{R_L T_s} \qquad (17)$$

D. Inductances L_1 and L_2

The critical value of $K(K_{crit})$ required for L_1 to be in DCM is found by rearranging (5) and (16), which gives

$$K_{crit} = \frac{1}{2}\left(\frac{1-D_1}{D_1}\right) \qquad (18)$$

For values of $K \le K_{crit}$, then L_1 is operating in DCM; otherwise, L_1 will enter the CCM region. Note that the proposed converter has a wider range of voltage conversion ratio when it is compared to the conventional buck–boost converter, which has $K_{crit} = (1-D_1)^2/2$.

The critical value of $L_1(L_{1,crit})$ required for DCM operation occurs at maximum output power $R_{L,min}$ and at the peak of the low-line voltage $V_{m,min}$. Using (16) –(18) gives $L_{1,crit}$ as

$$L_{1,crit} = \frac{R_{L,min} T_{s,max}}{16}\left[-1+\sqrt{1+\frac{4V_{m,min}}{V_0}}\right]^2 \qquad (19)$$

For values of $L_1 > L_{1,crit}$, the converter enters the CCM region, where (16) is no longer valid. In CCM, there are only two operating stages per switching cycle, i.e., Fig. 3(a) and (b). The voltage conversion ratio in CCM can be expressed by $M = 2D_1^2/[\pi(1-D_1)]$, which can be derived by equating the average capacitor current during a half-cycle to zero and applying the power balance between the input–output ports. However, operating L_1 in the CCM region results in a more distorted input line current and a lower input power factor than in the DCM region. The best choice for the value of L_1 is to be close to $L_{1,crit}$ since this will reduce the ripple value of input current i_{in}.

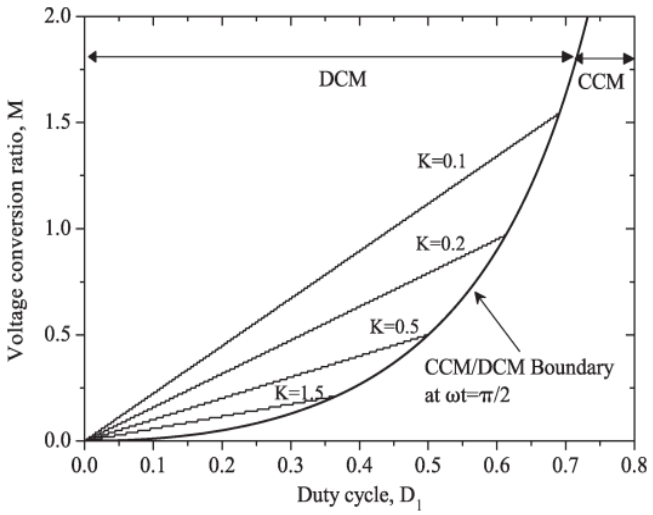

Fig. 8 Voltage conversion ration M as a function of duty cycle D_1 for several values of K

The DCM characteristic is plotted in Fig. 8 for several values of K. Note that the CCM/DCM boundary line in Fig. 8 is valid for ωt=π/2, i.e., when $v_i=V_m$, which gives the minimum required value of K_{crit}.

Similarly, the condition for inductor L_2 to operate in DCM occurs when the average output current $\langle i_{L2}\rangle_{T_s} \le I_{L2,pk}/2$, Fig. 1. Thus, the minimum value of $L_2(L_{2,crit})$ can be found as

$$L_{2,crit} = \frac{R_{L,min} T_{s,max}}{2} \times \left[1 - \frac{V_0}{2V_{m,min}}\left(-1+\sqrt{1+\frac{4V_{m,min}}{V_0}}\right)\right] \qquad (20)$$

For L_2 to operate in BCM, then the value of L_2 must be equal to $L_{2,crit}$.

E. Averaged Circuit Model

The averaged model for the converter of Fig. 1 when both inductors L_1 and L_2 are in DCM is derived here based on averaging various waveforms over one switching cycle T_s. The averaged diode D_x and D_y currents are given by

$$\langle i_{Dx}\rangle_{T_s} = \frac{V_i^2}{V_C R_e} = \frac{\langle p_{ac}(t)\rangle_{T_s}}{v_C} \qquad (21)$$

$$\langle i_{Dy}\rangle_{T_s} = \frac{V_0^2}{\eta R_L v_C} = \frac{\langle p_{ac}(t)\rangle_{T_s}}{\eta v_C} \qquad (22)$$

and the average voltage across output diode D_F is equal to

$$\langle v_{DF}\rangle_{T_s} = G_0 v_C \qquad (23)$$

where G_0 is given by

$$G_0 = \frac{\eta L_1 R_L}{2L_2 R_e}\left[\sqrt{1+\frac{4L_2 R_e}{\eta L_1 R_L}} - 1\right] \qquad (24)$$

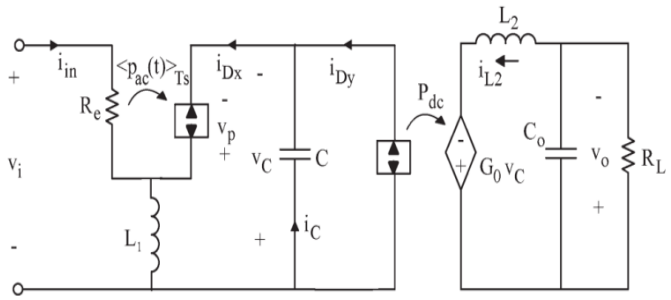

Fig. 9 Averaged circuit model in DCM (Both L_1 and L_2 are in DCM).

By using (14) and (21)–(23), a complete averaged model for the proposed PFC can be obtained, as shown in Fig. 9, which is based on the "Loss-Free-Resistor" concept presented in [30] and [32]. Note that if this model is implemented by MATLAB, then a large resistor must be inserted across capacitor C to avoid floating problems. Moreover, the power sources elements in Fig. 9 can be modelled in MATLAB as a "voltage-controlled current source." Moreover, the model is also valid when L_2 operates in CCM, provided that coefficient G_0 is replaced by duty cycle D_1.

From Fig. 9, capacitor current i_C can be written as

$$C\frac{dv_C(t)}{dt} = \frac{v_i^2(t)}{R_e v_C(t)} - G_0^2\frac{v_C(t)}{\eta R_L} \tag{25}$$

Eliminating the intermediate steps, the exact expression for the capacitor voltage is obtained as

$$v_C(t) = [-(B_0 + B_1)e^{-yt} + B_0 + B_1 cos(2\omega_L t) + B_2 sin(2\omega_L t)]^{1/2} \tag{26}$$

Where

$$y = \frac{2G_0^2}{\eta R_L C} \qquad B_0 = \frac{P_{dc}R_L}{\eta G_0^2}$$

$$B_1 = \frac{-B_0}{1 + \left(\frac{\omega_L R_L C}{G_0^2}\right)^2} \qquad B_2 = \frac{\omega_L R_L C}{G_0^2} B_1$$

The peak–peak low-frequency voltage ripple on capacitor C can be evaluated from (26) as

$$\Delta v_{C,p-p} = \sqrt{B_0 - B_2} - \sqrt{B_0 + B_2} \tag{27}$$

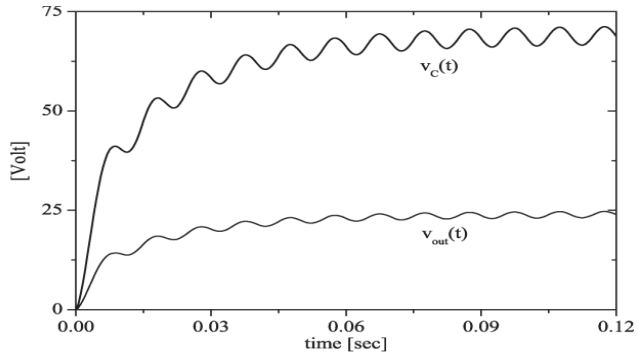

Fig. 10 Turn-on transient waveforms

The time-variant expression for output voltage $v_0(t)$ and the peak–peak low-frequency output voltage ripple can be simply obtained by multiplying both (26) and (27) by coefficient G_0. The maximum peak voltage ripple of v_C occurs at low-line voltage and at maximum power throughput. Theoretical transient waveforms are plotted in Fig. 10 for the following values: V_i=90Vrms at 50Hz, P_0=150W, V_0=24V, L_1/L_2=2.6, and C=1.5mF.

IV. Simulation Results

The converter of Fig. 1 is simulated using MATLAB for the following input and output data specifications:

- input voltage: 110 Vrms at 50 Hz;
- output voltage: 20 V ±2%;
- maximum load power: 50 W;
- minimum switching frequency: 60 kHz.

Input inductor L_1 is designed for the DCM operation, whereas L_2 is designed for the BCM operation. The circuit components are calculated based on the analysis performed in previous sections, and they are given as L_1=100μH, L_2=$L_{2,crit}$=47μH,C=680μF and C_o=100μF. Duty cycle D_1 is set to 0.22. A high-frequency input filter (L_F=2mH, and C_F=0.68μF) is inserted after the bridge rectifier to filter the ripples in the rectified line current. MATLAB actual semiconductor models have been used to simulate the switches: IRF840 for the active switch and MUR1560 for the diodes. The simulated waveforms shown in Fig. 11 are for the converter without controlled switch, which correctly demonstrates the DCM/BCM operating mode. The simulation result gives a total harmonic distortion in the input line current of about 1%. Moreover, it is clear from Fig. 11(c) that output voltage V_o has a significant low-frequency ripple, which is unacceptable for some specific applications. The low-frequency ripple in V_o can be greatly reduced by simply regulating the output voltage. Therefore, a simple feedback controller has been implemented to regulate V_o at 20 V.

The converter of Fig. 2 is simulated using MATLAB with same circuit parameters as mentioned for Fig. 1. In this simulation we will provide an extra feedback path from the load to the switch, so that the switch can operate according to the load variation. For automatic control of the switch according to the load variation we will control the gate triggering pulses. For the control of the gate pulses we use the PI controller and PWM technique in the feed-back path. The PI controller used is discrete type and the proportional gain is taken as 0.01 and the integral gain is considered as zero. In the PWM generator the reference signal used is a triangular wave.

The simulated waveforms shown in Fig. 12 are for the converter with controlled switch. The Fig. 12(a) shows the input voltage and current waveforms and the Fig. 12(b) shows the voltage across the capacitor. The output voltage waveform is shown Fig. 12(c) and the output current waveform is almost similar with output voltage waveform. The gate triggering pulses generated by a PWM generator was shown in Fig. 12(d). These gate pulses are generated according to the load variation.

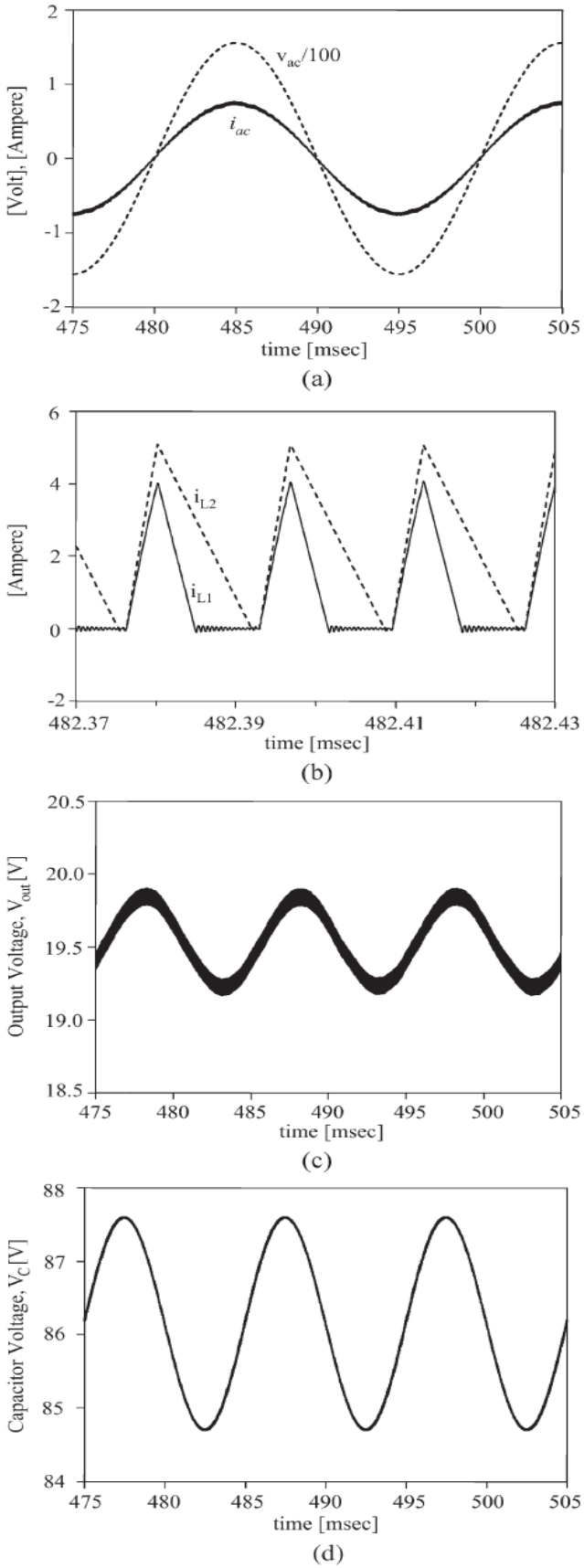

Fig. 11 MATLAB simulated waveforms for the converter without controlled switch

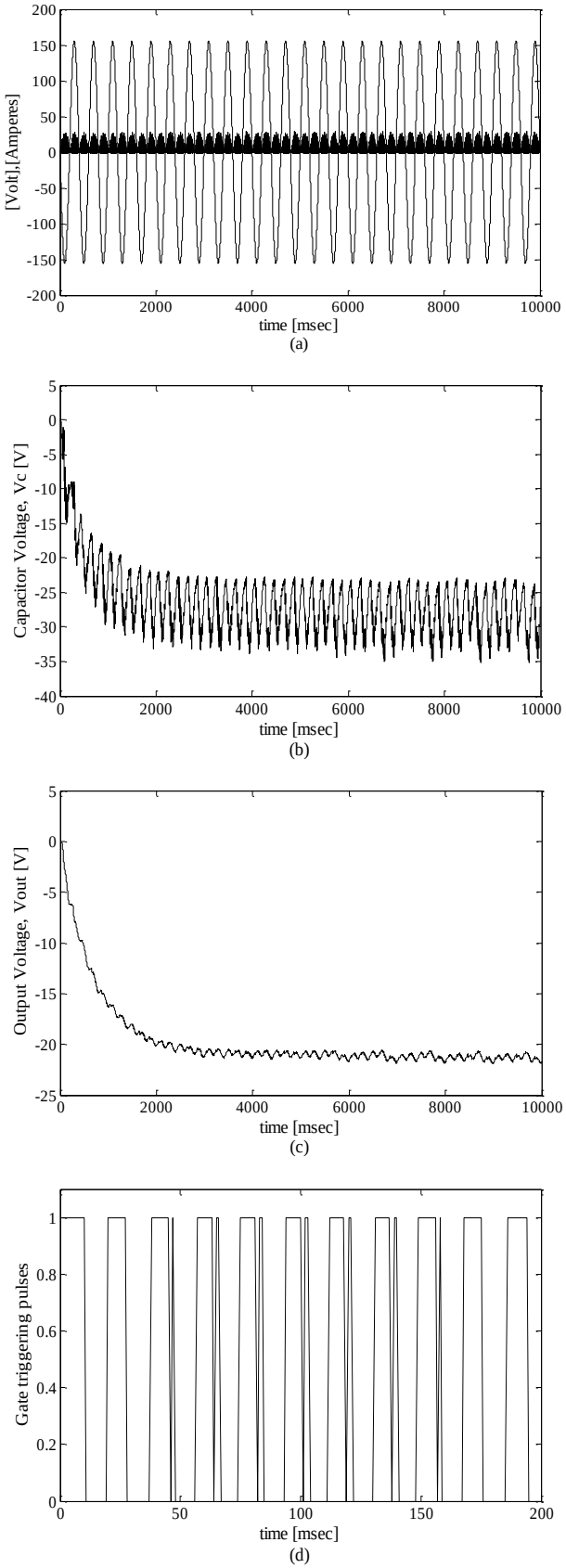

Fig. 12 MATLAB simulated waveforms for the converter with controlled switch

V. Conclusion

In this paper, the converters topologies have been proposed by combining a buck–boost and a buck converter. As a result, a single switch single-stage UPF capability is obtained from the converter without controlled switch. The steady-state behaviour of the converters has been theoretically analysed with performance characteristics, and a large-signal averaged model is presented. It has been shown that several advantages can be obtained by operating both input and output inductors in the DCM. These advantages include automatic PFC, low voltage stress on the semiconductor components, zero-current switch turn-on, and a well-regulated output voltage with a small low-frequency voltage ripple. A converter model is also proposed for the requirement of controlling the switch according to the load variation, but the switch suffers a small amount of stresses. Moreover, the converters are well suited for universal-line PFC applications.

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