Design of Speed and Area Efficient 16-bit pipelined RISC with Harvard Architecture

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Abstract*— This research work is devoted to design speed and area optimized fully functional 16-Bit 5 phased pipelined harvard RISC processor. All of us know that there are two types of processors mainly available in the market; those are RISC (Reduced Instruction Set Computer) and CISC (Complex Instruction Set Computer). RISC and CISC processors were always the hot topics of debate, but still no conclusion has been drawn till now, that which one better is than another. RISC is advantageous in many aspects than the CISC processor as it uses reduced or small number of instructions to perform any action than CISC processors does. RISC processor is a digital processor which is called as the heart of the many digital devices. By optimizing speed and area of this processor, overall efficiency of those digital devices can be enhanced which are mainly based upon this processor. RISC processor works upon harvard architecture. In harvard architecture program and data are separated so that different data width can be chosen. Along with this digital signal processors can execute most instructions in one clock cycle. This is due to the strong, additional parallelism in the hardware structure maintained using pipelining. But there is always a problem of stalling in pipeling with RISC that is resolved using Harvard register Architecture (also having minimal structural and data flow hazards). To remove this issue a LIFO stack (8bit width) is inserted, which in the routine receives the data prior to the entry (subroutine interrupt). Another method that has been used is to save the register and the jump address when a subroutine call or an interrupt request occurs. We also have used register shadowing to save register.

To design proposed RISC Processor VHDL hardware description language (HDL) has been used. To design operational sub-modules data flow modeling and to integrate these modules behavioral modeling style has been used. For this design the target FPGA belongs to Spartan-3E (family), XC3S500E (device), PQ208 (package) with speed grade of -5. For synthesis purpose Xilinx synthesis tool (XST) of Xilinx ISE-9.2i has been used. For the behavioral simulation purpose ISE simulator has been used.

***Keyword*- RISC processor, Xilinx-ISE9.2i.**

I. INTRODUCTION

Today in the digital domain world digital signal processing is of main concern, whose performance is mainly dependent upon the processors' speed. Processor parameter optimization can also provide the Digital Signal Processors' performance optimization, and pipelining is the main key element in RISC processor to have the parallelism. Digital Signal Processors can execute most instructions in one clock cycle. This is due the strong additional parallelism in the hardware structure. But in stalling is always the main problem with pipelining. With these considerations, it is always important to have fast and efficient mechanism to implement those methodologies through the use of which the problem of pipeline can be removed.

To increase the processing speed, there are different methods. If the clock frequency increases, increases linearly to the performance of the processor. Occurring disorders and heat problems can complicate this "simple" method very quickly.

An elegant way is also applied to RISC processors, is pipelining. In pipelining different phases of the commands are pushed over each other in time. This is only possible, if the various phases take various hardware blocks. There are five phases on the basis of which various operations are performed in the RISC processor.

1. IF--Instruction fetch from memory load to a register
2. Reg--Read register while instruction is decode.
3. EX--Run the operation or calculate the address
4. DA--Data Access to an operand in Data Memory
5. WB--Write Back result to a register

II. LITERATURE SURVEY

In [1] Mr. Raman Deep Kaur, has designed 8-bit RISC processor with 16 instruction set. In which Every instruction has been executed in one clock cycle with 3 stage pipelining. In [2], Mr. M.K. Jain et.al. has shown that microprocessor is a general purpose IC which follows the instructions given to it, and the instructions set for the microprocessor designed such a way that it can handle any type of computations. In [3], Mr. Vivek Dubey et.al. has aimed to reduce the area requirements than the conventional RISC processor architecture and to support powerful CISC instruction set. In [4] has author have presented design of a single cycle 16-Bit non-pipelined RISC processor for its application towards convolution application. Novel adder and multiplier structures has been employed in the RISC architecture. The processor has been designed for

executing the instruction set comprising of 27 instructions in total, which is expandable up to 32 instructions, based on the user requirements. The processor design promises its use towards any signal processing applications. In [5], an 8-bit RISC processor with 16 instruction set has been designed. Every instruction is executed in one clock cycles with 3-stage pipelining. This paper has worked upon area and power dissipation optimization. In [6], A 16-bit RISC processor harvard based architecture has been designed that utilizes minimum functional units. In [7], has shown design implementation and testing of the 16-bit RISC processor. In [8], 32bit RISC Processor core has been design and implemented in hardware using VHDL. In [10], 9 bit RISC Processor core has been design and simulated using verilog. Most of the goals were achieved and simulation. Every instruction is executed in one clock cycles with 4-stage pipelining. The design is verified through simulations.

III. PROPOSED RISC PROCESSOR

Before designing the proposed RISC processor we have shown that how will it look and work when we would place it inside the FPGA board. That is shown as follows:-

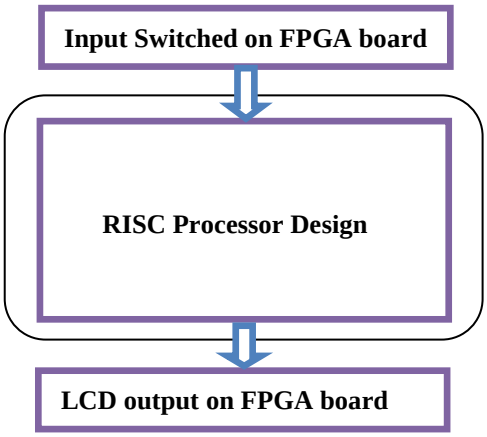

Figure 1 RISC processor on FPGA board

Proposed fully functional 16-bit 5 phase pipelined Harvard RISC processor supporting MIPS instruction set, is shown as below, following diagram we have designed on the paper and placed as it is, to maintain uniqueness, along with this the diagram shown below is self-explanatory in itself: -

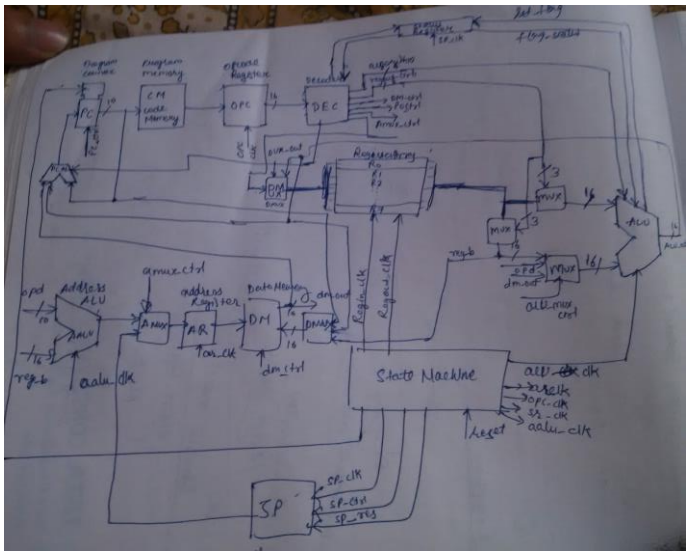

Figure 2 Proposed RISC Processor Block Diagram

Register Transfer Level top-view for the above maintained block diagram is given in the following, in this all components has not been included. We have include only those components which are really necessary to show, so that bulkiness of diagram can be reduced:-

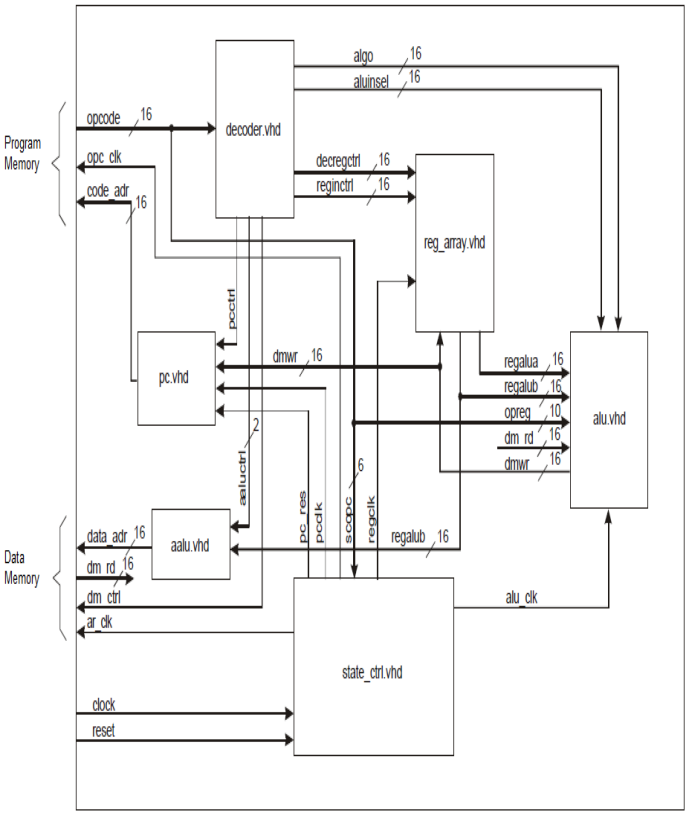

Figure 3 RTL top-view of the Proposed RISC processor

To remove the stall problem of pipelining, feed-forward path is used. Diagram for same is given in the following:-

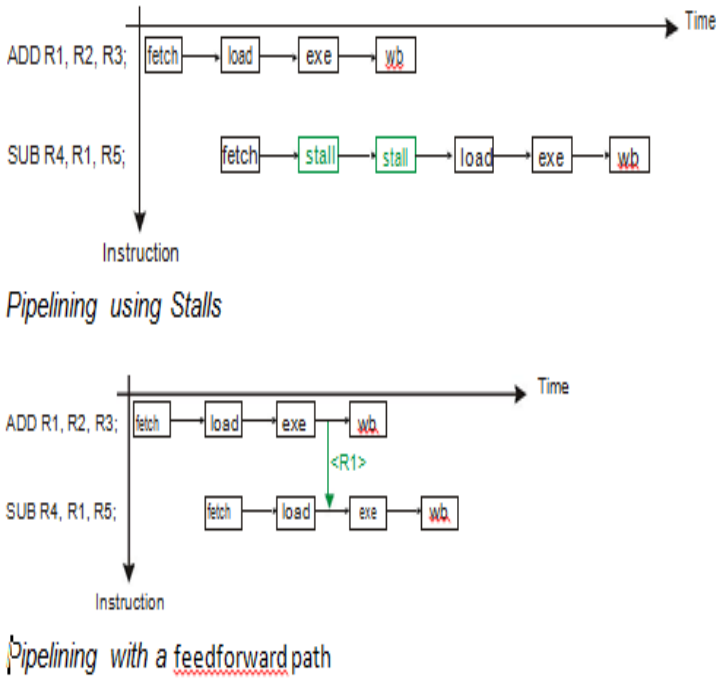

Figure 4 Proposed RISC Processor Pipeline with Feed-Forward path

State machine for our proposed RISC processor is given in the following:-

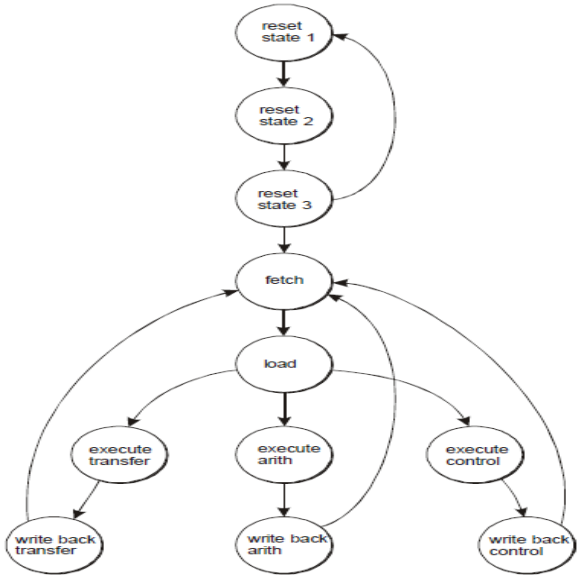

Figure 5 Proposed RISC Processor Pipeline with Feed-Forward path

Timing behavior for our proposed RISC processor is given in the following:-

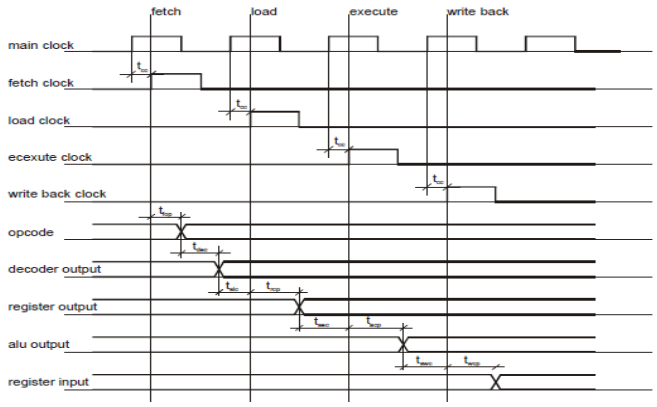

Figure 6 Proposed RISC Processor Pipeline with Feed-Forward path

Methods which we have used to improve the timing response:-

1. Manually Routing.
2. Changing the hardware structure (Xilinx foundation).

IV. SIMULATION AND SYNTHESIS RESULTS OF THE CPU

1. Simulation Results:-

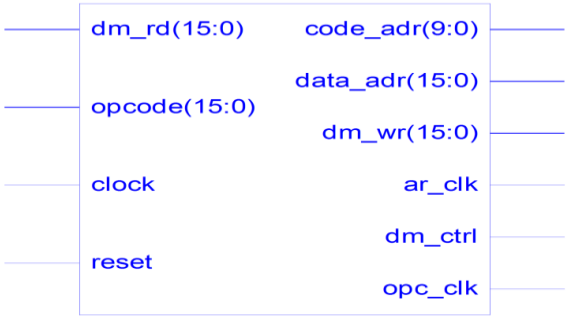

Figure 7 Processor's RTL Schematic Top-View

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	85	1,536	5%	
Number of 4 input LUTs	545	1,536	35%	
Logic Distribution				
Number of occupied Slices	350	768	45%	
Number of Slices containing only related logic	350	350	100%	
Number of Slices containing unrelated logic	0	350	0%	
Total Number of 4 input LUTs	641	1,536	41%	
Number used as logic	545			
Number used as a route-thru	32			
Number used for Dual Port RAMs	64			
Number of bonded IOBs	79	124	63%	
IOB Flip Flops	2			
Number of MULT18X18s	1	4	25%	
Number of GCLKs	4	8	50%	
Total equivalent gate count for design	13,100			
Additional JTAG gate count for IOBs	3,792			

Figure 8 Device Utilization Summary of Proposed RISC Processor

2. Synthesis Results:-

Minimum period: 5.892ns (Maximum Frequency: 169.714MHz)

Minimum input arrival time before clock: 16.307ns

Maximum output required time after clock: 14.182ns

Maximum combinational path delay: 16.491ns

V. APPLICATION

The RISC processor can be used in almost all places where the digital signal processors are used. Along with that it can be used in signal processing and image processing too.

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