

SPEED CONTROL OF INDUCTION MOTOR DRIVE USING SEVEN LEVEL DIODE CLAMPED INVERTER

K.Hari, K.Kishore Reddy

Abstract: The main aim of this paper is to control the speed of an induction motor by using seven level diode clamped inverter. To obtain quality of sinusoidal output voltage with reduced THD. The proposed Scheme for seven level inverter is multicarrier SPWM control. Speed control can be achieved by using constant V/f method. This constant V/f method can be implemented by changing the supply voltage and frequency applied to the induction motor at constant ratio. This system is replacement for the conventional method which has high THD and high switching losses, it results a poor drive performance. This simulation result shows the effectively control the motor speed. The performance of the drive can be validated using SPWM technique in terms of Total Harmonic Distortion (THD). The effectiveness of this system is verified through using MATLAB Simulink.

Keywords – Diode clamped multilevel inverter; induction motor; Multicarrier PWM technique; THD; Constant V/f method.

I. Introduction

An induction motor being rugged, reliable, and comparatively inexpensive makes it additional preferred in most of the industrial drives. There are chiefly used for constant speed applications because of inconvenience of the variable-frequency supply voltage. However several applications are in would like of variable speed operations. In early days, mechanical gear systems were used to acquire variable speed. Recently, power physics and control systems have matured to permit these elements to be used for control in place of mechanical gears. These electronics not solely management the motor's speed, however will improve the motor's dynamic and steady state characteristics. Adjustable speed ac machine system is supplied with an adjustable frequency drive that an influence device for speed management of an electrical machine. It controls the speed of the electric machine by changing the mounted voltage and frequency to adjustable values on the machine aspect. High power induction motor drives exploitation classical three phase converters have the disadvantages of poor voltage and current qualities. To boost these values, the shift frequency has to be raised that causes further shift losses. Another possibility is to place a motor input filter between the devices and motor, that causes further

weight. The diode clamp method will be applied to higher level converters. As the number of level will increase, the synthesized output wave shape adds additional steps, manufacturing a stairs wave shape. A zero harmonic distortion of the output wave will be obtained by an infinite variety of levels.

II. Drive System Description

In the standard technique traditional PWM methodology is employed. so the voltage and current is of poor qualities and therefore the shift frequency causes additional quantity of shift losses. Those drawbacks square measure corrected exploitation 3 section diode clamped structure electrical converter. The voltage and current quality square measure higher and therefore the shift losses square measure reduced compared to the standard technique.

A. Structure of Seven Level Diode Clamped Multilevel Inverter

The seven-level neutral point-clamped voltage supply electrical converter is shown in Fig one. It contains thirty six unidirectional active switches and thirty neutral purpose clamping diodes. The center purpose of the half dozen capacitors "n" will be outlined because the neutral purpose.

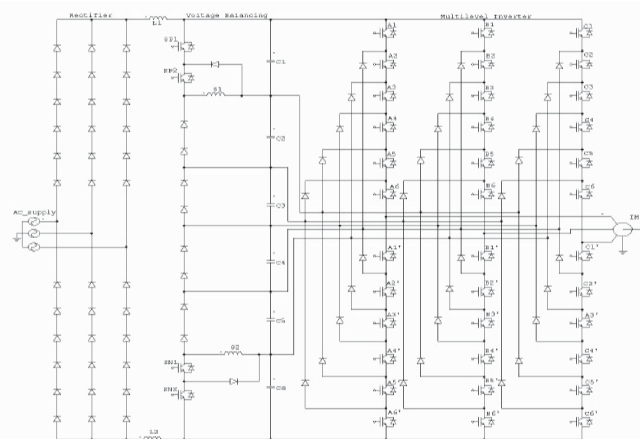


Fig 1. Seven level inverter based drive circuit

The foremost advantage of this configuration is each switch must block only one-half of the dc link voltage ($V_{dc}/6$). In order to produce seven levels, exclusively 2 of the twelve switches in every section leg ought to be turned on at any time. The dc-bus voltage is split into three levels by two series-connected bulk capacitors, C_a and C_b , via. They are same in rating. The diodes all are same to provide the voltage sharing equally and clamp the voltage level at across the switch, when the switch at off position. By this given structure provides less voltage stress at across switch.

B. Principle of operation of seven level inverter

The voltage levels and switch states are shown in table. If the switch is on then state condition is 1, if the switch is off then state condition is 0. There are two alternate switch pairs in every phase. The pairs in one leg are (A_1, A_1') , (A_2, A_2') , (A_3, A_3') , (A_4, A_4') , (A_5, A_5') , (A_6, A_6') .if one of the switch pair is on state, the other of same pair must be off state.

TABLE 1

Output voltage level and its switching states

Voltage V_{ao}	Switch State											
	A ₁	A ₂	A ₃	A ₄	A ₅	A ₆	A _{1'}	A _{2'}	A _{3'}	A _{4'}	A _{5'}	A _{6'}
V7	1	1	1	1	1	1	0	0	0	0	0	0
V6	0	1	1	1	1	1	1	0	0	0	0	0
V5	0	0	1	1	1	1	1	1	0	0	0	0
V4	0	0	0	1	1	1	1	1	1	0	0	0
V3	0	0	0	0	1	1	1	1	1	1	0	0
V2	0	0	0	0	0	1	1	1	1	1	1	0
V1	0	0	0	0	0	0	1	1	1	1	1	1

For produce a staircase output, considering one leg of inverter. The process for synthesize the seven level voltages are

- If turn on all upper half switches A_1, A_2, A_3, A_4, A_5 and A_6 then the output voltage level $V_{ao}=V_{dc}$
- If turn on upper half switches A_2, A_3, A_4, A_5, A_6 and lower switch A_1' then the output voltage level $V_{ao}=5V_{dc}/6$
- If turn on lower half switches A_3, A_4, A_5, A_6 and A_1, A_2' then the output voltage level $V_{ao}=4V_{dc}/6$
- If turn on lower half switches A_4, A_5, A_6 and A_1', A_2', A_3' then the output voltage level $V_{ao}=V_{dc}/2$
- If turn on lower half switches A_5, A_6 and A_1', A_2', A_3', A_4' then the output voltage level $V_{ao}=V_{dc}/3$

- If turn on lower half switches A_6 and $A_1', A_2', A_3', A_4', A_5'$ then the output voltage level $V_{ao}=V_{dc}/6$
- If turn on all lower half switches $A_1', A_2', A_3', A_4', A_5'$ and A_6' then the output voltage level $V_{ao}=0$

The features of multilevel inverters

- It may be easier to design high voltage, high power inverters
- If number of voltage levels increases then the harmonic content in output voltage is decreases
- Due to better spectral performance filtering components will less required
- No EMI problem in MI due to it operate at low switching frequency
- It have higher efficiency

III. Proposed Scheme

The block diagram of multilevel inverter fed three phase induction motor shown in Fig. The whole system will have of two sections they are a power circuit and a control circuit. The power segment consist a rectifier, filter capacitor, and diode clamped multilevel inverter. And the motor is associated with multilevel inverter. Ac input voltage is fed to a three phase diode bridge rectifier, in order to generate dc output voltage across the capacitor filter. An capacitor filter will terminates the ripple contents in dc output voltages. Then the pure dc voltage is supplied to the three multilevel inverter throughout capacitor filter. The structures of multilevel inverter have 12 MOSFET switches in each single leg. This are restricted in order to produce an ac output voltage. This output ac voltage can be controlled in both magnitude and frequency (constant V/f open loop control). Then the controlled ac output voltage is feed to the induction motor drive. Whenever the switches are ON state then the current will flows from the dc bus to the motor winding.

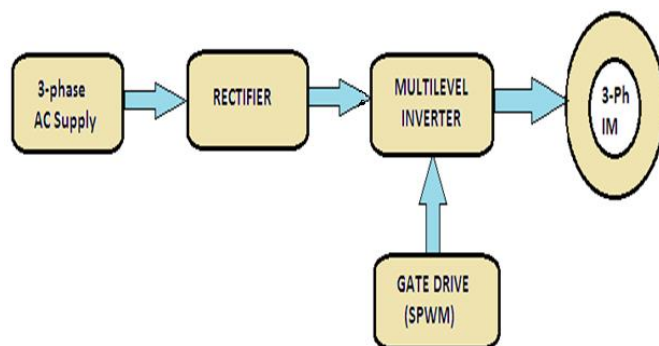


Fig 2 Basic Block diagram

The motor windings is highly inductive, it can grip electric energy in the form of current. While switches are

off state that current will needs to be dissipated. By the Diodes which are connected across the switches its give a path for the current to dissipate when the switches are off. Those diodes are called as freewheeling diodes.

IV. Modulation Strategy

In this Paper mostly focuses on multicarrier SPWM method. SPWM method is easy and more flexible compare with Space Vector Modulation methods. In this method uses several triangular or ramp carrier signals and keep only one modulating sinusoidal signal. For n-level inverter is in use, n-1 carriers will be needed. This carrier singles have the same frequency WC and the same peak to peak amplitude Ac. The zero reference is placed within the middle of the carrier set. At every instantaneous each carrier single is compared with modulating signal. . Every comparison offers 1(-1) if the modulating signal is larger than (lower than) the triangular carrier within the initial (second) half the elemental amount, zero otherwise. The results are more to administer the voltage level that is needed at the output terminal of the electrical converter. Multicarrier PWM methodology may be classified into 2 groups: 1) Carrier Disposition methodology 2) phase shifted PWM methodology.

- APOD, where each carrier band is shifted by 180° from the adjacent bands
- POD, where the carriers above the zero reference are in phase, but shifted by 180° from those carriers below the zero reference.
- PD, where all the carriers are in phase.

Advantages of multicarrier PWM Techniques

- To distribute the switching signals properly so as to attenuate the switching losses
- Implement is simple
- Extensible to high number levels

In this paper the gating pulses for switches are generated by using In-phase disposition technique.

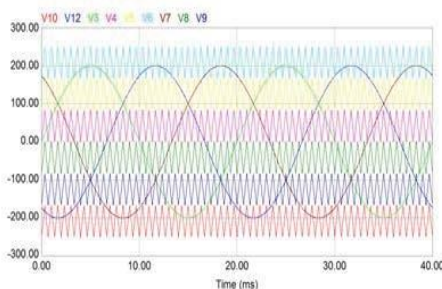


Fig 3 In-Phase disposition technique

A. Modulation Index

$$MI = \frac{A_m}{\left(\frac{N-1}{2}\right) * A_c}$$

N=number of levels, A_m =Modulating signal Amplitude, A_c =Carrier Signal Amplitude

B. V/f Control Theory

The relation between the voltage and torque versus frequency shown in fig. The voltage and frequency being enlarged up to the bottom speed. At base speed, the voltage and frequency reach the rated values. We are able to drive the motor on the far side base speed by increasing the frequency any. However the voltage applied cannot be enlarged on the far side the rated voltage. Therefore, only the frequency is often enlarged, which ends up within the field weakening and therefore the force availability being reduced. Above base speed, the factors governing force become complicated, since friction and windage losses increase considerably at higher speeds. Hence, the force curve becomes nonlinear with relation to speed or frequency.

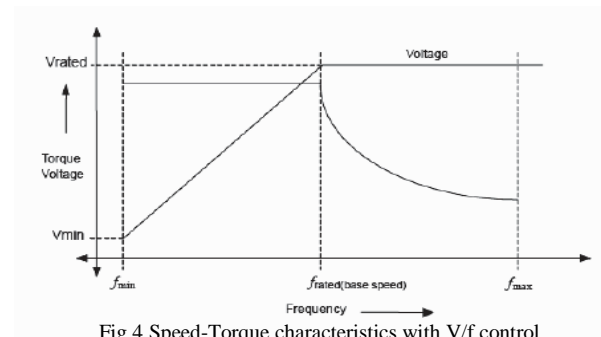


Fig 4 Speed-Torque characteristics with V/f control

V. Simulation Circuits and Waveforms

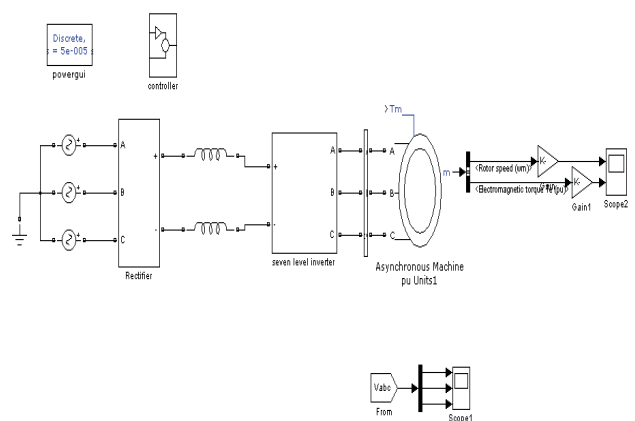


Fig 5 Induction Motor Drive using Seven Level Inverter Simulation Diagram

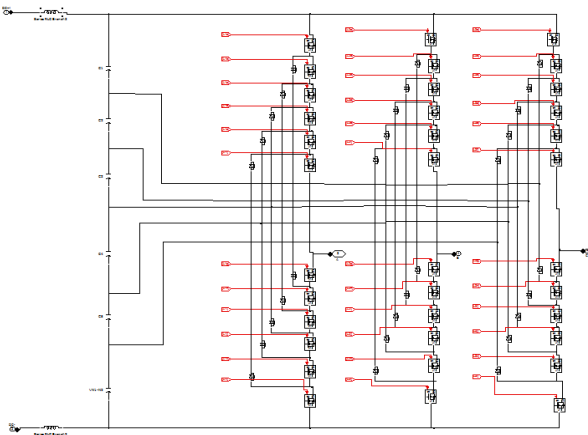


Fig 6 Seven level inverter sub circuit

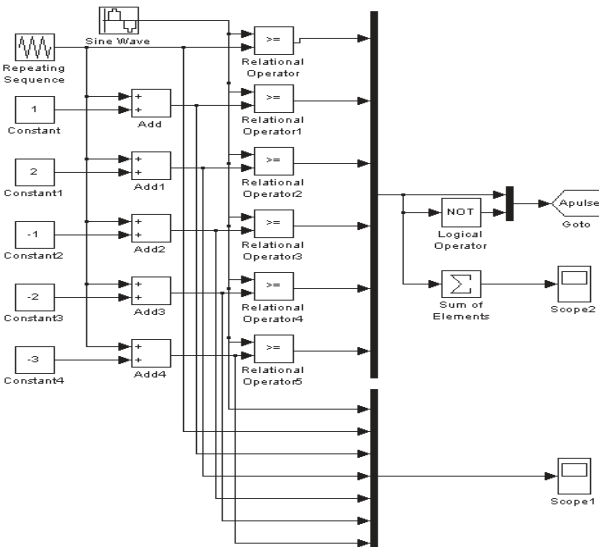


Fig 7 Multi carrier SPWM simulation circuit

Output Voltage for 50HZ and 45HZ frequency are shown in 8 and 11

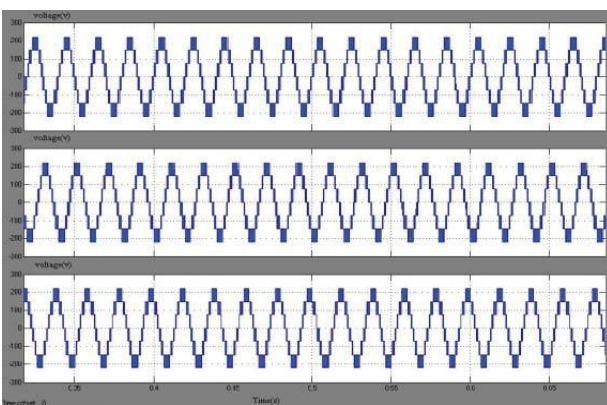


Fig 8 Output Phase Voltage for 50HZ Frequency

Speed-Torque curves for 50HZ and 45HZ frequencies are shown in figure 9 and 12

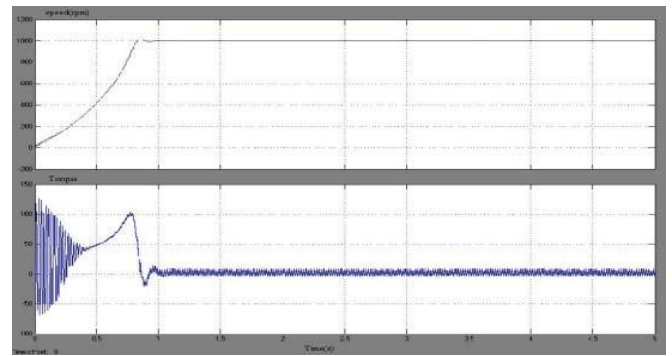


Fig 9 Speed-Torque Curves for 50HZ Frequency

The output voltage FFT plot is shown in figure 10.

This plot shows that the harmonic content in attendance in output voltage.

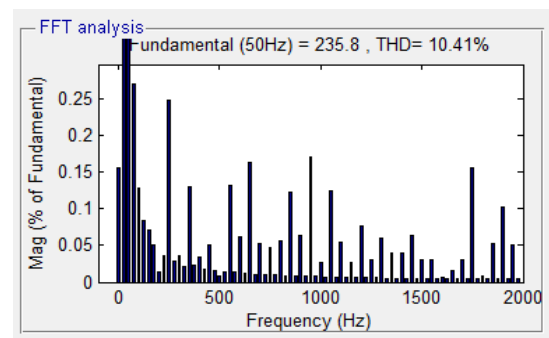


Fig 10 FFT for Output voltage

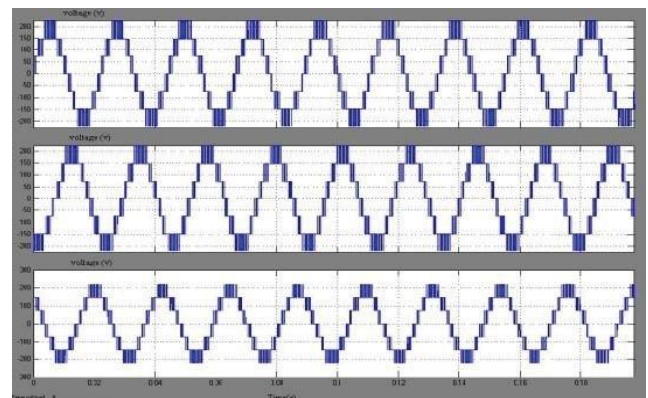


Fig 11 Output Phase voltage for 45HZ Frequency

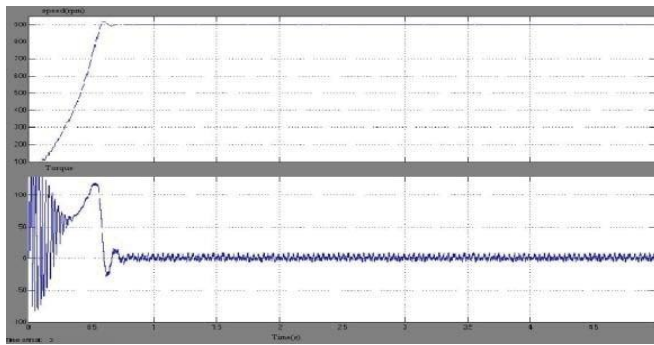


Fig 12 Speed-Torque Curves for 45HZ Frequency

By varying the voltage and frequency, the motor Speed-Torque characteristics are varied, simultaneously the motor speed also varies.

VI. Conclusion

In this paper, the performance of the three-phase Diode Clamped Seven-level inverter is studied. The inverter has been simulated and improved by employing SPWM control scheme. The use of seven-level converters reduced the harmonic components of the line to line voltage compared with the other-level converter at the same device switching frequency.

REFERENCES

- [1] S. Malik and D. Kluge, "ACS 7000 world's first standard ac drive for Medium-voltage applications," *ABB Rev.*, no. 2, pp. 4–11, 2006.
- [2] H. Natchpong, Y. Kondo, and H. Akagi, "Five-level diode clamped PWM converters connected back-to-back for motor drives," *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1268–1276, Jul./Aug. 2008.
- [3] T. S. Key and J. S. Lai, "IEEE and international harmonic standards impact on power electronic equipment design," in *Conf. Rec. IEEE IECON*, Nov. 2005, vol. 2, pp. 430–436.
- [4] F. DeWinter, N. Zargari, S. Rizzo, and X. Yuan, "Medium voltage drives: Are isolation transformers required?," in *Conf. Rec. IEEE IAS Petroleum Chem. Ind. Conf.*, 2002, pp. 191–196.
- [5] B. Wu, *High-Power Converters and AC Drives*. Piscataway, NJ: IEEE Press, 2006.
- [6] Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep. 2008.
- [7] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, Jan./Feb. 2003.



K.Hari was born in 1989 in India. He has graduated from Santhiram Engineering College, Nandyal in 2011. Presently he is pursuing post graduation in Power electronics Specialization at RGM College of engineering and Technology, Nandyal. His areas of interested include Power electronics, Drives and Control and Electrical Machines. (E-Mail: hari.k027@gmail.com)



K.Kishore Reddy was born in kurnool, India. He received the B.Tech (Electrical and Electronics Engineering) degree from the Jawaharlal Nehru Technological University, Anantapur in 2005; M.Tech (Power Electronics) from the Karunya university in 2009. He is currently an Asst.Professor of the Dept. of Electrical and Electronic Engineering, R.G.M College of Engineering and Technology, Nandyal. His area of interest power electronics and Electric Drives. (E-Mail: kishorekamireddy@gmail.com).



S.Aswak Hussain was born in kurnool, India. He received the B.Tech (Electrical and Electronics Engineering) degree from Rajeev Gandhi Memorial college of Engg., & Tech, Nandyal; M.Tech (Power Electronics) from the G.Pulla Reddy college, Kurnool. He is currently an Asst.Professor of the Dept. of Electrical and Electronic Engineering, R.G.M College of Engineering and Technology, Nandyal. His area of interest power electronics and Electrics, PWM techniques. (E-Mail: shaikaswakhussain@gmail.com).