CLOSED LOOP CONTROL OF AC-DC CONVERTER USING SINGLE SWITCH

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***Abstract* : This paper presents a transformer less ac/dc converter which can be used in voltages between 90- 230 Vrms. Instead of a transformer, this topology consists of a buck dc/dc converter and a buck boost dc/dc converter. By the absence of transformer, reduce the complexity of converter and it is cost effective. Buck dc/dc converter keeps o/p voltage below the line voltage; limit the leakage current. By controlling the circuit with feedback, we can increasing the efficiency and reduce total harmonic distortion. Output voltage is 40 V with THD 12.36%. And output current is near 4 A. For further modification a feedback PI controller is used. After using PI controller THD is reduced to 6.231%.Thus using controlled circuit harmonic content is reduced and efficiency is improved. Working of the proposed circuit and verification by simulation results are discussed in this paper. Simulation is done in MATLAB.**

Keywords: - Integrated buck-buck- boost converter, Total harmonic distortion (THD), Transformer less, PI control

I. INTRODUCTION

The use of rectifiers in industrial applications started at the era of mercury converters with the electromechanical contact converter. DC machines are common in day to day use. But the supply that we get from power companies is AC. To use those machines AC supply has to be turned into DC supply by the use of a rectifier .The basic block diagram of AC/DC converter is shown in Figure 1.1. A rectifier is an electrical device that converts the incoming AC (alternating current) from a transformer or any other ac power source to pulsating DC (direct current). Rectifier may be made of diodes, solid states, vacuum tube, mercury arc valves and other components. Rectifiers are widely used in non linear loads which are connected with distribution systems which plays an important role in power system network (ex: UPS, discharge lamp, television, computer, fax machines, ferromagnetic devices, arc furnaces, energy savers etc).

The research on single-stage PFC ac/dc converters can be traced back to the early 1990s .Single-stage (ss) ac/dc converters have lot of applications because of its cost effectiveness, compact size, and simple control mechanism. Among existing SS converters, most of them are comprised of a boost power-factor correction (PFC) cell followed by a dc/dc cell. Dc/dc cell is used for output voltage regulation . Several such methods are shown in references [1]–[7] .But their intermediate bus voltage is usually greater than the line input voltage and goes beyond 450 V at high-line application. Also there are a lot of efforts to limit this bus voltage, it is still near or above the peak of the line voltage due to the nature of boost-type PFC cell. In addition, the other drawbacks of the boost-type PFC cell are that it cannot limit the input inrush current and provide output short-circuit protection [14].

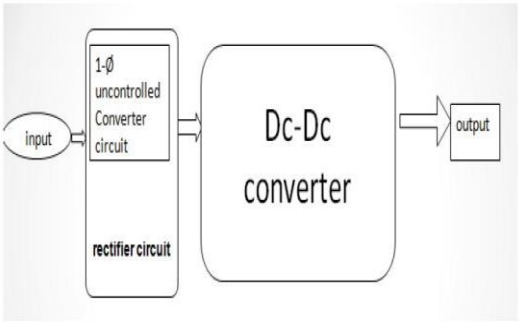


Fig 1.1block diagram of ac to dc converter

Some multistage power electronics system (e.g., in data center, electrochemical and petrochemical

industries), the isolation has been done in the PFC stage, the second transformer in the dc/dc cell for the sake of isolation is considered as redundant. Hence, non-isolated ac/dc converter can be employed to reduce unnecessary or redundant isolation and enhance efficiency of the overall system. Besides, leakage inductance of the transformer causes high spike on the active switch and lower conversion efficiency. To protect the switch, snubber circuit is usually added resulting in more component counts[13]. For low voltage application (e.g.,≤48V), this high intermediate bus voltage increases components stresses on the dc/dc cell. This problem can be overcome by using a simple step-down dc/dc cell (i.e. buck or buck–boost converter).Extremely narrow duty cycle is needed for the conversion. This leads to poor circuit efficiency and limits the input voltage range for getting better performance.

To tackle the aforementioned problems an intergrated buck–buck–boost (IBuBuBo) converter with low output voltage is proposed. This proposed circuit consists of a buck converter, used as PFC cell and a buck-boost converter as a dc/dc converter. This circuit is able to limit the bus voltage below the input voltage effectively. In addition, by In addition, by sharing voltages between the intermediate bus and output capacitors, further reduction of the bus voltage can be achieved. Therefore, a transformer is not needed to obtain the low output voltage. The converter is able to achieve::

1) low intermediate bus and output voltages in the absence of transformer;
2) simple control structure with a single-switch;
3) positive output voltage;
4) high conversion efficiency due to part of input power is processed once and
4) input surge current protection because of series connection of input source and switch.

DIRECT POWER TRANSFER:

In a conventional two-stage or S PFC ac/dc converter, there are two functional cells, i.e., PFC cell and dc/dc cell. AC input power is first transferred into somewhat pulsating dc power stored on intermediate bulk capacitors by the PFC cell. The stored dc power on the bulk capacitors is processed again by the dc/dc cell to the desired dc output power. So the input power is processed twice to reach the output, as shown in Fig. 2.1(a).

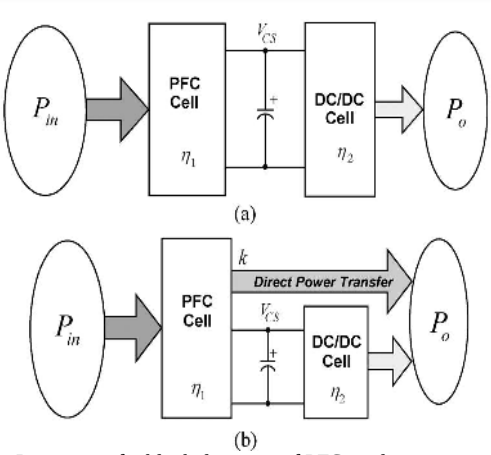


Fig 2: Power transfer block diagrams of PFC ac-dc converter : a) Conventional power transfer and b) proposed power transfer with DPT concept

II. SINGLE STAGE PFC CONVERTER

Power factor correction (PFC) techniques have become increasingly important since several regulations that are used to limit harmonic injection to the power utilities have been enacted recently. There are two basic PFC approaches, namely, active PFC and passive PFC. Active PFC, classified by the system configurations, can be categorized into two-stage and single-stage SS schemes. A two-stage scheme results in high power factor and fast response output voltage regulation by using two independent controllers and optimized power stages, as shown in Fig. 3.1(a). The main drawbacks of this scheme are its relatively higher cost and larger size resulted from its complicated power stage topology and control circuits, particularly in low power applications.

An SS scheme combines the PFC cell and dc/dc power conversion cell into one stage, and typically uses only one controller and shares power switches, as shown in Fig.3order to get high power factor and regulated output, an SS converter actually still needs to complete PFC and dc/dc regulating tasks as a two-stage converter. Usually, the high power factor of an SS PFC converter is guaranteed by operating the PFC cell in discontinuous current mode (DCM), while the fast response output regulation is achieved by the dc/dc cell. Although the single-stage scheme is especially attractive in low cost and low power applications due to its simplified power stage and control circuit, major issues still exist, such as low efficiency and difficulty being moved to higher power level, and high as well as wide-range intermediate dc bus voltage stress.

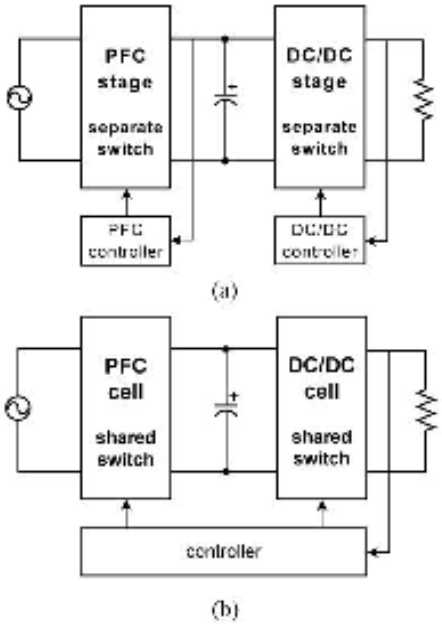


Fig 3: Functional block diagram of PFC converters: a) Two stage PFC converter and b) Typical single-stage PFC converter

III. PROPOSED CIRCUIT AND ITS OPERATING PRINCIPLE

The proposed IBuBuBo converter, which consists of the merging of a buck PFC cell (L_1 , S_1 , D_1 , C_o , and C_B) and a buck–boost dc/dc cell (L_2 , S_1 , D_2 , D_3 , C_o , and C_B) is il- lustrated in Fig. 1(a). Although L_2 is on the return path of the buck PFC cell, it will be shown later in Section III-A that it does not contribute to the cell electrically. Thus, L_2 is not con- sidered as in the PFC cell. Moreover, both cells are operated in discontinuous conduction mode (DCM) so there are no currents in both inductors L_1 and L_2 at the beginning of each switching cycle t_0 . Due to the characteristic of buck PFC cell, there are two operating modes in the circuit.

Mode A (vin (θ) ≤ VB + Vo): When the input voltage vin (θ) is smaller than the sum of intermediate bus voltage VB , and output voltage Vo , the buck PFC cell becomes inactive and does not shape the line current around zero-crossing line voltage [20], owing to the reverse biased of the bridge rectifier. Only the buck–boost dc/dc cell sustains all the output power to the load. Therefore, two dead-angle zones are present in a half-line period and no input current is drawn as shown in Fig. 1(b). The circuit operation within a switching period can be divided into three stages and the corresponding sequence is Fig. 2(a),(b), and (f). Fig. 3(a) shows its key current waveforms.

1) Stage 1 (period d1 Ts in Fig. 3) [see Fig. 2(a)]: When switch S1 is turned ON, inductor L2 is charged linearly by the bus voltage VB while diode D2 is conducting. Output capacitor Co delivers power to the load.

2) Stage 2 (period d2 Ts in Fig. 3) [see Fig. 2(b)]: When switch S1 is switched OFF, diode D3 becomes forward biased and energy stored in L2 is released to Co and the load.

3) Stage 3 (period d3 Ts - d4 Ts in Fig. 3) [see Fig. 2(f)]: The inductor current iL 2 is totally discharged and only Co sustains the load current.

Mode B (vin (θ) > VB + Vo): This mode occurs when the input voltage is greater than the sum of the bus voltage and output voltage. The circuit operation over a switching period can be divided into four stages and the corresponding sequence is Fig. 2(c), (d), (e), and (f). The key waveforms are shown in Fig. 3(b).

1) Stage 1 (period d1 Ts in Fig. 3) [see Fig. 2(c)]: When switch S1 is turned ON, both inductors L1 and L2 are charged linearly by the input voltage minus the sum of the bus voltage and output voltage (vin (θ) − VB − Vo), while diode D2 is conducting.

2) Stage 2 (period d2 Ts in Fig. 3) [see Fig. 2(d)]: When switch S1 is switched OFF, inductor current iL 1 decreases linearly to charge CB and Co through diode D1 as well as transferring part of the input power to the load directly. Meanwhile, the energy stored in L2 is released to Co and the current is supplied to the load through diode D3 . This stage ends once inductor L2 is fully discharged.

3) Stage 3 (period d3 Ts in Fig. 3) [see Fig. 2(e)]: Inductor L1 continues to deliver current to Co and the load until its current reaches zero.

4) Stage 4 (period d4 Ts in Fig. 3) [see Fig. 2(f)]: Only Co delivers all the output power.

An integrated buck-buck-boost converter with low output voltage is proposed. the converter utilizes a buck converter as a PFC cell .it is able to reduce the bus voltage below the line input voltage effectively. In addition, by sharing voltage between the intermediate bus and output capacitor, further reduction of bus voltage can be achieved.

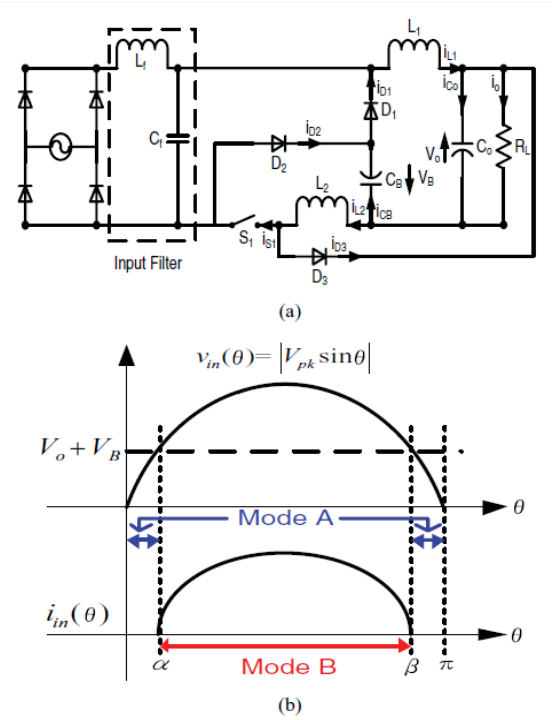
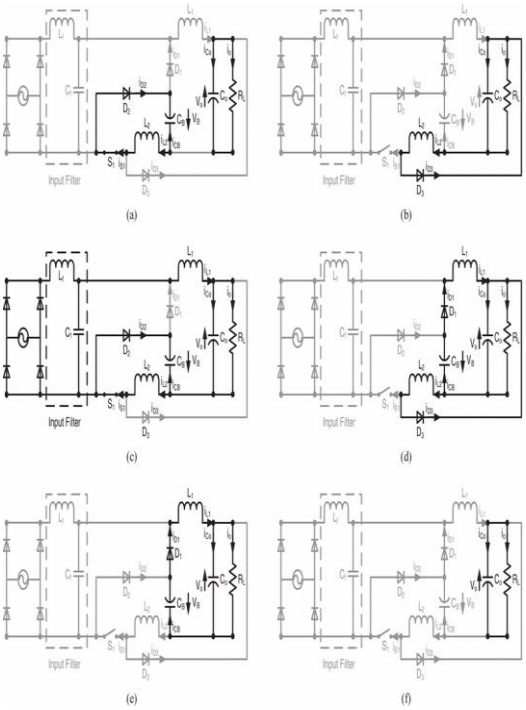


Fig 4 (a) Proposed IBuBuBo SS ac/dc converter. (b) Input voltage and current waveforms.



III DESIGN CONSIDERATION

To simplify the circuit analysis, some assumptions are made as follows:

1)all components are ideal;
2)line input source is pure sinusoidal, i.e vin (θ) = Vpk sin(θ) where Vpk and θ are denoted as peak Voltage and phase angle, respectively;

3) both capacitors CB and Co are sufficiently large such that they can be treated as constant DC voltage sources without any ripples;

4) the switching frequency fs is much higher than the line frequency such that the rectified line input voltage |vin (θ)| is constant within a switching period.

IV. CIRCUIT CHARACTERISTICS

According to Fig. 1(b), there is no input current drawn from the source in Mode A, and the phase angles of the dead-time α and β can be expressed as

$$\alpha = \arcsin\left(\frac{V_T}{V_{pk}}\right)$$

$$\beta = \pi - \alpha = \pi - \arcsin\left(\frac{V_T}{V_{pk}}\right) \qquad (3.1)$$

In addition, by considering volt–second balance of the L1 and L2 , respectively, the important duty ratio relationships can be expressed as follows:

$$\gamma = \beta - \alpha = \pi - 2\arcsin\left(\frac{V_T}{V_{pk}}\right) \qquad (3.2)$$

From the key waveforms (see Fig. 3), the peak currents of the two inductors are

$$i_{L1-pk} = \begin{cases} \frac{V_{in}(\theta)-V_T}{L_1} d_1 T_S, \alpha < \theta < \beta \\ 0, otherwise \end{cases} \qquad (3.3)$$

$$I_{L2-pk} = \frac{V_B}{L_1} d_1 T_S \qquad (3.4)$$

where Ts (1/fs) is a switching period of the converter. In (3) and (4), the dependency of iL 1 pk on θ has been omitted for clarity. It is noted that L2 does not contribute in (3) even though it is on the current return path of the PFC cell.

$$d_2 + d_3 = \begin{cases} \frac{v_{in}(\theta)-V_T}{V_T} d_1, \alpha < \theta < \beta \\ 0, otherwise \end{cases} \qquad (3.5)$$

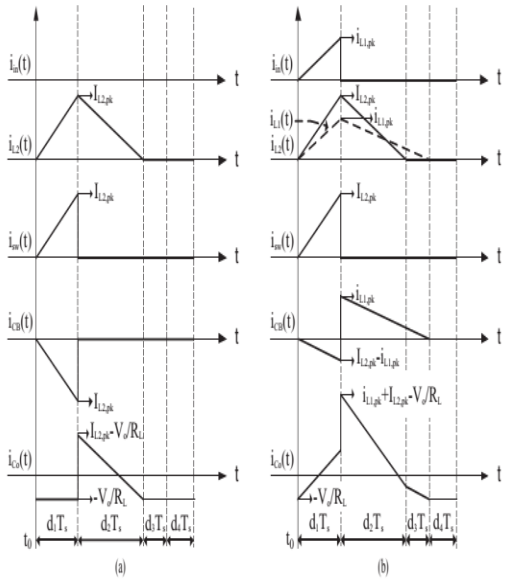


Fig .5(a)Proposed IBuBuBo SS ac/dc converter. (b) Input voltage and current waveforms

$$d_2 = \frac{V_B}{V_o} d_1 \quad (3.6)$$

By applying charge balance of CB over a half-line period, the bus voltage VB can be determined. From Fig. 3, the average current of CB over a switching and half-line periods are expressed as follows:

$$< i_{CB} >_{SW} = \frac{1}{2}\left(i_{L1-pk}\left(d_1 + d_2 + d_3\right) - I_{L2-}pkd_1\right) = \frac{d_1^2 T_S}{2}\left[\left(\frac{\left(v_{in}(\theta) - V_T\right)v_{in}(\theta)}{L_1 V_T} - \frac{V_B}{L_2}\right)\right] \quad (3.7)$$

$$< i_{CB} >_{\pi} = \frac{1}{\pi}\int_0^{\pi} < i_{CB} >_{sw} d\theta = \frac{d_1^2 T_S}{2\pi}\left[\frac{V_{pk}}{L_1}\left(V_{pk}V_T\left(\frac{\gamma}{2} + \frac{A}{4}\right) - B\right) - \frac{V_B \pi}{L_2}\right] \quad (3.8)$$

where the constants A and B are

$$A = \sin(2\alpha) - \sin(2\beta) \quad (3.9)$$

$$B = \cos(\alpha) - \cos(\beta) \quad (3.10)$$

Putting (8) to zero due to the steady-state operation, this leads to

$$V_B = \frac{MV_{pk}^2}{2\pi\left(V_B + V_0\right)} \times \left[\pi - 2arc\right]\sin\left(\frac{V_B + V_0}{V_{pk}}\right) - \frac{2\left(V_B + V_0\right)\sqrt{\left(V_{pk} + V_B + V_0\right)\left(V_{pk} - V_B - V_0\right)}}{V_{pk}^2} \quad (3.11)$$

Where M is the inductance ratioL2/L1.

As observed from (11), the bus voltage VB can be obtained easily by numerical method. It is noted that VB is independent on the load, but dependent on the inductance ratio M. Fig. 4 depicts the relationship among VB, rms value of the line voltage, and inductance ratio M. It is noted that the bus voltage is kept below 150 V at high-line input condition.

Similarly, the instantaneous and average input currents of the proposed circuit are

$$\left\langle i_{in} \right\rangle_{sw} = \frac{i_{L1-PK} d_1}{2} = \begin{cases} \frac{v_{in}(\theta) - V_T}{2L_1} d_1^2 T_S, \alpha < \theta < \beta \\ 0, otherwise \end{cases} \quad (3.12)$$

$$I_{in} = \frac{1}{\pi}\int_{\alpha}^{\beta} < i_{in} >_{sw} d\theta = \frac{d_1^2 T_S}{2\pi L_1}\left[V_{pk}B - V_T\gamma\right] \quad (3.13)$$

Using (3.12) and (3.13), the rms value of the input current, average input power and power factor are given by

$$I_{in-rms} = \sqrt{\frac{1}{\pi}\int_{\alpha}^{\beta}\left(< i_{in} >_{sw}\right)^2 d\theta} = \frac{d_1^2 T_S}{2\sqrt{\pi}L_1}\sqrt{V_{pk}^2\left(\frac{\gamma}{2} + \frac{A}{4}\right) - 2V_{pk}V_T B + V_T^2\gamma} \quad (3.14)$$

$$P_{in} = \frac{1}{\pi}\int_{\alpha}^{\beta} v_{in}(\theta) < i_{in} >_{sw} d\theta = \frac{d_1^2 T_S V_{pk}}{2\pi L_1}\left[V_{pk}\left(\frac{\gamma}{2} + \frac{A}{4}\right) - V_T B\right]$$

$$PF = \frac{\frac{1}{\pi}\int_{\alpha}^{\beta} v_{in}(\theta) < i_{in} >_{sw} d\theta}{\frac{V_{pk}}{\sqrt{2}} I_{in-rms}} = \sqrt{\frac{2}{\pi}} \frac{V_{pk}\left(\frac{\gamma}{2}+\frac{A}{4}\right) - V_T B}{\sqrt{V_{pk}^2\left(\frac{\gamma}{2}+\frac{A}{4}\right) - 2V_{pk}V_T B + V_T^2 \gamma}} \quad (3.16)$$

exhibits the variation of power factor as a function of line input voltage and the inductance ratio M of the converter.

V. CONDITION FOR DCM

To ensure both cells working in DCM mode throughout the ac line period, we must determine their critical inductance first. To allowL1working in DCM and from (5), we have the following inequalities:

$$d_2 + d_3 \le 1 - d_{1\_}PFC \quad (3.1$$

$$d_{1\_}PFC \le \left\{ \begin{matrix} \frac{V_T}{v_{in}(\theta)}, \alpha < \theta < \beta \\ 0, otherwise \end{matrix} \right\} \quad (3.18)$$

Where $d_{1\ PFC}$ is the maximum d_1 of the PFC cell. For the buck–boost dc/dc cell working in DCM mode, the following inequality must be held:

$$d_2 \le 1 - d_{1\_}DC/DC \quad (3.19)$$

From (3.6) and (3.19), the maximumd1of the dc/dc cell is

$$d_{1\_}DC/DC \le \frac{V_0}{V_0 + V_B} = \frac{V_0}{V_T} \quad (3.20)$$

Due to sharing switch in both cells of the converter, the maximum duty cycle d_{1_max} of the proposed converter is

$$d_{1-\max} = \left\{ \begin{matrix} \min(d_{1\_}DC/DC), \alpha < \theta < \beta \\ d_{1\_}DC/DC, otherwise \end{matrix} \right\} \quad (3.21)$$

By applying input–output power balance of the PFC cell and substituting (21) into (15), the critical inductance L_{1_crit} is given by

$$L_{1-crit} = \frac{R_{L-\min} T_S V_{pk} V}{2V_0{}^2 \pi} \left[\begin{matrix} V_{pk}\left(\frac{\gamma}{2} + \frac{\sin(2\alpha) - \sin(2\beta)}{4}\right) \\ + V_T(\cos(\beta) - \cos(\alpha)) \end{matrix} \right] d_{1-\max} \quad (3.22)$$

For the dc/dc cell sustaining all the power to the load under DCM operation in Mode A, the critical inductance L_{2_crit} is the smallest. Under the input–output power balance of the dc/dc cell, the critical inductance L_{2_crit} can be determined. The input power of the dc/dc cell in Mode A is given by

$$P_{in-DC/DC} = \frac{V_B}{\pi}\int_0^{\pi} < i_{DC/DC} >_{sw} d\theta = \frac{V_B^2 T_S}{2L_2} d_1^2 \quad (3.23)$$

Where<idc/dc>sw is the instantaneous input

current of dc/dc cell.

Hence, by substituting (3.21) into (3.23), the critical inductance L_{2_crit} is given by

$$L_2 - crit = \frac{R_{L-}\min V_B^2 T_S}{2V_0^2} d_1^2 \_\max \quad (3.24$$

VOLTAGE STRESSES ON THE SEMICONDUCTOR DEVICES

SEMICONDUCTER DEVICE	PEAK VOLTAGE
DIODE D1	Vpk
DIODE D2	Vpk
DIODE D3	VT
SWITCH S1	Vpk + VT

VI. COMPONENT STRESSES

$$C_B = \frac{2P_0 t_{hold-up}}{(V_B @ 90V_{rms})^2}$$

Apart from the size of C_B, it is noted that the line frequency ripple on the output capacitor Co is inevitable since a portion of the input power is coupled to the load directly. However, this ripple can be reduced by increasing its capacitance.

Distribution of Direct Power Transfer

The interaction of power processing between both PFC and dc/dc cells under low and high-line conditions is described as

$$p_0(\theta) = p_{0\_}PFC^{(\theta)} + P_{0\_}DC/DC^{(\theta)} \quad (3.33)$$

Where $P_o(\theta)$, $P_{o\_PFC}(\theta)$, and $P_{o\_DC/DC}(\theta)$ are denoted as instantaneous output power of the converter, output power of PFC cell and output power of dc/dc cell, respectively.

Both instantaneous output powers of PFC and dc/dc cells can be calculated as

$$p_{0\_}PFC^{(\theta)} = V_0 \left\langle i_{L1(\theta)} \right\rangle_{SW} = \left\{ \frac{(d_1(\theta))^2 V_0 T_S}{2} \left[\frac{v_{in}(\theta)(v_{in}(\theta) - V_T)}{L_1 V_T} \right], \alpha < \theta < \beta \right\} \quad (3.35)$$

$$P_{O-DC/DC}(\theta) = P_{in-DC/DC}(\theta) = V_B < i_{DC/DC} >_{sw} = \frac{V^2{}_B T_S}{2L_2}(d_1(\theta))^2 \quad (3.36)$$

Where $P_{in_dc/dc}(\theta)$and $d_1(\theta)$are defined as the instantaneous value of input power of the dc/dc cell and duty cycle d_1. From (34) and (35), it can be seen that $d_1(\theta)$plays a crucial role in this analysis.$d_1(\theta)$can be obtained easily once the average output current of the converter is determined. By considering the average currents of i_{L1} and i_{d3} over a switching cycle, the average output current of the converter is given b

$$I_O = \left\{ \begin{matrix} \langle i_{l1}(\theta) \rangle_{sw} + \langle i_{d3}(\theta) \rangle_{sw}, \alpha < \theta < \beta \\ \langle i_{d3}(\theta) \rangle, otherwise \end{matrix} \right\} = \left\{ \begin{matrix} \frac{(d_1(\theta))^2 T_S}{2} \left[\frac{v_{in}(\theta)(v_{in}(\theta)) - V_T}{L_1 V_T} + \frac{V_{B^2}}{L_2 V_O} \right], \alpha < \theta < \beta \\ \frac{(d_1(\theta))^2 T_s V^2 B}{2L_2 V_O}, otherwise \end{matrix} \right\} \quad (3.36)$$

Hence,$d_1(\theta)$in a half-line period is expressed as

$$\text{?}\, d_1(\theta) = \left\{ \begin{matrix} \sqrt{\frac{2P_O}{V_O T_S \left[\frac{v_{in}(\theta)(v_{in}(\theta) - V_T)}{L_1 V_T} + \frac{V_{B^2}}{L_2 V_O} \right]}}, \alpha < \theta < \beta \\ \sqrt{\frac{2L_2 P_O}{V_{B^2} T_S}}, otherwise \end{matrix} \right\} \quad (3.37)$$

By substituting (3.37) into (3.34) and (3.35), the simultaneous output power of the converter and power distribution of the PFC and dc/dc cells are plotted as in Fig. 6. The traces of single and double power processing represent the power proceed by PFC cell $P_{o\_PFC}(\theta)$ and dc/dc cell $P_{o\_dc/dc}(\theta)$, respectively. Besides, the green dash trace is the output power ($P_{o\_total}(\theta)$) of the converter. It is noted that the power handled by both cells is changed oppositely to maintain the load power under different input voltages. At low-line condition, there is more input power coupled to the output directly. In contrast, more power is delivered to the output by the dc/dc cell at high-line condition.

Distribution of Direct Power Transfer

The interaction of power processing between both PFC and dc/dc cells under low and high-line conditions is described as

$$p_0(\theta) = p_{0\_}PFC^{(\theta)} + P_{0\_}DC/DC^{(\theta)} \quad (3.33)$$

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Both instantaneous output powers of PFC and dc/dc cells can be calculated as

$$p_{0\_}PFC^{(\theta)} = V_0 \left\langle i_{L1(\theta)} \right\rangle_{SW} = \left\{ \frac{(d_1(\theta))^2 V_0 T_S}{2} \left[\frac{v_{in}(\theta)(v_{in}(\theta) - V_T)}{L_1 V_T} \right], \alpha < \theta < \beta \right\} \quad (3.35)$$

$$P_{O-DC/DC}(\theta) = P_{in-DC/DC}(\theta) = V_B < i_{DC/DC} >_{sw} = \frac{V^2{}_B T_S}{2L_2} (d_1(\theta))^2 \quad (3.36)$$

Where $P_{in_dc/dc}(\theta)$and $d_1(\theta)$are defined as the instantaneous value of input power of the dc/dc cell and duty cycle d_1. From (34) and (35), it can be seen that $d_1(\theta)$plays a crucial role in this analysis.$d_1(\theta)$can be obtained easily once the average output current of the converter is determined. By considering the average currents of i_{L1} and i_{d3} over a switching cycle, the average output current of the converter is given by

$$I_O = \left\{ \begin{array}{c} \langle i_{l1}(\theta) \rangle_{sw} + \langle i_{d3}(\theta) \rangle_{sw}, \alpha < \theta < \beta \\ \langle i_{d3}(\theta) \rangle, otherwise \end{array} \right\} = \left\{ \begin{array}{c} \frac{(d_1(\theta))^2 T_S}{2} \left[\frac{v_{in}(\theta)(v_{in}(\theta)) - V_T}{L_1 V_T} + \frac{V_{B^2}}{L_2 V_O} \right], \alpha < \theta < \beta \\ \frac{(d_1(\theta))^2 T_s V^2 B}{2 L_2 V_O}, otherwise \end{array} \right\} \quad (3.36)$$

Hence,$d_1(\theta)$in a half-line period is expressed as,

$$d_1(\theta) = \left\{ \begin{array}{c} \sqrt{\frac{2P_O}{V_O T_S \left[\frac{v_{in}(\theta)(v_{in}(\theta) - V_T)}{L_1 V_T} + \frac{V_{B^2}}{L_2 V_O} \right]}}, \alpha < \theta < \beta \\ \sqrt{\frac{2L_2 P_O}{V_{B^2} T_S}}, otherwise \end{array} \right\} \quad (3.37)$$

By substituting (3.37) into (3.34) and (3.35), the simultaneous output power of the converter and power distribution of the PFC and dc/dc cells are plotted as in Fig. 6. The traces of single and double power processing represent the power proceed by PFC cell $P_{o\_PFC}(\theta)$ and dc/dc cell $P_{o\_dc/dc}(\theta)$, respectively. Besides, the green dash trace is the output power ($P_{o\_total}(\theta)$) of the converter.

TABLE II

CIRCUIT COMPONENTS

Parameters	
IC Controller	TL594
Input filter inductor Lf	2 mH
Input filter capacitor Cf	2 µF
Inductor L1	106 µH
Inductor L2	46 µH
Inductance Ratio (M = L2/L1)	0.434
MOSFET S1	SPW47N60CFD
D1	MUR3040PT
D2	MUR3040PT
D3	MUR3040P
CB	5 mF
Co	5 mF

VII. SIMULATION RESULTS

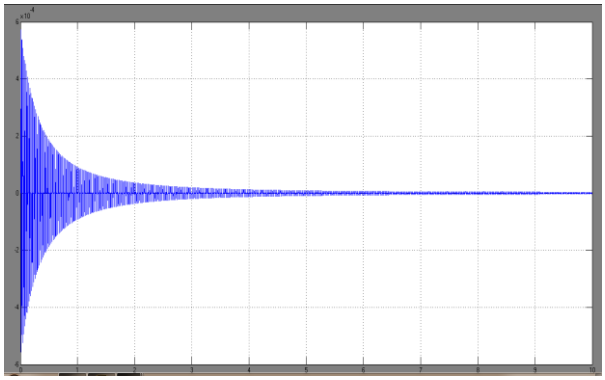

Fig 1 .output current at 90 Vrms

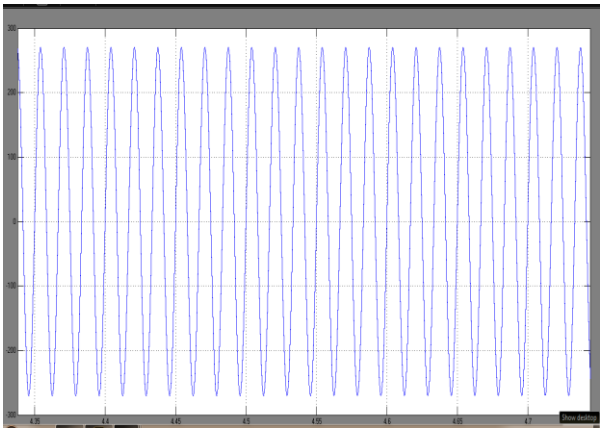

Fig 2.mean value at123v output voltage 270Vrms

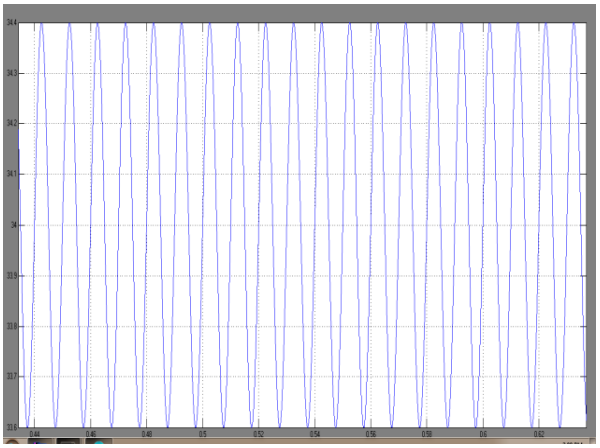

Fig 5 .Extension output voltage at mean value

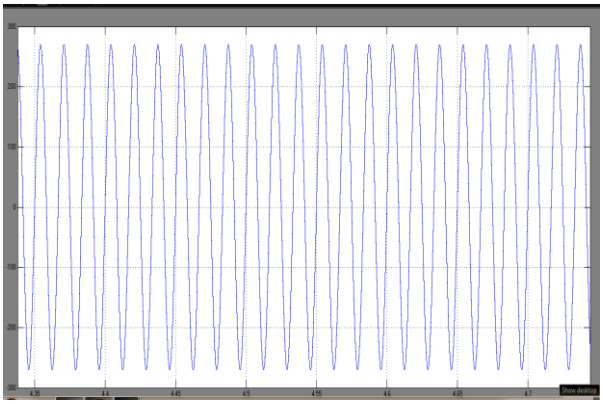

Fig 3.output voltage at 270Vrms

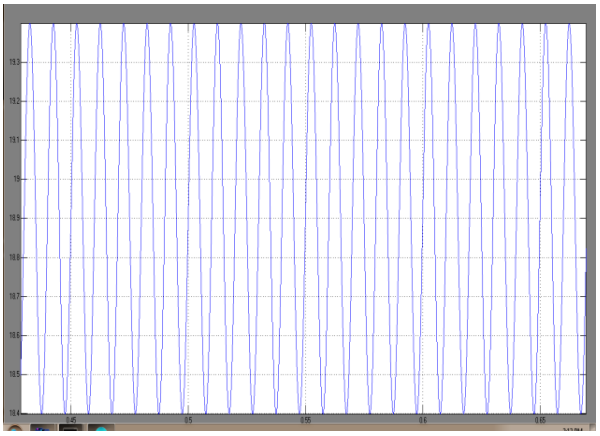

Fig .Extension output voltage

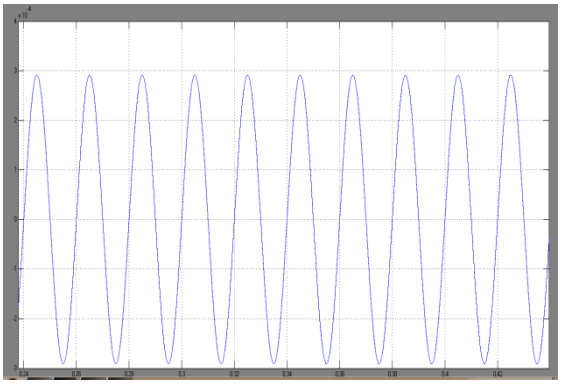

Fig 4 .Extension output current

VIII. CONCLUSION

Proposed AC/DC converter has been simulated and wave forms have been observed. This topology is able to obtain low output voltage without a high step down transformer. Output voltage is achieved about 40 volt and output current is obtained 4 A. Because of the direct power transfer, it is able to achieve high efficiency. Basic circuit has no control loop, for more efficiency and to reduce harmonic distortion added a feedback controller. Output voltage is direct current with THD 12.36%. For further modification a feedback PI controller is used. After using PI controller THD is reduced to 6.231%.Thus using controlled circuit harmonic content is reduced and efficiency is improved. Using the control loop, we can achieve the desired output by changing the

PI controller constant. Total harmonic distortion is decreased and efficiency is increased. We can also develop a high step up ac/dc converter without transformer by replacing buck converter with a boost converter. Proposed converter is used only for the voltages between 90-230Vrms, it keeps intermediate bus voltage below the input line voltage. Thus efficient step down can be achieved. Because of the series connection of source and switch, input surge current can be prevented. Output voltage will be positive in this converter .Simple control mechanism due to single switching. Complexity due to transformer is eliminated, thus leakage inductance and spikes in active switching is absent leads to high efficient conversion

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