Design and Implementation of Speed Efficient MAC Unit Based on Ancient Vedic Multiplication Technique

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Abstract*— This research work is devoted to design high speed thirty two bit Multiply Accumulate Unit. MAC Unit is the key element of digital signal processors to perform various sophisticated tasks like as FFT, DFT, resolving various complex equations and Convolution etc. along with this it is also used in various configurations like as IIR, FIR etc. Every digital domain based technology depends upon the operations performed by MAC Unit either partially or whole. Speed is the most prominent factor of processor and controllers being used recently. That's why it is highly required to design high speed MAC, which can enhance the efficiency of those modules which lies upon the operations performed by MAC. The speed of MAC greatly depends upon the speed of multiplier. At algorithmic and structural level there are so many multiplication algorithms exist now-a-days. After a thorough study and proper analysis we have seen that Vedic multiplication technique is the best algorithm that gives much better result in comparison to others in terms of speed. Further we have analyzed different existing Vedic multiplication hardware, and compared those with respect to speed. And found that the Vedic multiplier with Carry Save Adder gives better outcome. Then we have proposed that multiplier for the MAC unit design. This proposed MAC Unit is able to perform different arithmetic operations at high speed. All sub-modules in the MAC unit has been designed in combinatorial form. And integrated in the final module, in which we have provided the reset and clock functionality to have better control on the circuitry. To design proposed multiply accumulate unit verilog hardware description language (HDL) has been used. To design operational sub-modules data flow modeling and to integrate these modules behavioral modeling style has been used. For this design the target FPGA belongs to Spartan-3E (family), XC3S500E (device), FG320 (package) with speed grade of -5. For synthesis purpose Xilinx synthesis tool (XST) of Xilinx ISE-9.2i has been used. For the behavioral simulation purpose ISE simulator has been used.

***Keywords*— MAC, Vedic Multiplier with CSA, Xilinx-ISE9.2i,**

I. INTRODUCTION

Today in the digital domain world digital signal processing is of main concern, whose performance is mainly dependent upon the MAC unit. MAC unit optimization can also provide the Digital Signal Processors' performance optimization, and Multiplication is the main operation in MAC unit. Multiplication is the most time consuming module amongst the basic mathematical calculation. With these considerations, it is always important to have fast and efficient mechanism to implement mathematical functions. Vedic Mathematics is a name which is heard many times by us from childhood to solve complex mathematics problem mentally. One of the main purposes of Vedic mathematics is to transform the tedious calculations into simpler, orally manageable operation without much help of pen and paper. Any ordinary human can perform mental operations for very small magnitude of numbers and hence Vedic mathematics provides techniques to solve operations with large magnitude of numbers easily by converting it to small magnitude of numbers. Vedic mathematics provides more than one method for multiplication operations. For each operation there is at least one generic method provided along with some methods which are directed towards specific cases simplifying the calculations further. [2] has described the Vedic mathematics thoroughly. Vedic mathematics provides algorithms to simplify the mathematics and hence is perfect solution for the problem stated. After a thorough and comparative study we have found that Vedic multiplier designed by **[**1] is better than other available multipliers.

Before designing our proposed MAC unit it's imperative to elaborate the working of the Vedic multiplier:-

In our daily life all of us, perform so many tasks based upon simple calculations, which is based upon conventional multiplication algorithm of the arithmetic. So it can be easily said that all of us are very familiar with conventional multiplication algorithm. It is very tedious to multiply two numbers with large in magnitude than with smaller in magnitude, as human mind is not able and not trained to handle these large magnitude numbers. It can be illustrated using a very simple example, where we have taken the multiplier and multiplicand of two digit length. Suppose we want to multiply 31 with 44:-

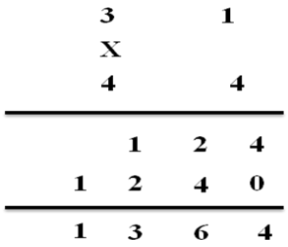

Figure 1 Conventional Multiplication Technique

To perform conventional multiplication: -
Multiply 31 with first RHS digit 4 = 124. And store it in register.
Then multiply second RHS digit 4 with 31 = 124.
Provide left padding of 1 digit = 1240.
Add first partial product with second. And get result, which is 1364.
This is a very handy job. So, to handle these kind of problems mental mathematics (Vedic mathematics), developed by the Jagatguru Swami Balkrishna Teerth Ji Maharaj based approaches can be used, to have a better outcome. This is based upon sixteen formulas and sixteen sub-formulas. Using mental multiplication approaches, suggested by Vedic mathematics, Human mind can be trained to perform the multiplication of numbers with the large magnitudes also. Actually the logic behind this one is that, the Vedic (mental) multiplication breaks the multiplication of large magnitude numbers into the multiplication of small magnitude numbers. There are two algorithms which are suggested by the Vedic mathematics, first one is the Urdhva Triyambakam and second one is the Nikhilam. But Nikhilam algorithm doesn't provide better outcome in all cases, it provide better result only then when multiplier and multiplicand both are near to the base, for other cases it has some limitations. So, it can't be used universally. Vedic Urdhva Triyambakam algorithm is the multiplication algorithm, which provide better outcome in all cases, and so can be applied to all type of numbers universally. This is illustrated using an example where multiplier and multiplicand of two digit length. Suppose we want to multiply 31 with 44 using the Vedic (mental) multiplication approach:-
First we are showing the syntax for two digit multiplication using Vedic multiplication approach:-

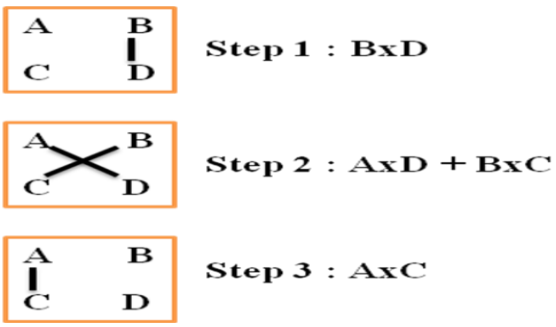

Figure 2 two bit vedic multiplication syntax

Then with the use of above given syntax the multiplication has been performed, which is shown below:-

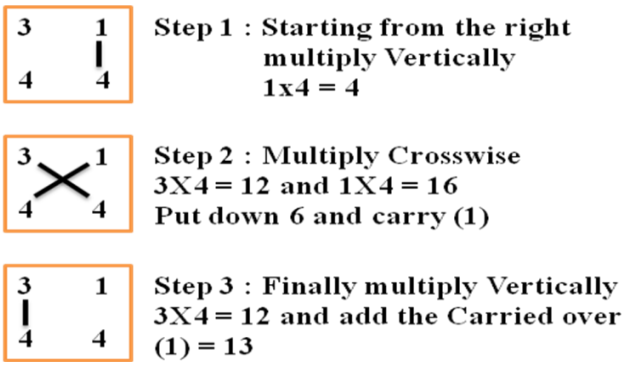

Figure 3 Decimal Multiplication Using Vedic Multiplication syntax

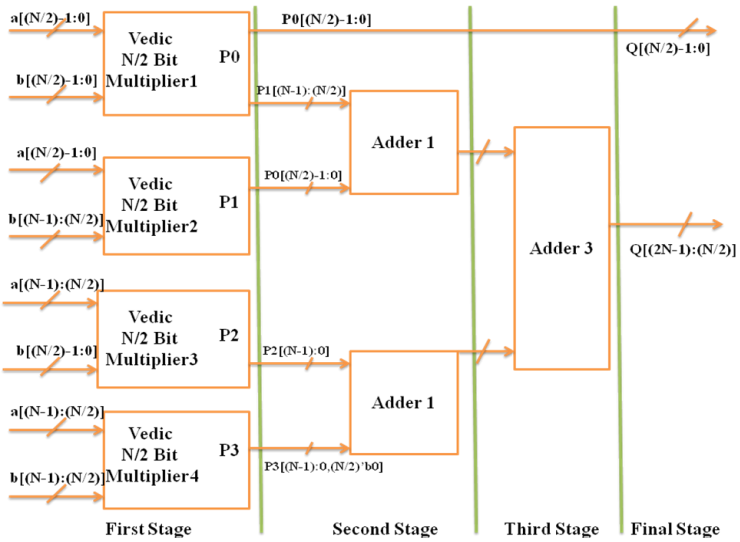

Figure 4: NxN bit Vedic multiplier architecture [4]

On the basis of above example we can say that how efficient the Vedic multiplication is.
After a thorough study we have found that [1] has introduced a new approach to design the architecture of Vedic multiplier, Apart from vedic multiplier there are two popular methods to perform multiplication operation first one is Wallace due to its high speed because of its unique addition tree structure and second one is Booth that takes less area to perform multiplication. Using combination of these two techniques a high speed multiplier has been designed known as Modified Booth Wallace Multiplier. We also have proposed the combination of Urdhva Triyakbhyam sutra with unique addition tree structure similar to Wallace for multiplication to design MAC unit. Here [1] has used conventional Vedic multiplier for design of 2x2 bit multiplier and for higher level multiplier [1] has replaced the Conventional Adder which is required during the Partial Product generation with unique addition tree structure similar to Wallace addition tree structure and found that our proposed design is better than conventional Vedic multiplication hardware in terms of speed.

II. PROPOSED MAC UNIT

The proposed 32-bit MAC unit's block diagram can be shown as below: -

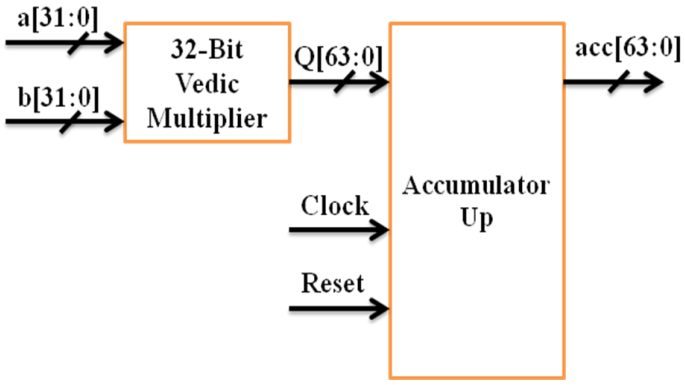

Figure 4 Proposed MAC unit Block Diagram

Here multiplier and multiplicand are the two 32-bit inputs of our MAC Unit. And other sections of the design are self-explanatory. We have compared various Multipliers and found that Vedic Urdhva Triyambakam is the better multiplier in comparison to other conventional Multipliers. Now here a basic question arises that why we have not used Multiplier of XILINX CORE IP, the answer is simple is if we put clock in that XILINX CORE IP multiplier then its SET-UP and HOLD-TIME gets increased in comparison to our proposed Vedic Multiplier.

III. COMPARATIVE RESULTS OF PROPOSED VEDIC MULTIPLIER FOR MAC UNIT

To show the efficiency of proposed Vedic multiplier, it has been implemented and compared with other popular multiplier structures based on different multiplication algorithms on the same platform of target FPGA, which has been used to implement these popular multiplier structures. We have compared our module with different modules and shown comparison on the basis of provided results availability of results. Comparison tables are shown below:-

- In the following given table, target FPGA belongs to Spartan 3AN (family), XC3S50A (device), -7 (speed grade). this multiplier is with clock circuitry, so we have also placed clock circuitry with our multiplier: -

Path Delay (in ns) for different multipliers at sixteen bit level	
Urdhva Triyagbhyam multiplier [31]	**Proposed**
21.647	**6.463**

- In the following given table which target FPGA has been used belongs to Spartan 3 (family), XC3S400 (device), TQ144 (Package), -5 (speed grade).

Maximum Combinational Path Delay (in ns) for different multipliers at eight bit level				
Array Multiplier [33]	**Booth Multiplier [33]**	**Vedic Multiplier with KSA [33]**	**Vedic Multiplier with KSA [32]**	**Proposed**
32.01	**29.549**	**23.644**	**28.699**	**19.467**

- In the following given table which target FPGA has been used belongs to Spartan 3E (family), XC3S500E (device), FG320 (Package), -5 (speed grade).

Maximum Combinational Path Delay (in ns) for different multipliers at eight, sixteen and thirty two bit level			
Bit Level	**Karatsuba Multiplier [34]**	**Vedic multiplier with CSA [34]**	**Proposed**
8	**31.029**	**15.418**	**15.673**
16	**46.811**	**22.604**	**20.337**
32	**82.834**	**31.526**	**26.573**

- In the following given table which target FPGA has been used belongs to Virtex-5 (family), XCVLX50 (device), FF324 (Package), -2 (speed grade).

Maximum Frequency (in MHz) for different multipliers at sixteen and thirty two bit level			
Bit level	**Normal Booth Multiplier [35]**	**Urdhva multiplier [35]**	**Proposed**
16	**100**	**233.3**	**316.636**
32	**100.12**	**165.3**	**269.964**

- In the following given table which target FPGA has been used belongs to Spartan3 (family), XC3S50 (device), PQ208 (Package), -5 (speed grade).

Maximum Combinational Path Delay (in ns) for different multiplier at four bit level			
Bit level	**Urdhva Multiplier with RCA [36]**	**Urdhva Multiplier with CLA adder [36]**	**Proposed**
4	**17.796**	**17.560**	**15.673**

- In the following given table which target FPGA has been used belongs to Spartan3E (family), XC3S500E (device), FG320 (Package), -5 (speed grade).

Maximum Combinational Path Delay (in ns) for different multipliers at four bit level			
Array	**KCM**	**Urdhva**	**Proposed**

Multiplier [37]	(Constant coefficient multiplier [37]	multiplier [37]	
4	18.792	22.864	13.954

- In the following given table which target FPGA has been used belongs to Spartan3 (family), XC3S50 (device), PQ208 (Package), -4 (speed grade).

Maximum Combination Path Delay (in ns) for different multipliers at four bit level		
Array multiplier [38]	Vedic multiplier [38]	Proposed
20.471	17.768	16.143

- In the following given table which target FPGA has been used belongs to Virtex 2P (family), XC2VP2 (device), FG 256 (Package), -7 (speed grade).

Maximum Combinational Path Delay (in ns) for different multipliers at eight bit level						
Karatsuba [41]	Vedic Karatsuba [41]	Modified Booth-Wallace [42]	Vedic with Partitioning [42]	Conventional Vedic [41]	Vedic with CSA [39]	Proposed
31.029	18.695	15.815	15.685	15.418	13.07	11.886

- In the following given table which target FPGA has been used belongs to Spartan 3 (family), XC3S50 (device), PQ 208 (Package), -4 (speed grade).

Maximum Combinational Path Delay (in ns) for different multipliers at eight bit level			
Array [40]	Booth [40]	Conventional Vedic [40]	Proposed
32.01	29.549	24.1	19.467

- In the following given table which target FPGA has been used belongs to Spartan3E (family), XC3S500E (device), FG320 (Package), -5 (speed grade).

Maximum Combinational Path Delay (in ns) for MAC Unit at thirty two bit level		
MAC using Wallace tree [43]	MAC using Vedic multiplier [43]	Proposed
64.624	37.799	6.100

- In the following given table which target FPGA has been used belongs to Spartan3E (family), XC3S100E (device), TQ144 (Package), -5 (speed grade).

Maximum Combinational Path Delay (in ns) for MAC Unit at thirty two bit level	
MAC using Vedic multiplier [45]	Proposed
14.69	6.100

- In the following given table which target FPGA has been used belongs to Spartan2 (family), XC2S200 (device), PQ208 (Package), -6 (speed grade).

Maximum Combinational Path Delay (in ns) for MAC Unit at thirty two bit level	
MAC using Vedic multiplier [45]	Proposed
14.69	6.100

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