Harmonic distortion analysis of induction motor drive with advanced multilevel control strategy using photo voltaic system

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***Abstract*--This paper shows that versatile stand-alone photovoltaic (PV) systems still demand on at least one battery inverter with improved characteristics of robustness and efficiency, which can be achieved using multilevel topologies. A compilation of the most common topologies of multilevel converters is presented, and it shows which ones are best suitable to implement inverters for stand alone applications in the range of a few kilowatts. The harmonics content of the output signals are analyzed. Two types of harmonics are investigated for induction motors: space harmonics and time harmonics. Space harmonics are generated due to the different phase windings interaction when the power supply is sinusoidal and they can be reduced by applying a proper machine design. A simplified Pulse Width Modulation (SPWM) method for a multilevel inverter that supplied an induction motor is developed. The controller equations are such that the SPWM pulses are generated automatically for any number of levels.**

***Index Terms*— Induction motor, Multilevel inverter, Energy management, PV Battery, Multilevel SPWM, THD.**

I. INTRODUCTION

Now adays solar power is the quintessential energy source and receiving considerable attention from the researchers. Solar photovoltaic (PV) system generates electricity with advantages such as no pollution, no noise and many more. Solar PV is well suited to remote or arid regions. The rapid evolution of semiconductor devices manufacturing technologies and the designer's orientation has enabled the development of new structures of converters (inverters) with a great performance compared to conventional structures. So, these new technologies of semiconductor are more suited to high power applications and they enable the design of multilevel inverters. The constraints due to commutation phenomena are also reduced and each component supports a much smaller fraction of the DC-bus voltage when the number of levels is higher. For this reason, the switches support more high reverse voltages in high-power applications and the converter output signals are with good spectral qualities. Thus, the using of this type of inverter, associated with a judicious control of power components, allows deleting some harmonics [1]. Among the control algorithms proposed in the literature in This field [2-3-4], the SPWM, appears most promising. It offers great flexibility in optimizing the design and it is well suited for digital implementation. It also helps to maximize the available power. The main advantage of multilevel inverters is that the output voltage can be generated with a low harmonics. Thus it is admitted that the harmonics decrease proportionately to the inverter level. For these reasons, the multilevel inverters are preferred for high power applications [5-6]. However, there is no shortage of disadvantages. Their control is much more complex and the techniques are still not widely used in industry [7-8].

The traditional inverters are Voltage Source Inverter (VSI) and Current source Inverter (CSI), which consist of diode rectifier front end, DC link and Inverter Bridge. In order to improve power factor, either an AC inductor or DC inductor is normally used. The DC link voltage is roughly equal to 1.35 times the line voltage and the Voltage source inverter is a buck converter that can only produce an AC voltage limited by the dc link voltage. Because of this nature, the Voltage source inverter based PWM VSI and CSI are characterized by relatively low efficiency because of switching losses and considerable Electromagnetic Interference (EMI) generation.

I. PHOTOVOLTAIC SYSTEM

The PV cell characteristics are strongly nonlinear in nature; it's most referred equivalent circuit. The Related expression is given in equation (1) [9] as follows:

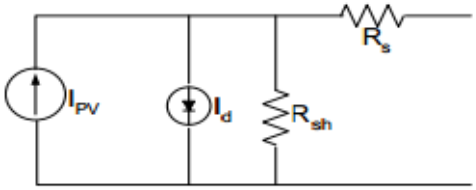


Fig.1. Equivalent circuit of solar PV

As shown in the fig-1, IPV stands for PV shortcircuits current, Id is a diode current, Rs means the series resistance of photovoltaic cells, Rsh represents the photovoltaic battery parallel resistance; the internal value is less than 1 Ω. The equation governing the behavior of photovoltaic cell is expressed as

$$I = I_{PV} - I_0 \left[e^{\frac{q\,V+IR_s}{AKT}} - 1 \right] - \frac{V + IR_s}{R_{sh}} \qquad (1)$$

Where, IPV= Photo-generated current (A)
I= Cell output current (A)
I0=Diode Saturation Current (A)
V=Cell Output Voltage (V)
Rs=Series Resistor (Ω)
e= Electron Charge 1.6×10-19 (coul)
K=Boltzman Constant (j/K)
T=cell temperature

Many research works are focusing in the development of the efficient control algorithms for high performance variable speed induction motor (IM) drives. Induction motor has been operated as a work horse in the industry due to its easy build, high robustness and generally satisfactory efficiency. Recent development of high speed power semi conductor devices, three phase inverters take part in the key role for variable speed AC motor drives. Traditionally, Three Phase inverters with six switches (SSTP) have been commonly utilized for variable speed IM drives; this involves the losses of the six switches as well as the complexity of the control algorithms and interface circuits to generate six PWM logic signals. So far researchers mainly concentrated on the development of new control algorithms. However, the cost, simplicity and flexibility of the overall drive system which are some of the most important factors did not get that much attention from the researchers. That is why, despite tremendous research in this area, most of the developed control system failed to attract the industry. Thus, the main issue of this work is to develop a cost effective, simple and efficient high performance IM drive.

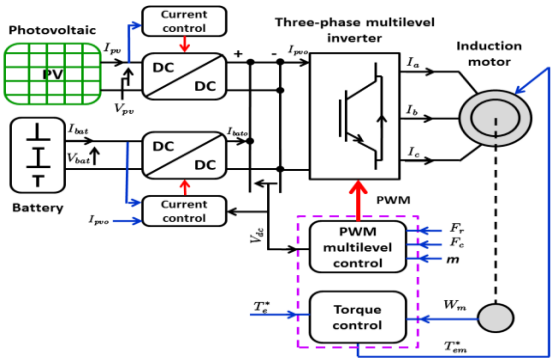


Fig. 2: Induction motor driven by PV-batteries standalone system using a controlled multilevel inverter

II. MULTILEVEL INVERTER CONTROL STRATEGIES

A. The three-level inverter control strategy:

Fig. 2 shows a three-phase three-level inverter. It has three arms. Each arm has four switches. Every switch is connected in antiparallel with a diode. This paragraph describes the operation of one of the legs shown at Fig. 4. The voltage Vao between the phase "a" and the neutral point O is defined entirely by the switches position (0 'open' or 1'closed'). Switch sets [S11,S13], and [S12,S14] have complementary positions. When [S11,S13] are open [S12,S14]are closed. The three-level NPC inverter is mostly used [10] for medium-voltage high-power applications.

In this converter, the number of commutation sequences (Seq) is equal to 2^4= 16., where 4 stands for the number of switches per arm and 2 is the number of state per switch (0, 1). Vdc is the DC-bus voltage. Only three commutation sequences are possible. They are represented at Table 1.

Fig. 4 shows the configurations of the inverter's arm which correspond to the three possible commutation sequences:
- Sequence 1: S_{11},S_{12} conduct and S_{13} ,S_{14} open (Fig. 4.a). V_{a0}=+Vdc/2.
- Sequence 2: S_{12} , S_{13}conduct and S_{11}, S_{14} open (Fig. 4.b). V_{a0} = 0.
- Sequence 3: S_{13} , S_{14} conduct and S_{11} ,S_{12} open (Fig. 4.c). V_{a0}=-Vdc/2.

Sequences 1, 2 and 3 are applied in this order periodically.

A pulse width modulation is used to control the switches. Consider Fig. 5 and Fig.6, the reference voltage Vra is compared to the positive and negative sawtooth carrier Vcx and Vcy respectively. The comparator output is sent to the switches (Insulated Gate Bipolar Transistor or IGBT) to generate the machine phase voltage. The modulated SPWM voltage has the following characteristics:
- SPWM pulses frequency is the same as the sawtooth carrier fc. The magnitude is 1 (f_{SPWM}= f_C, |Vpwm|=1)
- the fundamental frequency is controlled by fr which is the same as the reference voltage where Ar and Ar are the peak to peak value of Vao and Vc respectively frequency.

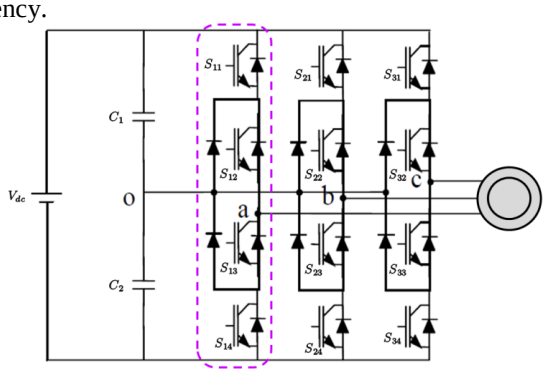
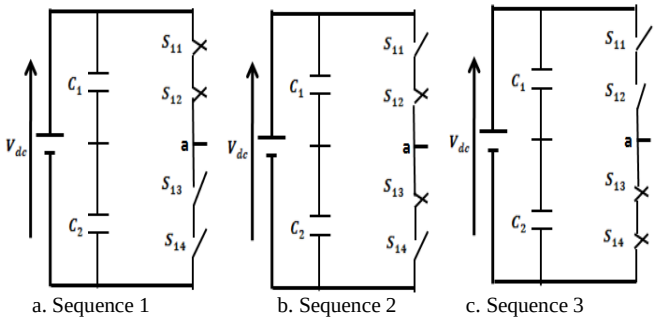


Fig. 3: Three-level three phase inverter



a. Sequence 1 b. Sequence 2 c. Sequence 3

Fig. 4: Different possible configurations for one arm

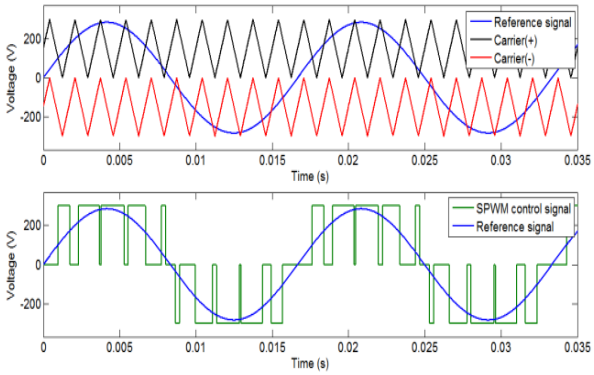


Fig. 5: Three-level SPWM control method

TABLE 1: Sequences of control vectors

S	$(S_{11}\ S_{12}\ S_{13}\ S_{14})$	V_{ao}
1	[1 1 0 0]	V_{ao}
2	[0 1 1 0]	$V_{ao}=0$
3	[0 0 1 1]	V_{ao}

The inverter output voltages are written as follow (1):

$$\begin{cases} V_{ao} = \frac{1}{3}(V_{ab} - V_{ca}) \\ V_{bo} = \frac{1}{3}(V_{bc} - V_{ab}) \\ V_{co} = \frac{1}{3}(V_{ca} - V_{bc}) \end{cases} \quad (1)$$

Modulation index (ma) is defined by (2):

$$m_a = \frac{A_r}{(n-1)A_c} \quad (2)$$

B. The higher level inverter control strategy:

The previous study for the three-level voltage inverter is now extended to higher level inverters. For an n-level inverter, it is possible to determine the number of components that are needed per arm (number of switches, diodes, carrier, etc).

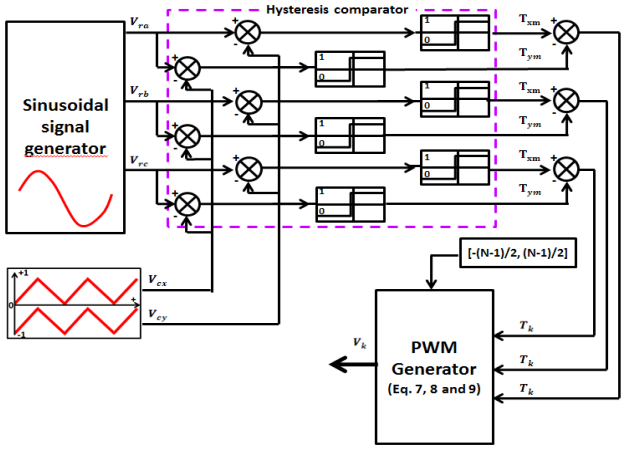


Fig. 6: Principle SPWM multilevel inverter control

Numbers of inverter components calculation:

Define Seq as the number of commutation sequence possibilities. S is the number of secondary voltage sources. K stands for the number of switches per phase. D is the number of diodes loop including the diode switches per phase. C represents the magnitude of the voltage across each capacitor and P is the number of carriers.

The following equations provide how these quantities are calculated and table 2 shows the values for several multilevel inverters.

$$\begin{cases} S_{eq} = 2^{(n+1)} \\ S = P = n-1 \\ K = 2(n-1) \\ D = 4n-6 \\ C = \frac{V_{dc}}{n-1} \end{cases} \quad (3)$$

TABLE 2: Sequences of control vectors

n	S_{eq}	S=P	K	D	C
3	16	2	4	6	$V_{dc}/2$
5	64	4	8	14	$V_{dc}/4$
7	256	6	12	22	$V_{dc}/6$
9	1024	8	16	30	$V_{dc}/8$
11	4096	10	20	38	$V_{dc}/10$
15	65536	14	28	54	$V_{dc}/14$

- Calculation of carrier :

A bipolar sawtooth carrier is illustrated at Fig 7.
The voltages Vc,xand Vc,y have the expression given by equation (4):

$$\begin{cases} V_{cx} = \sum_{x=2}^{h} V_{cx-1} + 1 \\ V_{cy} = \sum_{y=-2}^{-h} V_{cy-1} - 1 \end{cases} \quad (4)$$

- Calculation of reference voltages :

The balanced three-phase reference voltage is given by (5):

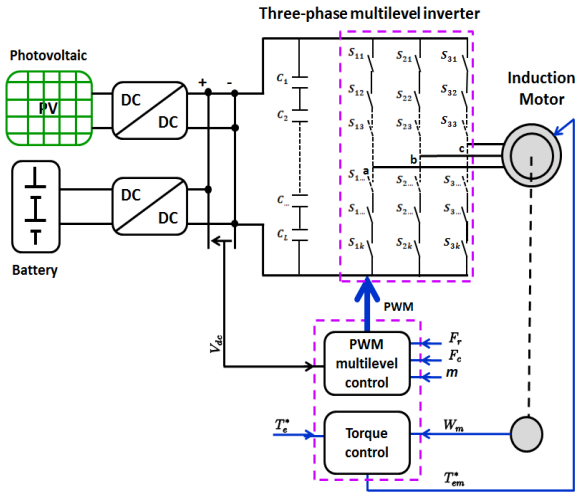


Fig. 7: Diagram of the induction motor control principle based on the multilevel inverter

$$V_r : \begin{cases} V_{ra}(t) = A_r Sin(2\pi f_r t) \\ V_{rb}(t) = A_r Sin\left(2\pi f_r t - \frac{2\pi}{3}\right) \\ V_{rc}(t) = A_r Sin\left(2\pi f_r t - \frac{4\pi}{3}\right) \end{cases} \quad (5)$$

where Vr is the three phase reference voltage.

- Calculation of the comparator :

The comparator uses the reference and carrier signals to generate a binary signal according to the following equation:

$$\begin{cases} If\ V_r \geq V_{cx} => T_{xm} = 1 \\ or \\ If\ V_r < V_{cx} => T_{xm} = 0 \\ and \\ If\ V_r \leq V_{cy} => T_{ym} = 1 \\ or \\ If\ V_r > V_{cy} => T_{ym} = 0 \end{cases} \quad (6)$$

where matrices Txm and Tym are the comparator output**.**

- Calculation of the adder :

The parameter Tkis the difference between Txm and Tym . It is therefore calculated as follows.

$$T_k = T_{xm} - T_{ym} \quad (7)$$

Calculation of inverter control vectors:

The generation of the pulse vector that control the inverter is very important. The pulse vector can be generated by applying the Gn vector for each Tk according equation (8). The inverter output voltage Vk is given by equation (9).

$$If\ T_k = \frac{n-1}{2} - i => \begin{cases} G_1 = [0 \ldots 0\ 1 \ldots 1] \\ G_2 = [1 \ldots 0\ 0 \ldots 1] \\ G_3 = [1 \ldots 0\ 0 \ldots 1] \\ \ldots \\ G_n = [1 \ldots 1\ 0 \ldots 0] \end{cases} \quad (8)$$

$$V_k = \frac{h - i}{n - 1} V_{dc} \quad (9)$$

Where $h = \frac{n-1}{2}, i = \{0, 1, 2, \ldots, n-1\}$

and Gn is 1x2(n-1) vector. It contains 1x(n-1) zero vector and 1x(n-1) ones vector.

III. CASCADED H-BRIDGE MULTILEVEL INVERTER

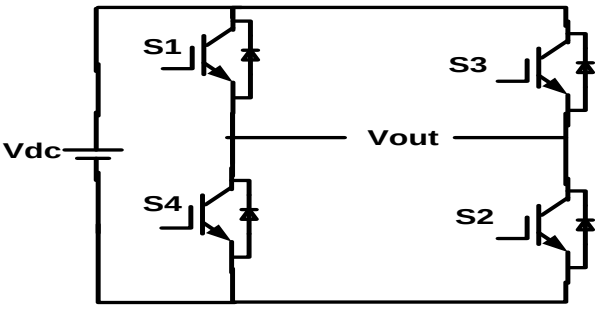


Fig. 8 Circuit of the single cascaded H-Bridge Inverter

Fig.8 shows the circuit model of a single CHB inverter configuration. By using single H-Bridge we can get 3 voltage levels. The number of output voltage levels of CHB is given by 2n+1 and voltage step of each level is given by Vdc/2n, where n is number of H-bridges connected in cascaded. The switching sequence is given in Table-I.

Table-I Switching table of single CHB inverter

Switches Turn ON	**Voltage Level**
S1,S2	Vdc
S3,S4	-Vdc
S4,D2	0

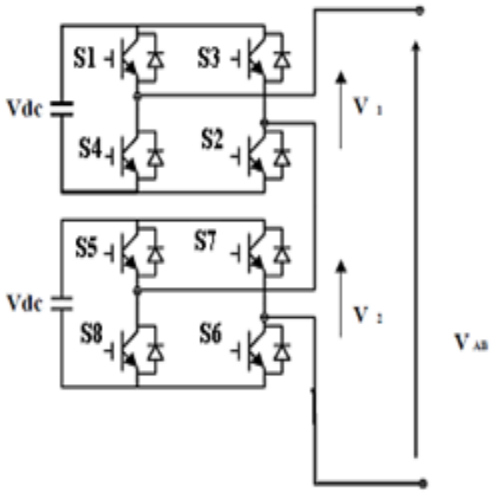


Fig-9 Block diagram of 5-level CHB inverter model

The switching mechanism for 5-level CHB inverter is shown in Table-2.

Table-2:- Switching sequence for 5-level CHB Inverter

Switches Turn On	**Voltage Level**
S1, S2	Vdc
S1,S2,S5,S6	2Vdc
S4,D2,S8,D6	0
S3,S4	-Vdc
S3,S4,S7,S8	-2Vdc

A. PWM Techniques for CHB Inverter

The most popular PWM techniques used for CHB inverter are 1. Phase Shifted Carrier PWM (PSCPWM), 2. Level Shifted Carrier PWM (LSCPWM)

Case-1:- Phase Shifted Carrier PWM (PSCPWM)

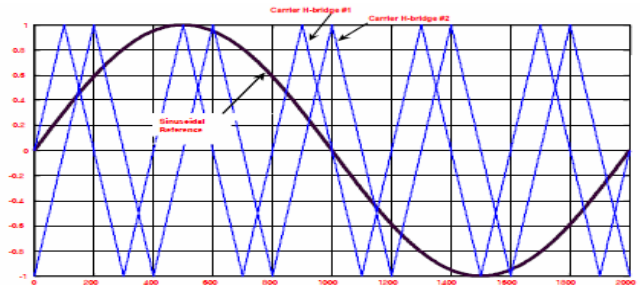


Fig-10 Phase Shifted Carrier PWM

Fig-10 shows the PSCPWM. In general, a multilevel inverter with *m* voltage levels requires (*m*–1) triangular carriers. In the PSCPWM, all the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by $\varphi_{cr}=360^0/(m–1)$. The modulating signal is usually a three-phase sinusoidal wave with adjustable amplitude and frequency. The gate signals are generated by comparing the modulating wave with the carrier waves. It means for five-level inverter, four triangular carriers are needed with a 90° phase displacement between any two adjacent carriers. In this case the phase displacement of V_{cr1} = 0°, V_{cr2} = 90°, V_{cr1-} = 180° *and* V_{cr2-} = 270°.

Case-2:- Level Shifted Carrier PWM (LSCPWM)

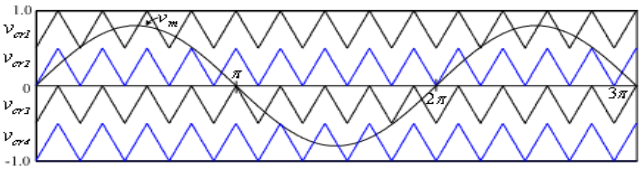


Fig-11 Level shifted carrier PWM (IPD)

Fig-11 shows the LSCPWM. The frequency modulation index is given by

$$m_f = f_{cr} / f_m, \qquad (10)$$

where f_m is modulating frequency and f_{cr} are carrier waves frequency. The amplitude modulation index 'm_a' is defined by

$$m_a = V_m / V_{cr}\ (m\text{-}1) \qquad \text{for } 0 \le m_a \le 1 \qquad (11)$$

Where V_m is the peak value of the modulating wave and V_{cr} is the peak value of the each carrier wave [1]. The amplitude modulation index, m_a is 1 and the frequency modulation index, m_f is 6. The triggering circuit is designed based on the three phase sinusoidal modulation waves V_a, V_b, and V_c. The sources have been obtained with same amplitude and frequency but displaced 120° out of the phase with each others. For carriers signals, the time values of each carrier waves are set to [0 1/600 1/300] while the outputs values are set according to the disposition of carrier waves. After comparing, the output signals of comparator are transmitted to the IGBTs. Figs 11 and 12, 13 show the waveforms based on three schemes of LSCPWM: (a) in phase disposition (IPD) fig-9, where all carriers are in phase; (b) alternative phase opposite disposition (APOD) fig-10, where all carriers are alternatively in opposite disposition; and (c) phase opposite disposition (POD) fig-11, where all carriers above zero reference are in phase but in opposition with those

below the zero reference [1]. Out of IPD, APOD and POD; the authors studied that, IPD give better harmonic performance.

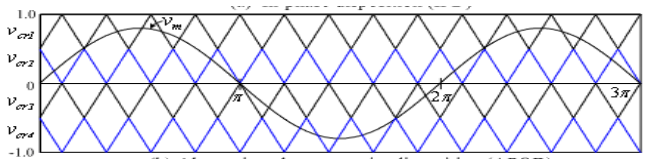


Fig. 12 Alternative Phase Opposite Disposition (APOD)

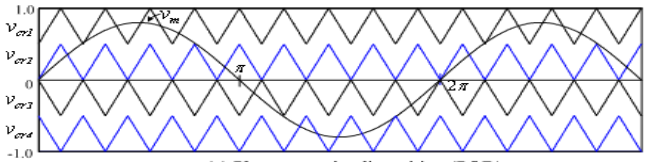


Fig. 13 Phase Opposite Disposition (POD)

VI.MATLAB MODELING AND SIMULATION RESULTS

Here simulation is carried out in two different configurations, 1). Implementation of Proposed Concept using Neutral Clamped Type Multilevel Inverter. 2). Implementation of Proposed Concept using Cascaded H-Bridge Multilevel Type Inverter.

Case 1: Implementation of Proposed Concept using Neutral Clamped Type Multilevel Inverter.

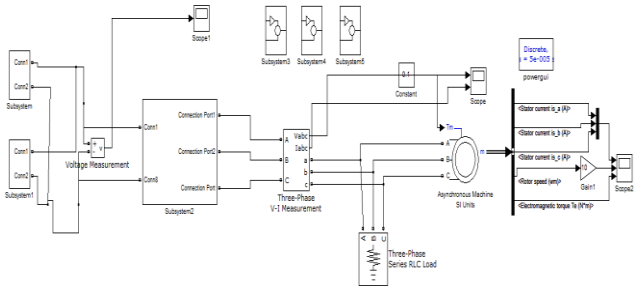


Fig. 14 Matlab/Simulink Model of Proposed NPC Converter with Induction Machine Drive

Fig.14 shows the Matlab/Simulink Model of Proposed NPC Converter with Induction Machine Drive.

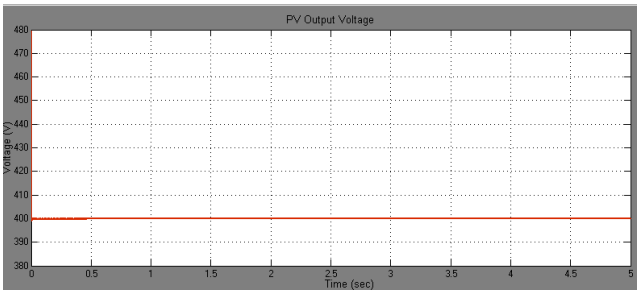


Fig.15 PV Output Voltage

Fig.15 Output Voltage coming from PV arrays with the help of high step up DC/DC Converter and directly fed to our proposed inverter.

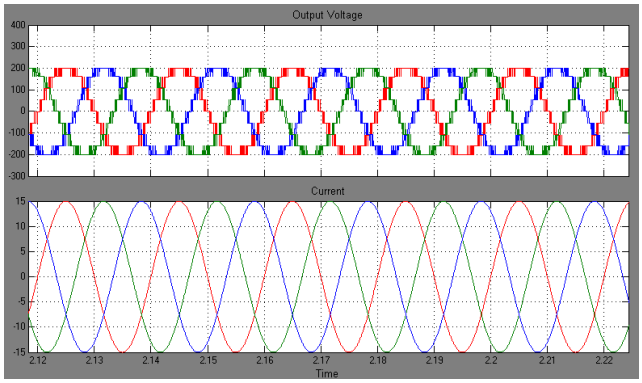


Fig.16 Level Output Voltage and Current

Fig. 16 shows the 9-Level Output Voltage and current coming from the proposed NPC multilevel inverter.

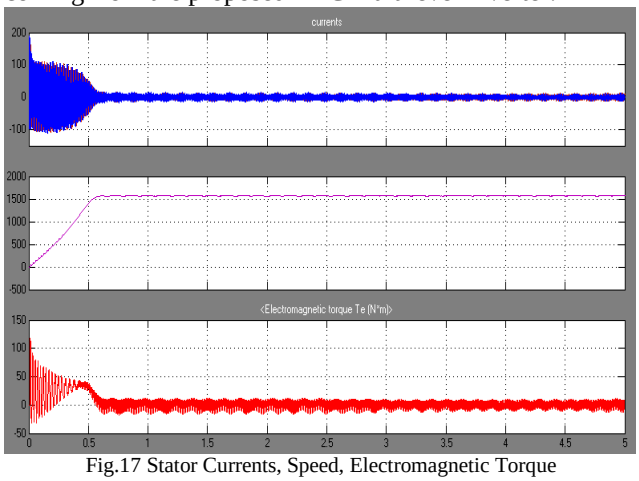


Fig.17 Stator Currents, Speed, Electromagnetic Torque

Fig.17 shows the Stator Currents, Speed, and Electromagnetic Torque of the proposed NPC Strategy Controlled Drive Performance Characteristics.

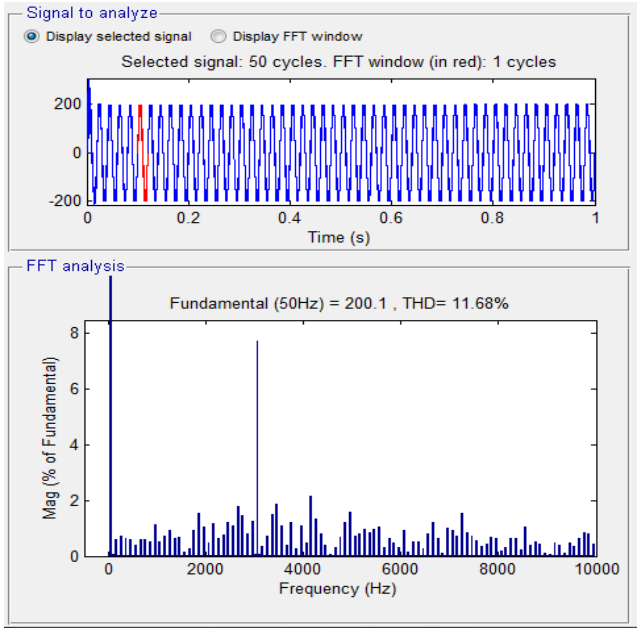


Fig. 18 FFT Analysis of Proposed NPC Converter Output Voltage

Fig. 18 shows the FFT Analysis of Proposed NPC Converter Output Voltage, we get 15.18% no need of any filter we get this value.

Case 2: Implementation of Proposed Concept using Cascaded H-Bridge Multilevel Type Inverter

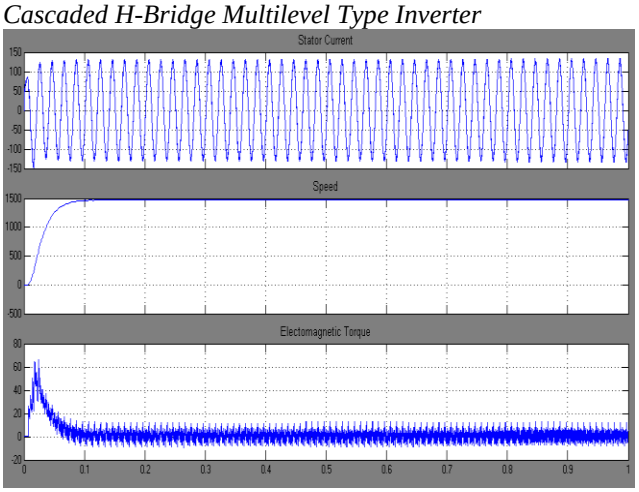


Fig.19 Stator Currents, Speed, Electromagnetic Torque

Fig.19 shows the Stator Currents, Speed, and Electromagnetic Torque of the proposed CHB Multilevel Inverter to Controlled Drive Performance Characteristics.

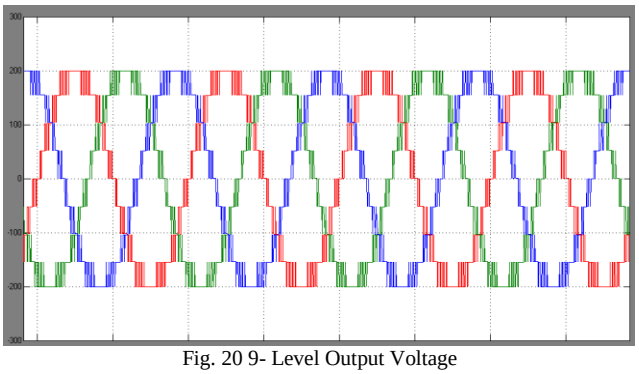


Fig. 20 9- Level Output Voltage

Fig. 20 shows the 9-Level Output Voltage and coming from the proposed CHB Multilevel Inverter.

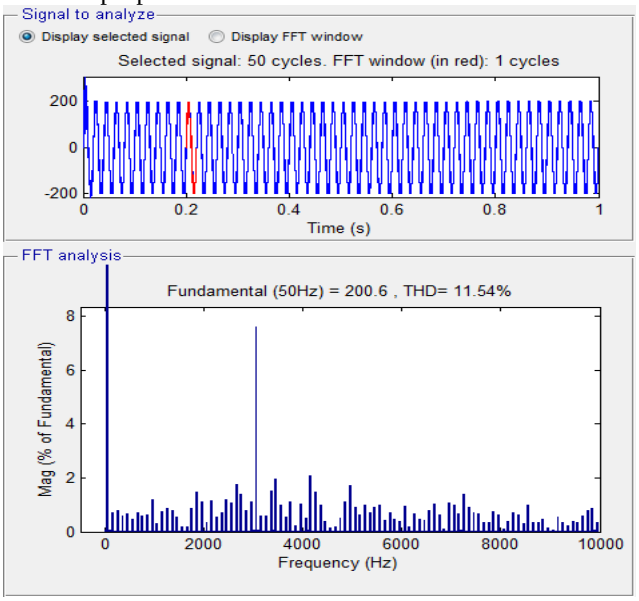


Fig. 21 FFT Analysis of Proposed CHB Multilevel Converter Output Voltage

Fig. 21 shows the FFT Analysis of Proposed CHB Multilevel Converter Output Voltage, we get 15.18% no need of any filter we get this value.

VII. CONCLUSION

In this paper, a general multilevel SPWM control algorithm for *9-level* inverter has been modelled and simulated using Matlab®/Simulink with different topologies. This algorithm can generate automatically SPWM pulses for any level of inverter by changing only a parameter *n* which is the number of inverter level. Simulation of nine inverter of NPC topology and CHB Multilevel Converter is connected to induction motor has been performed and the generated signals THD is analysed. The system is supplied by a PV panel and batteries bank. That gives energy autonomy to the system. Simulation results give a better quality of stator current in terms of low harmonics, thus reducing the adverse effects on of the machine life and eventually the electrical network which supplies it, and reduces the switch count, low switching losses, etc.

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