Single-Phase 13-Level Grid-Connected Inverter For Photovoltaic System

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Abstract: **This paper proposes a single-phase 13-level inverterfor grid-connected photovoltaic systems, with a novelpulsewidth-modulated (PWM) control scheme. Three referencesignals that are identical to each other with an offset thatis equivalent to the amplitude of the triangular carrier signalwere used to generate the PWM signals. The inverter is capable of producing thirteen levels of output-voltage levels (V_{dc}, $5V_{dc}/6$, $2V_{dc}/3$, $V_{dc}/2$, $V_{dc}/3$, $V_{dc}/6$, 0, $-V_{dc}/6$, $-V_{dc}/3$, $-V_{dc}/2$, $-2V_{dc}/3$, $-5V_{dc}/6$, $-V_{dc}$) from the dc supply voltage. A digital proportional–integral current-control algorithm was used to keep the current injected into the grid sinusoidal. The proposed system wasverified through simulation.**

***Keywords*— Grid connected, modulation index, multilevel inverter, photovoltaic (PV) system, pulsewidth-modulated (PWM),total harmonic distortion (THD).**

I.INTRODUCTION

The ever-increasing energy consumption, fossil fuels soaring costs and exhaustible nature, and worsening global environment have created a booming interest in renewableenergy generation systems, one of which is photovoltaic.Such a system generates electricity by converting the Sun's energydirectly into electricity. Photovoltaic-generated energy canbe delivered to power system networks through grid-connectedinverters.

A single-phase grid-connected inverter is usually used for residential or low-power applications of power ranges that are less than 10 kW [1]. Types of single-phase grid-connected inverters have been investigated [2]. A common topology of this inverter is full-bridge three-level. The three-level inverter can satisfy specifications through its very high switching, but it could also unfortunately increase switching losses, acoustic noise, and level of interference to other equipment. Improving its output waveform reduces its harmonic content and, hence, also the size of the filter used and the level of electromagnetic interference (EMI) generated by the inverter's switching operation [3].

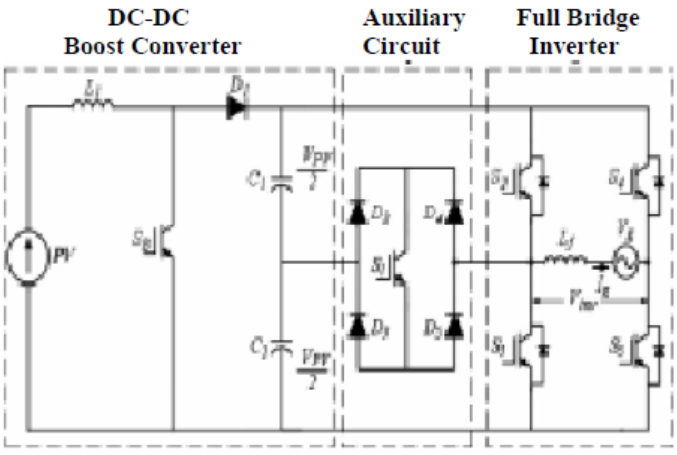

Fig. 1. Proposed single-phase grid-connected inverter for photo voltaic systems.

Multilevel inverters are promising; they have nearly sinusoidaloutput-voltage waveforms, output current with betterharmonic profile, less stressing of electronic components owingto decreased voltages, switching losses that are lower than thoseof conventional two-level inverters, a smaller filter size,

andlower EMI, all of which make them cheaper, lighter, and morecompact [3], [4].

Various topologies for multilevel inverters have been proposed over the years. Common ones are diode-clamped [5]– [10], flying capacitor or multi cell [11]–[17], cascaded H-bridge [18]–[24], and modified H-bridge multilevel [25]–[29]. This paper recounts the development of a novel modified H-bridge single-phase multilevel inverter that has two diode embedded bidirectional switches and a novel pulse width modulated (PWM) technique. The topology was applied to a grid-

Connected photovoltaic system with considerations for a maximum-power-point tracker (MPPT) and a current-control algorithm.

II. PROPOSED MULTILEVEL INVERTER TOPOLOGY

The proposed single-phase 13-level inverter was developed from the seven-level inverter in [25]–[29]. It comprises a single-phase conventional H-bridge inverter, six bidirectional switches, and a capacitor voltage divider formed by *C*1, *C*2, *C*3, C4, C5, and C6. The modified H-bridge topology is significantly advantageous over other topologies, i.e., less power switch, power diodes, and less capacitors for invertersof the same number of levels.

Photovoltaic (PV) arrays were connected to the inverter via a dc–dc boost converter. The power generated by the inverter is to be delivered to the power network, so the utility grid, rather than a load, was used. The dc–dc boost converter was required because the PV arrays had a voltage that was lower than the grid voltage. High dc bus voltages are necessary to ensure that power flows from the PV arrays to the grid. A filtering inductance *Lf* was used to filter the current injected into the grid. Proper switching of the inverter can produce seven output-voltage levels (*V*dc, 5*V*dc/6, *2V*dc/3, *V*dc/2, *V*dc/3, *V*dc/6, 0, −*V*dc/6,−*V*dc/3, −*V*dc/2, −*2V*dc/3, −5*V*dc/6, −*V*dc) from the dc supply voltage. The proposed inverter's operation can be divided into nine switching states. The required nine levels of output voltage were generated as follows.

1) *Maximum positive output (Vdc):* S1 is ON; connecting the load positive terminal to Vdc, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is Vdc.

2) *Five-sixth positive output (5Vdc/6):* The bidirectional switch S5 is ON, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is 5Vdc/6.

3) *Two-Third of the positive output (2Vdc/3):* The bidirectional switch S6 is ON, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is 2Vdc/3.

4) *Half of the positive output (Vdc/2):* The bidirectional switch S7 is ON, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is Vdc/2.

5) *One-third of the positive output (Vdc/3):* The bidirectional switch S8 is ON, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is Vdc/3.

6) *One-sixth of the positive output (Vdc/6):* The bidirectional switch S6 is ON, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground.All other controlled switches are OFF; the voltage applied to the load terminals is Vdc/6.

7) *Zero output:* This level can be produced by two switching combinations; switches S3 and S4 are ON, or S1 andS2 are ON, and all other controlled switches are OFF; terminal ab is a short circuit, and the voltage applied to the load terminals is zero.

8) *One-sixth of the negative output (-Vdc/6):* The bidirectional switch S5 is ON, connecting the load positive terminal, and S2 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is -Vdc/6.

9) *One-third of the negative output (-Vdc/3):* The bidirectional switch S6 is ON, connecting the load positive terminal, and S2 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is -Vdc/3.

10) Half of the negative output (-Vdc/2): The bidirectional switch S7 is ON, connecting the load positive terminal, and S2 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is -Vdc/2.

11) *Two-Third of the negative output (-2Vdc/3):* The bidirectional switch S8 is ON, connecting the load positive terminal, and S2 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is -2Vdc/3.

12) Five-sixth of the negative output (-5Vdc/6): The bidirectional switch S9 is ON, connecting the load positive terminal, and S2 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is -5Vdc/6.

13) *Maximum negative output (- Vdc):* S3 is ON; connecting the load positive terminal to Vdc, and S2 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is -Vdc.

TABLE I
OUTPUT VOLTAGE ACCORDING TO THE SWITCHES' ON–OFF CONDITION

Table I shows the switching combinations that generated the thirteen output-voltage levels (*V*dc, 5*V*dc/6, *2V*dc/3, *V*dc/2, *V*dc/3, *V*dc/6, 0, −*V*dc/6,−*V*dc/3, −*V*dc/2, −*2V*dc/3, −5*V*dc/6, −*V*dc) from the dc supply voltage.

Vo	S1	S2	S3	S4	S5	S6	S7	S8	S9
Vdc	*on*	*off*	*off*	*On*	*Off*	*Off*	*Off*	*Off*	*Off*
5Vdc/6	*Off*	*Off*	*Off*	*On*	*On*	*Off*	*Off*	*Off*	*Off*
2Vdc/3	*Off*	*Off*	*Off*	*On*	*Off*	*On*	*Off*	*Off*	*Off*
Vdc/2	*Off*	*Off*	*Off*	*On*	*Off*	*Off*	*On*	*Off*	*Off*
Vdc/3	*Off*	*Off*	*Off*	*On*	*Off*	*Off*	*Off*	*On*	*Off*
Vdc/6	*Off*	*Off*	*Off*	*On*	*Off*	*off*	*Off*	*Off*	*On*
zero	*Off*	*Off*	*On*	*On*	*Off*	*Off*	*Off*	*Off*	*Off*
-Vdc/6	*Off*	*On*	*Off*	*Off*	*On*	*Off*	*Off*	*Off*	*Off*
-Vdc/3	*Off*	*On*	*Off*	*Off*	*Off*	*On*	*Off*	*Off*	*Off*
-Vdc/2	*Off*	*On*	*Off*	*Off*	*Off*	*Off*	*On*	*Off*	*Off*
-2Vdc/3	*Off*	*On*	*Off*	*Off*	*Off*	*Off*	*Off*	*On*	*Off*
-5Vdc/6	*Off*	*On*	*Off*	*Off*	*Off*	*Off*	*Off*	*Off*	*On*
- Vdc	*Off*	*On*	*On*	*Off*	*Off*	*Off*	*Off*	*Off*	*off*

III. PWM MODULATION

A novel PWM modulation technique was introduced to generate the PWM switching signals. Three reference signals (*V*ref1, *V*ref2, and *V*ref3) were compared with a carrier signal (*Vcarrier*). The reference signals had the same frequency and amplitude and were in phase with an offset value that was equivalent to the amplitude of the carrier signal. The reference signals were each compared with the carrier signal. If *V*ref1 had exceeded the peak amplitude of *V*carrier, *V*ref2 was comparedwith *V*carrier until it had exceeded the peak amplitude of *V*carrier. Then, onward, *V*ref3 would take charge and would be compared with *V*carrier until it reached zero. Once *V*ref3 had reached zero, *V*ref2 would be compared until it reached zero.Then, onward, *V*ref1 would be compared with *V*carrier. Fig. 3 shows the resulting switching pattern. Switches *S*1, *S*3, *S*5, and *S*6 would be switching at the rate of the carrier signal frequency, whereas *S*2 and *S*4 would operate at a frequency that was equivalent to the fundamental frequency.

For one cycle of the fundamental frequency, the proposed inverter operated through six modes. Fig. 4 shows the perunit output-voltage signal for one cycle. The six modes are described as follows:

Mode 1 : $0 < \omega t < \theta 1$ and $\theta 4 < \omega t < \pi$
Mode 2 : $\theta 1 < \omega t < \theta 2$ and $\theta 3 < \omega t < \theta 4$
Mode 3 : $\theta 2 < \omega t < \theta 3$
Mode 4 : $\pi < \omega t < \theta 5$ and $\theta 8 < \omega t < 2\pi$
Mode 5 : $\theta 5 < \omega t < \theta 6$ and $\theta 7 < \omega t < \theta 8$
Mode 6 : $\theta 6 < \omega t < \theta 7$. **(1)**

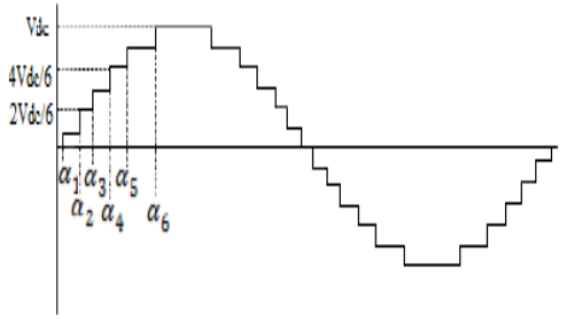

Fig 2. Ideal 13- level inverter output voltages

The phase angle depends on modulation index *Ma*. Theoretically, for a single reference signal and a single carrier signal, the modulation index is defined to be

$$Ma = Am / Ac \qquad (2)$$

While for a single-reference signal and a dual carrier signal, the modulation index is defined to be [26]–[29]

$$Ma = Am/2Ac \qquad (3)$$

Since the proposed thirteen-level PWM inverter utilizes three carrier signals, the modulation index is defined to be

$$Ma = Am/3Ac \qquad (4)$$

Where *Ac* is the peak-to-peak value of the carrier signal and *Am* is the peak value of the voltage reference signal *V*ref.

For *Ma* that is equal to, or less than, 0.33, only the lower reference wave (*V*ref3) is compared with the triangular carrier signal. The inverter's behaviour is similar to that of a conventional full-bridge three-level PWM inverter. However, if *Ma* is more than 0.33 and less than 0.66, only *V*ref2 and *V*ref3 reference signals are compared with the triangular carrier wave. The output voltage consists of five dc-voltage levels. The modulation index is set to be more than 0.66 for seven levels of output voltage to be produced. Three reference signals have to

be compared with the triangular carrier signal to produce switching signals for the switches.

IV. CONTROL SYSTEM

As Fig. 5 shows, the control system comprises a MPPT algorithm, a dc-bus voltage controller, reference-current

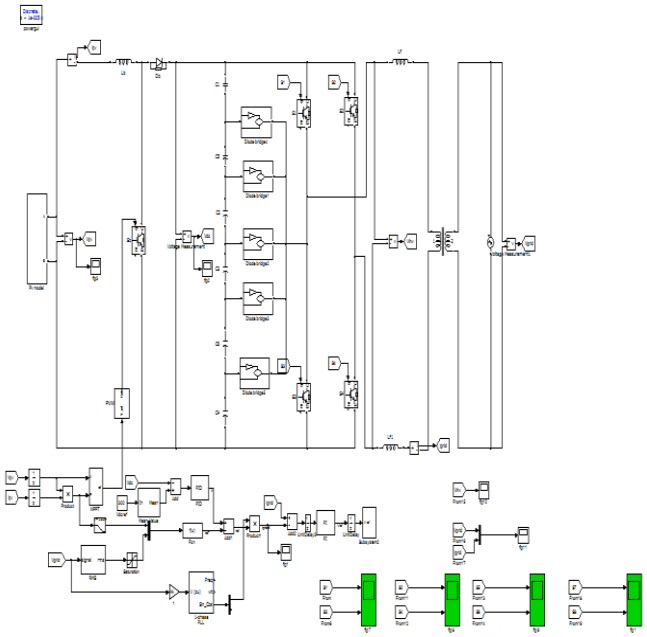

Fig 3. mat lab circuit of 13- level grid connected inverter

Generation, and a current controller. The two main tasks of the control system are maximization of the energy transferred from the PV arrays to the grid, and generation of a sinusoidal current with minimum harmonic distortion, also under the presence of grid voltage harmonics.

The proposed inverter utilizes the perturb-and-observe(P&O) algorithm for its wide usage in MPPT owing to its simple structure and requirement of only a few measured parameters. It periodically perturbs (i.e., increment or decrement) the array terminal voltage and compares the PV output power with that of the previous perturbation cycle. If the power was increasing, the perturbation would continue in the same direction in the next cycle; otherwise, the direction would be reversed. This means that the array terminal voltage is perturbed every MPPT cycle; therefore, when the MPP is reached, the P&O algorithm will oscillate around it.

The P&O algorithm was implemented in the dc–dc boost converter. The output of the MPPT is the duty-cycle function. As the dc-link voltage *V*dc was controlled in the dc–ac thirteen level PWM inverter, the change of the duty cycle changes the voltage at the output of the PV panels. A PID controller was implemented to keep the output voltage of the dc–dc boost converter (*V*dc) constant by comparing *V*dc and *V*dc ref and feeding the error into the PID controller, which subsequently tries to reduce the error. In this way, the *V*dc can be maintained at a constant value and at more than √2 of *V*grid to inject power into the grid.

To deliver energy to the grid, the frequency and phase of the PV inverter must equal those of the grid; therefore, a grid synchronization method is needed. The sine lookup table that generates reference current must be brought into phase with the grid voltage (*V*grid). For this, the grid period and phase must be detected.

A PI algorithm was used as the feedback current controller for the application. The current injected into the grid, also known as grid current *I*grid, was sensed and fed back to a comparator that compared it with the reference current *I*gridref. *I*gridref is the result of the MPPT algorithm. The error from the comparison process of *I*grid and *I*gridref was fed into the PI controller. The output of the PI controller, also known as *V*ref , goes through an anti-windup process before being compared with the triangular wave to produce the switching signals for*S*1–*S*9. Eventually, *V*ref becomes *V*ref1; *V*ref2 and *V*ref3 can be derived from *V*ref1 by shifting the offset value, which was equivalent to the amplitude of the triangular wave. The mathematical formulation of the PI algorithm and its implementation in the DSP are discussed in detail in [28].

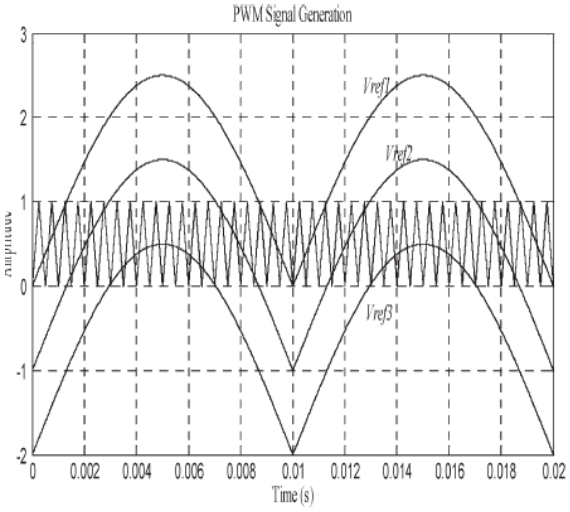

Fig 4.PWM switching signal generation

V. SIMULATION AND EXPERIMENTAL RESULTS

1). Simulation Results:

MATLAB SIMULINK simulated the proposed configuration before it was physically implemented in a prototype. The PWM switching patterns were generated by comparing three reference signals (*V*ref1, *V*ref2, and *V*ref3) against a triangular carrier signal (see Fig. 6). Subsequently, the comparing process produced PWM switching signals for switches *S*1–*S*6, as Figs. 7–9 show.

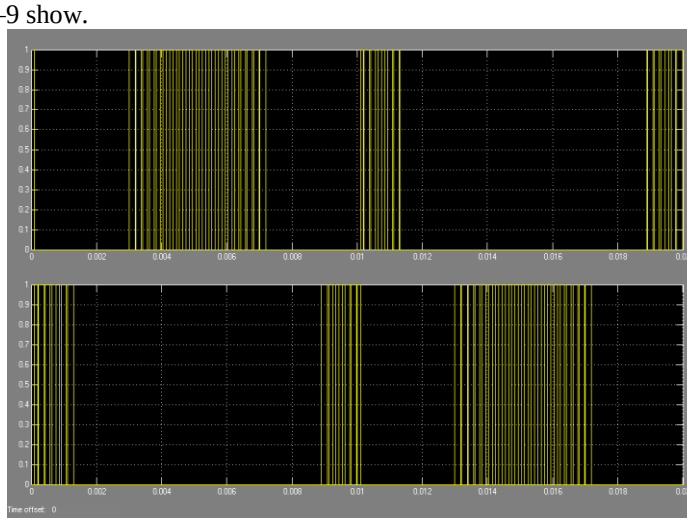

Fig5. PWM signals for *S*1 and *S*3

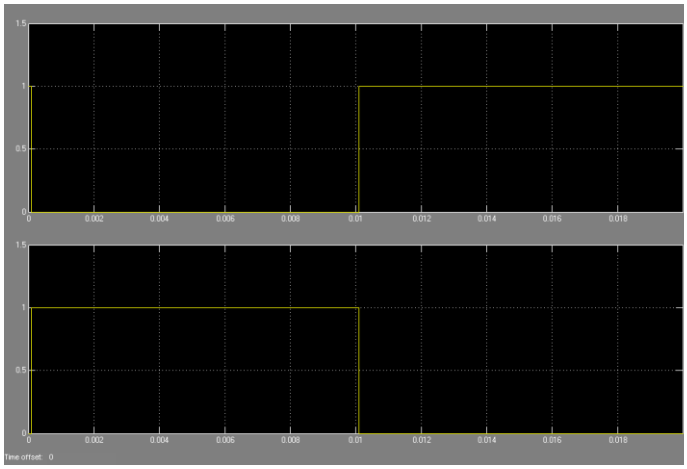

Fig 6. PWM signals for *S*2 and *S*4

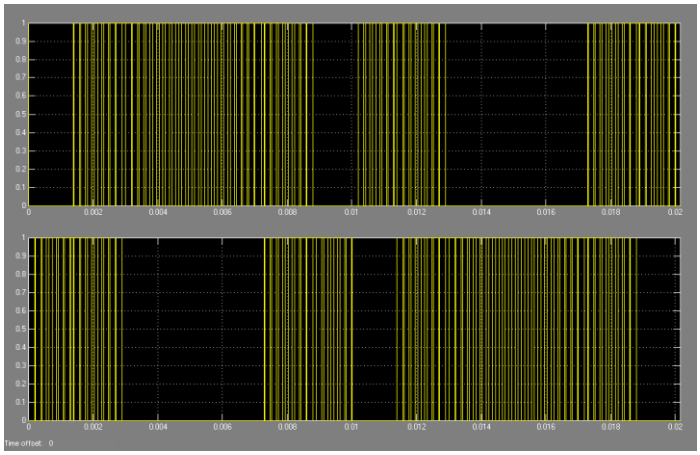

Fig 7. PWM signals for *S*5 and *S*6

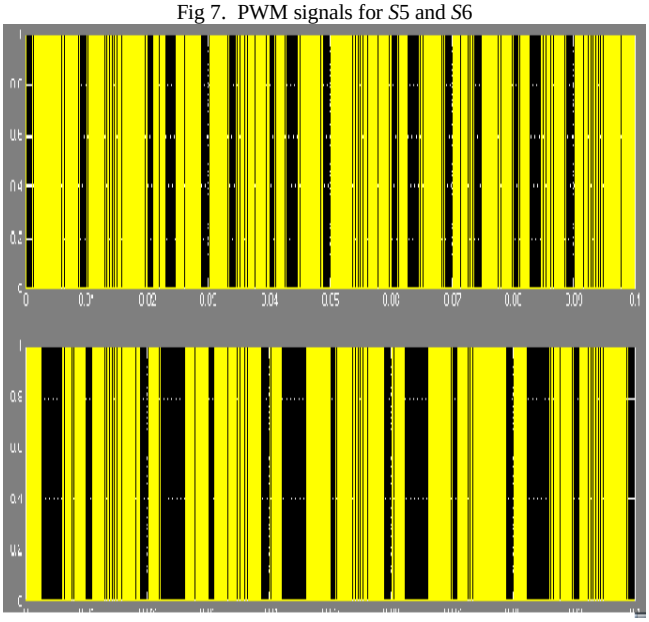

Fig 8. S7 and s8 switches operation of output wave forms

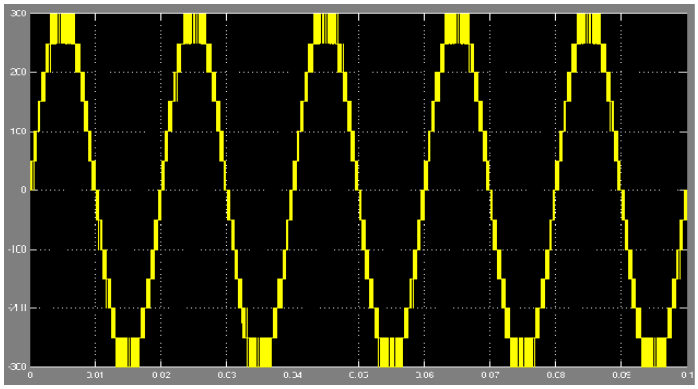

Fig 9. Thirteen-level output wave forms

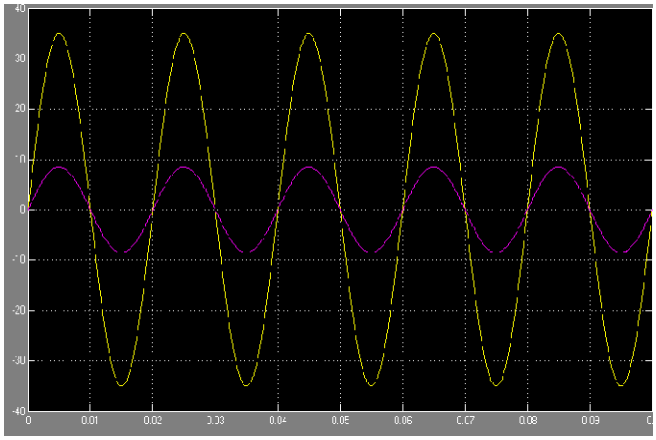

Fig 10. Voltage and current output wave forms

One leg of the inverter operated at a high switching rate that was equivalent to the frequency of the carrier signal, while the other leg operated at the rate of the fundamental frequency (i.e., 50 Hz). Switches *S*5 and *S*6 also operated at the rate of the carrier signal. Fig. 10 shows the simulation result of inverter output voltage *V*inv. The dc-bus voltage was set at 300 V (>√2*V*grid; in this case, *V*grid was 120 V). The dc-bus voltage must always be higher than √2 of *V*grid to inject current into the grid, or current will be injected from the grid into the inverter. Therefore, operation is recommended to be between *Ma* = 0.66 and *Ma*= 1.0. *V*inv comprises seven voltage levels, namely, *V*dc, 2*V*dc/3, *V*dc/3, 0, −*V*dc, −2*V*dc/3, and −*V*dc/3. The current flowing into the grid was filtered to resemble a pure sine wave in phase with the grid voltage (see Fig. 11). As *I*grid is almost a pure sine wave at unity power factor, the total harmonic distortion (THD) can be reduced compared with the THD in [28].

VI. CONCLUSION

Multilevel inverters offer improved output waveforms and lower THD. This paper has presented a novel PWM switching scheme for the proposed multilevel inverter. It utilizes three reference signals and a triangular carrier signal to generate PWM switching signals. The behaviour of the proposed multilevel inverter was analysed in detail. By controlling the modulation index, the desired number of levels of the inverter's output voltage can be achieved. The less THD in the 13-level inverter compared with that in the seven-level and five-level inverters is an attractive solution for grid-connected PV inverters.

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