Design and Analysis of Split-Capacitor model of a Tapper Buffer using 120 nm CMOS Technology

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Abstract: **This paper presents a design methodology and analytic relationships for the optimal tapering of cascaded buffers which consider the effects of local interconnect capacitance. The methodology utilizes analytical expressions for each of the performance criteria. The proposed buffer has been designed and simulated using Microwind3.5 in 120 nm CMOS /VLSI technology. The results show that modified taper buffer design provides 20% reduction in power dissipation as well as reduced propagation delay, are exhibited as compared with tapered buffers which neglect local interconnect capacitance**

Keywords**: Tapered buffer, CMOS, Microwind,**

I.INTRODUCTION

CMOS integrated circuits, large capacitive loads are often encountered. These large loads occur both on-chip, where high, localized fan-out and long global interconnect lines are common, and off-chip, where highly capacitive chip- to- chip communication lines exist. In order to drive these large capacitive loads at high speeds, buffer circuits are required which must quickly source and sink relatively large currents while not degrading the performance of previous stages. In CMOS, a tapered buffer system is often used to perform this task, particularly when the load is predominantly capacitive [l], [2] When the load is resistive, typically a long interconnect line, repeaters, a form of distributed buffer, rather than tapered buffers are used [3], [4].

The most commonly addressed criteria in tapered buffer design are propagation delay, power dissipation, physical area, and, quite recently, circuit reliability. Traditional design methods utilize analytic expressions to determine the tapering factor and the number of stages of a tapered buffer system; these parameters are the two primary variables in the design of tapered buffers. Unfortunately, the methods developed to deal with these different design constraints are quite diverse, do not deal with all four issues simultaneously, and often provide solutions which are in direct conflict. The primary result of this paper is the unification of these seemingly independent criteria into a single, integrated design methodology for determining an application-specific tapering factor and number of stages of a tapered buffer system for driving a wide range of capacitive load.

High-performance VLSI design is attracting much attention because of emerging need for miniaturization, and hence design optimization for trading-off power and performance in nanometer scale integrated circuits is the need of the present scenario, which demands a decrease in both supply voltage V_{DD} (to maintain low power dissipation) and threshold voltage V_{th} (to sustain propagation delay reduction), but the fact is that the decrease in V_{th} not only increases leakage power but also short circuit power. While working in nano scale technology the total power dissipation of clock drivers, which generally have CMOS inverters, is quite large and have 30 to 50% share only of leakage current and short circuit current [1,2]. To solve this problem of high power dissipation, a design scheme has been proposed, which not only minimizes short circuit power, and leakage power but also optimizes propagation delay [3, 4]. So our work presents a CMOS taper buffer design which considers the power dissipation as dominant cost function.

The rest of the paper is organized as follows: In section 2 taper buffer and its design aspects are discussed. Section 3 presents proposed CMOS taper buffer. The concept of power delay optimization is discussed in section 4.The results and discussions are reported in Section 5. Finally, concluding remarks are offered in section 6.

II. CMOS TAPERED BUFFER DESIGN

This section presents the conceptual details of CMOS taper buffer design. In this work, we have extended the split capacitor model of taper buffer given by [5]. The brief of this model is presented in Fig 1.

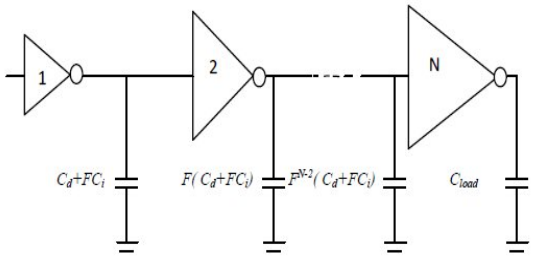

Figure 1. The split-capacitor model of a tapered buffer [15]

The buffer consists of a chain of inverter stages where width of each MOS transistor in a stage is increased by a constant factor (called taper factor) than that of the transistors in the previous stage. The model is named as split capacitor model as output capacitance and input capacitance of each stage is modeled separately. The constant increase in width of transistors in each stage provides fixed ratio of output current drive to output capacitance and hence equal rise, fall, and delay times for each stage. Here C_i denotes the input capacitance of minimum size inverter, C_d denotes the drain capacitance of minimum size inverter, C_{load} denotes the load capacitance of the last stage inverter, N denotes number of stages in the buffer chain and F denotes the scaling factor per stage in the inverter buffer chain. Design of taper buffer is based on analytical modeling of performance criteria and analyzing them individually with respect to the parameters like capacitive load dependent tapering factor and number of stages, which are the two primary variables in the design of tapered buffers for a specific application [6]. The design we have presented uses two different conditions. First condition is, when number of buffer stages are $N=ND$ to achieve minimum propagation delay irrespective of power dissipation. Second condition is, when number of buffer stages are $N=N_{opt}$ to minimize cost function.

The cost function is based on power (P), delay (D) product and is calculated depending on the weight of each component in the product which is given by

$$C = P^a \text{ X } P^b$$

If a =1 and b =2 then cost function becomes $PD2$ and is suitable for the applications where more weight is required to be given to propagation delay than to power dissipation. The number of buffer stages required in each of the two design conditions depends on technology dependent tapering factor F, load capacitance and input capacitance of buffer. The F is given by

$$F[\ln(F)-1]=\frac{C_d}{C_i}$$

Where C_d=drain C_i =gate capacitance and C_L=load capacitance.

For the first design condition to achieve minimum delay the number of stages required are given by [6] and are expressed as

$$N_D = \frac{\ln\left(\frac{C_L}{C_i}\right)}{Ln(F)}$$

Similarly for the second design condition to achieve minimum power delay product base on cost function C the number of stage used are

$$N_{opt} = \left[N_D\left(1-e^{-0.7\left(\frac{b}{a}\right)}\right)-1 \right]$$

For the design of taper buffer in 120nm technology node the different design parameter are V_{DD}=1 volt ,V_{th} value used is 0.2 volt , C_d =1fF ,C_i =1fF .range of capacitive load is C_l =15fF to 150000fF.

In first condition the transistor width of each inverter stage is increased by a factor F_D which depends on the number of stages used and ratio of load capacitance to the input capacitance [6] and is expressed as

$$F_D = \left(\frac{C_L}{C_i}\right)^{\frac{1}{N_{opt}}}$$

The propagation delay in the taper buffer can be calculated by

$$T_{delay} = NV_{DD}\frac{C_d+FC_i}{I_{D0}}\left[\left(\frac{9}{8}+\frac{V_{D0}}{0.8V_{D0}}\ln\left(\frac{10V_{D0}}{eV_{D0}}\right)\right)\left(\frac{1}{2}\frac{1-v_t}{1+\alpha}\right)+\frac{1}{2}\right]$$

Here I_{D0} is the drain saturation current at $V_{GS}=V_{DD}$,V_{DO} is the drain saturation voltage at $V_{GS}=V_{DD}$, V_t $=V_{th}/V_{DD}$ and α is velocity saturation index. The power dissipation in the taper buffer has three main components which are dynamic power, short circuit

power and subthreshold leakage power hence total power dissipation is given by

$$P_t = P_{dyn} + P_{s.c} + P_{sub}$$

Where f is the frequency of operation

$$P_{s.c} = P_{dyn}\left[\left(\frac{9}{8}+\frac{V_{Dd}}{0.8V_{Dd}}\ln\left(\frac{10V_{Dd}}{eV_{Dd}}\right)\right)\times\frac{1}{\alpha-1}\frac{1}{2^{\alpha-1}}\frac{(1-2V_T)^{\alpha+1}}{(1-V_T)^{\alpha}}\right]$$

The analytical expression for subthreshold leakage power, which is due to the weak inversion conduction current flowing between the drain and the source when $|V_{GS}| < |V_{th}|$,is stated in [7]and[8] and is expressed as

$$P_{sub} = V_{DD}I_{sub}\left[\frac{\frac{C_L}{C_i}-1}{F-1}\right]$$

Where

$$I_{sub} = \mu C_{dp} V_T^2 \times e^{\frac{C_{ox}(V_{GS}-V_{th})}{C_{dp}V_T}} \times \left(1-e^{\frac{-V_{DS}}{V_T}}\right)$$

and C_{dp} denotes the capacitance of the depletion region, VT is the thermal voltage that is equal to kT/q, Cox is the oxide capacitance per unit area between the gate metal and the bulk surface, VGS is gate to source voltage when MOS transistor is off (0 volt) and $:$ is the electron mobility.

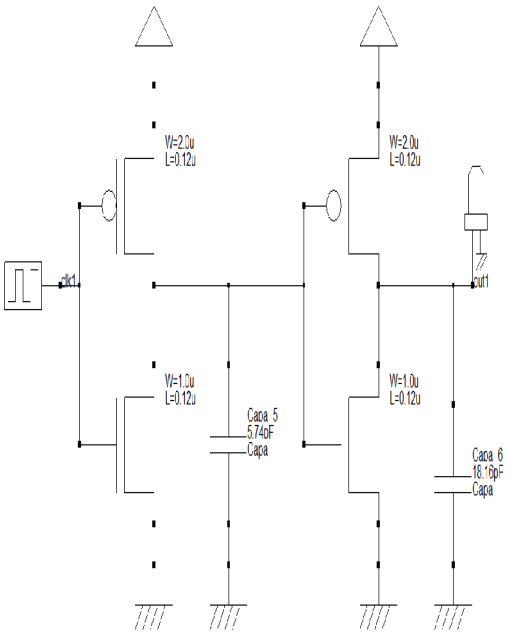

Figure 2: Two stage Taper Buffer

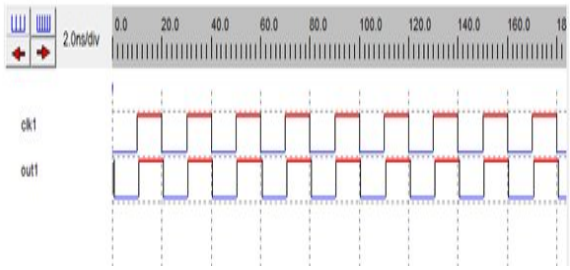

Figure 3 : Timing Diagram for Two Stage

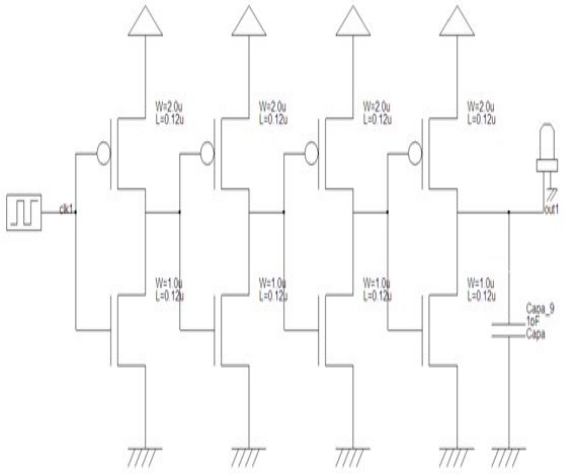

Figure 4.Four Stage Taper Buffer

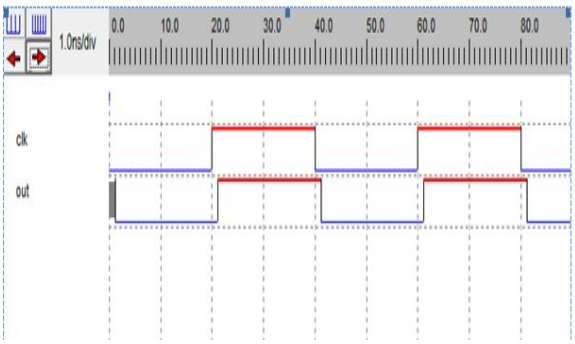

Figure 5.Timing Diagram for Four Stage

III.PROPOSED BUFFER DESIGN

It is well-known that the most of the power dissipation in CMOS structures is caused by charging/discharging the output load and by the short-circuit current that flows from the power supply to the ground, during switching of structures. The importance of short-circuit power dissipation in CMOS buffers, comes from the fact that a great fraction of the energy dissipated in VLSI circuits is due to on-chip and off-chip signal

driver circuits, which are based on inverting buffers [9]. In addition, the problem is exacerbated when the input signal operates at high frequencies since the number of times the power dissipates in a specific interval may also be proportionately high [10, 11]. So, it is desirable to reduce the short circuit power dissipation. Hence a modified buffer is proposed which dissipates less power because the short circuit component of power is eliminated in the design by tri-stating its output node momentarily before every output signal transition [12] .This is achieved by applying the gate driving signal of PMOS (NMOS) transistor to NMOS (PMOS) transistor of the output stage through a feedback network which delays the driving signal and avoids simultaneous turn on of NMOS and PMOS transistors during signal transition which is the very cause of short circuit current. Further, the capacitive load dependent tapering factor is applied to all the stages including the final stage. Figure 3 shows a 4 stage proposed taper buffer in which input signal is applied at IN which is amplified by 1st and 2nd stage. The feedback network is applied in 3rd and 4th stage, where T1, T4, T5, T7 are PMOS transistors and T2, T3, T6, T8 are NMOS transistors. INV1 and INV2 are minimum sized inverters which are connected to gate terminals of T8 and T7 for their input and with T2 and T5 as output respectively. The output of 2nd stage is connected toT1, T3, T4 and T6 only.

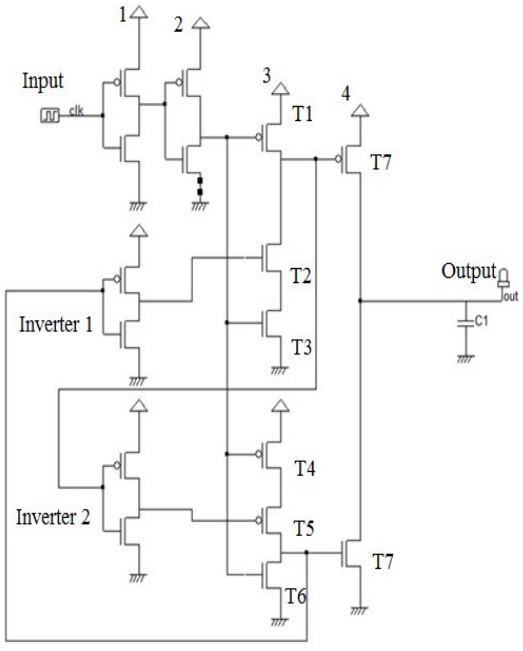

Figure 6: Four Stages Modified Taper Buffer

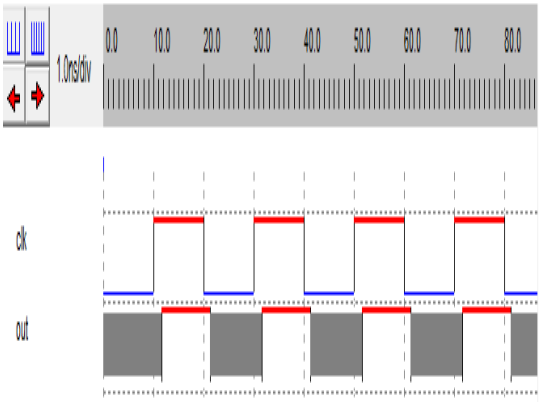

Figure 7: Timing Diagram for Modified Four Stages

IV. EXPERIMENT RESULTS

Many techniques have been employed to reduce power dissipation in VLSI circuits and lowering the supply voltage V_{DD} is the most effective to decrease the power dissipation, since CMOS power quadrically depends on V_{DD}. However low V_{DD} requires low threshold voltage V_{th}, but then the sub-threshold leakage power increases exponentially. Hence there is a great necessity to optimize V_{th} to achieve the required performance at minimum power dissipation [13,14]. In this context, V_{th} optimization has been investigated extensively with the objective to minimize the power consumption while satisfying a speed constraint. In our work, power and delay optimization is achieved by slightly increasing threshold voltage in the proposed design which not only reduces subthreshold leakage power but also optimize delay [15]. This is due to the fact that slight increase in threshold voltage causes a large amount of leakage power reduction with only small penalty in propagation delay. It is observed that increasing the threshold voltage between 0.2 V_{DD} and 0.4 V_{DD} gives the highest reduction in power with a minimal penalty in delay. Thereafter, the propagation delay increases quickly as V_{th} is increased beyond 0.4 V_{DD} and a high penalty in terms of speed has to be paid [16]. It is necessary to mention here that there is another incentive in not allowing the threshold voltage to increase beyond 0.4 V_{DD} which is that the threshold voltage value should be less than the switching threshold V_M= ($0.5V_{DD}$). If the threshold voltage is assigned a value that is higher than 0.4 V_{DD}, then due to any process variation the threshold voltage may reach V_M.

Table 1: Propagation delay for buffer stages $N=N_D$ (for minimum delay)

C_L(pF)	N_D	F_D	Propagation Delay(ns) for Tapper Buffer	Propagation Delay(ns) for Proposed Buffer
15	2	3.16	0.550	1.170
150	4	3.16	1.170	1.270
1500	5	3.98	1.480	1.650
15000	7	3.72	2.100	1.680
150000	9	3.59	2.720	1.750

V.CONCLUSIONS

Tapered buffer systems designed with this method are shown to have improved performance characteristics in the presence of local interconnect capacitance over those buffer systems in which the design method neglects local interconnect capacitance. The proposed buffer has been designed in 120nm technology node and simulated in Microwind 3.5. An improvement of 20% in power dissipation has been achieved while maintaining same delay as compared to the existing design. Hence, the proposed buffer can be used to provide power efficient solutions for portable VLSI applications at optimum propagation delay.. Thus, significant performance improvements can be attained by considering the effects of local interconnect capacitance during the design of tapered buffers.

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