Uninterruptible Power Supply: Interleaved Power Factor Improvement Techniques using Parallel Topology

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Abstract: Modern switching power supply design for power factor correction due to the introduction of many new controller chips have been developed in recent years. The various modes of operation, each with their own set of advantages and disadvantages with the power factor correction circuit is possible to make different designs. Stage power factor correction circuit, the need for more efficiency in all sectors have taken a close look, and with a small loss of development options. Significantly contribute to the damage of the department input rectifier bridge. Remove the diode bridge circuit or a dual-use it to carry, so alternative methods have been explored. In this paper, design considerations, and 300 watts of power factor correction design techniques are obtain by two 150−Watts PFC stages which are combined to form this 300−Watts PFC pre−regulator.

Keywords: Root Mean Square (RMS), Switch Mode Power Supplies (SMPS), Integrated Circuits (IC), Power Factor Correction (PFC), Electromagnetic Interference (EMI), Frequency Clamped Critical Conduction Mode (FCCCM), Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM), Reverse Recovery Time (TRR)

I. INTRODUCTION

Interleaving comprises parallel instead of one larger, it may be more difficult to design the two "small" stage. In fact, two 150-W PFC stage are combined to form 300-W PFC pre-regulator. This approach has several advantages, such as ease of implementation, the use of smaller components, or better heat distribution. In addition, the staggered extension critical conduction mode, which is an efficient and cost-effective technologies (without low TRR diode) power range. Also, if the operation of the two phases in the current ripple is significantly reduced. In particular, the input current looks like a CCM within a large-capacity capacitor RMS current is greatly reduced. When designing a CRM or interleaved PFC FCCCM, out-of- phase operation to maintain a major difficulty. This is because the switching frequency is not fixed nominal operation requires very moment the MOSFET is delayed until after the valley. Therefore, each stage must play in their own pace and at the same time synchronized to another branch, requiring a complex control circuitry. In a traditional master / slave mode, the main branch to operate freely, while other stages control, in accordance with 180 ° phase shift. The challenge is to promote a subordinate branch so that it never enters the CCM also showed unwanted dead times. [1]. NCP1631 by phase interaction options, including two branches operate independently in CRM, fundamentally prevent unwanted dead time or continuous conduction mode sequence risk. Nevertheless, the two phases exchange phase operation. It is worth noting, NCP1631 unique interleaving (which will be described in this paper) essentially maintain the desired 180 ° phase shift between branches in all conditions, including start-up, fault or transient sequence.

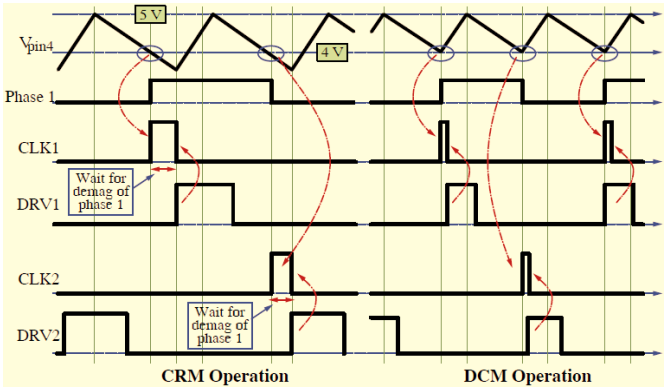

Figure 1: Clock Generation for Interleaved Technique

More generally, NCP1631 integrates a dual MOSFET driver, 2-phase interleaved PFC application. It drives the two branches of the so-called frequency clamp critical conduction mode (FCCCM), where each phase of work in CRM, in the most stressful conditions, in the DCM, otherwise, as a CRM controller with a frequency clamp (given by the oscillator). According to the conditions, PFC stage is actually converted from DCM CRM (or vice versa) without interruption operation, no degradation current shape. CRM traditional

control methods cannot provide this current shape integrity, even though some of them transition to DCM by using frequency clamping. NCP1631 FCCCM using their operating mode the oscillator means to manage by simple phase operation. Figure 1, the oscillator frequency is twice the voltage fluctuations outline each branch. When it reaches 4 - V lower threshold, the circuit generates a clock signal alternating phase 1 or phase 2.

II. GENERAL CASES OF INTERLEAVED PFC TECHNIQUE:

Case 1.

Inductor current cycle time is shorter than the two oscillation cycle. The clock signal generated when the corresponding branch of the inductor clock is demagnetized (the inductor current has reached zero), and can immediately start a new cycle. We have a fixed frequency DCM operation mode as described in each of the branches to the right in Figure 1. Naturally obtained Out-of-phase operation results, interleaved clock signal.

Case 2:

The inductor current is not zero when the clock signal corresponding to the inductance of the branch. If the MOSFET is turned on at that moment, the circuit will enter CCM. Instead, the phase is delayed until the next conduction core is reset and the inductor current reaches zero. This waiting period clock signal remains high, MOSFET conduction current in the coil as soon as possible has reached zero. In other words, the CCM operation. The oscillator continues to wait during the discharge, reducing the oscillator frequency and delay the next clock signal occurs. It analyzes show that proper selection of the charging and discharging current of the oscillator causes stability - of-phase operation as depicted in Figure 1 on the left. Voltage mode controller NCP1631 power MOSFET's on-time is the same for both branches. Demagnetization time only depends on the conduction time and the output voltage line, and the two branches of the same

$$\left(t_{demag} = t_{on} \cdot \frac{V_{in}}{V_{out} - V_{in}} \right).$$

So, if we ignore, adjusting on-time control signal in each circuit, the timing circuit in response to the tolerances in their respective branches of the two inductors, if not with the same inductance the current cycle duration is the same. Finally, the only source current imbalance inductance tolerance. One can easily show that the shared data by the following equation:

$$\frac{I_{in(branch1)}}{I_{in(branch2)}} = \frac{L_{branch2}}{L_{branch1}}$$

Where:

Lbranch1 and Lbranch2 are the inductance values of phase 1 and phase 2 respectively. Iin (branch1) and Iin (branch2) are the averaged input currents drawn by phase 1 and phase 2 respectively.

In fact, if the dispersion inductance in the range of ± 5%, is possible that the current imbalance less than ± 10%. Located in SOIC16 package, NCP1631 also provides many other useful features. In particular , the frequency of the clamp circuit is adapted in line / load range, optimizing the efficiency of the PFC stage : a programmable load below the level , the frequency is a linear function of the power attenuation in order to maintain a high level of efficiency , even in the very light load (frequency fold back) . NCP1631 PFC stage is also a drive to reduce the downstream converter is designed to provide a narrow range of DC voltage. With this goal, the circuit has a "PFC OK" output pin disables downstream converters, until large-capacity capacitor charge, and no failure is detected. In addition , NCP1631 in the mutant load or line transients (low bandwidth PFC loop usually causes large overshoot and undershoot problems) , greatly reducing the output voltage deviation :

• Dedicate a specific pin optimal planning overvoltage protection level

• Dramatically speeding regulation loop , when the output voltage falls below its required level (dynamic response enhancer) was 4.5% .In fact, the down converter can be optimized design due to PFC stage as it provides a very narrow voltage range.

Finally, NCP1631 protection (maximum current limit, inrush current detection, under voltage protection, brownout detect) protection system, most likely from excessive stress, the PFC stage is extremely rugged and reliable.

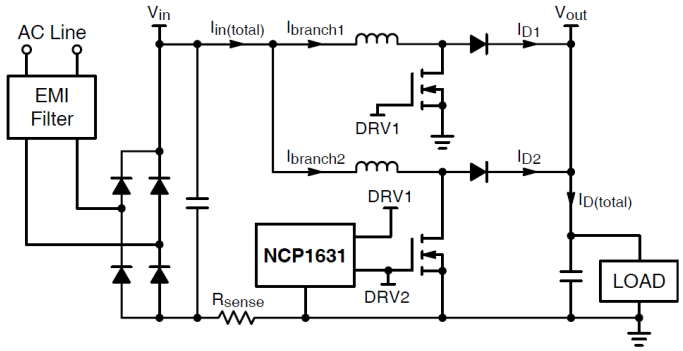

Figure 2: Interleaved PFC Stage Simplified Application Schematic

III. GENERAL BENEFITS OF INTERLEAVED PFC:

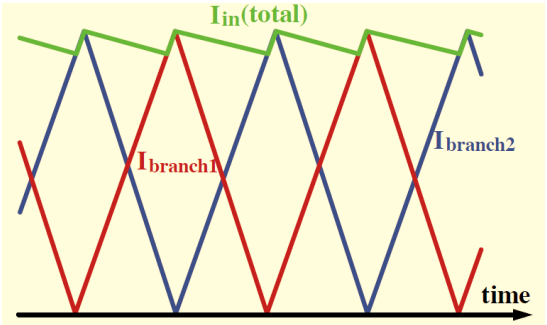

Figure 3: Reduced Ripple in the Total Current

Figure 2 shows a simplified schematic of the two parallel channels. The first branch sink current Ibranch1 and offer ID1 output. Other branches draw Ibranch2 produce ID2. These currents are the classic single stage FCCCM, PFC stage exhibit similar. However, we will see, when the out-of-phase operation results, interleaved PFC and the total current (Iin (total) of Figure 2) to provide the boost diode (ID (total) total current absorbed Figure 2) there was a significant reduction in ripple obtained with the traditional single stage PFC stage. Inductor current in each branch showed great ripple (CCM work), but shown in Figure 3 [2], out of phase operation results in a very small stage by the PFC total current ripple. In fact, there is no ripple at all, the input voltage of the output voltage of the half (up and down the road is the same), and enter the maximum value (100% of the average current - peak to peak), when Vin is close to zero, or close to the output voltage (see Figure 4). More specifically, assuming a permanent CCM operation (no frequency clamp - (1)) 180 - phase shift, the input current ripple can be calculated as follows:

$$\frac{\Delta I_{in(pk-pk)}}{I_{in}} = \frac{\left(2 \cdot \frac{V_{in}}{V_{out}}\right) - 1}{\frac{V_{in}}{V_{out}}} \quad if \quad \frac{V_{in}}{V_{out}} > 0.5$$

$$\frac{\Delta I_{in(pk-pk)}}{I_{in}} = \frac{1 - \left(2 \cdot \frac{V_{in}}{V_{out}}\right)}{1 - \frac{V_{in}}{V_{out}}} \quad if \quad \frac{V_{in}}{V_{out}} < 0.5$$

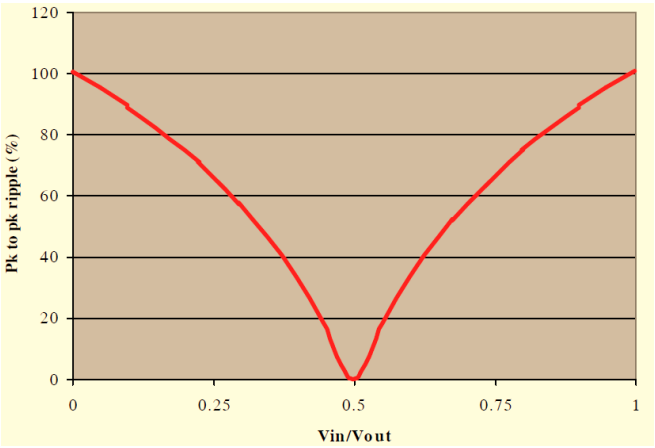

Figure 4: Peak - peak input ripple current amplitude as a function line Magnitude

In fact, the input current look similar in this sense, the current ripple to a CCM PFC. The feed volume and pulsation of the load current Minimize. As shown in Figure 5, still assuming CCM operation, 180° phase shift time to exchange the contents of delivery of two branches of large-capacity capacitor and the load (Figure 2 of the ID (total)) of the total current. This is because the performance of the two-stage fuel interleaved sequence. Also, if the input voltage is lower than half of the output voltage, there are two branches between refueling intervals do not overlap. This characteristic led to significant reduction in the bulk capacitor RMS current over a wide power applications at low line conditions, easier, cheaper and more reliable design.

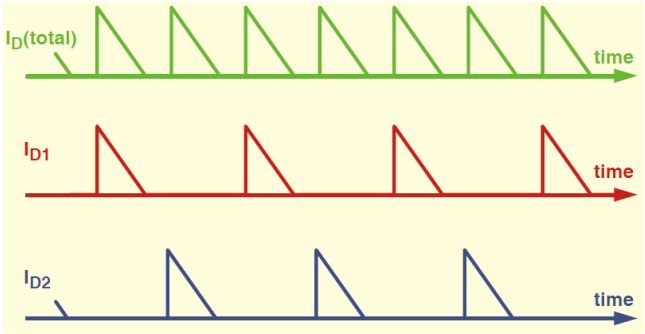

Figure 5: The result of interleaving to reduce the AC current Refuelling exchange of content

In the case of a wide supply (not overlap between the two phases the number of refueling), the maximum RMS current global fuel, can be expressed as follows:

$$I_{D(rms)} = \sqrt{\frac{16 \cdot \sqrt{2} \cdot P_{out}^2}{9 \cdot \pi \cdot V_{acLL} \cdot V_{out} \cdot \eta^2}}$$

RMS current, thus reducing the 30% (√2 points) compared to traditional CCM or FCCCM operation to get anything. Similarly, the flow of large-capacity capacitor RMS current is reduced. Assuming a constant load current, this current is a good approximation, using the following formula it is obtain:

$$I_{Cout(rms)} = \sqrt{\frac{16 \cdot \sqrt{2} \cdot P_{out}^2}{9 \cdot \pi \cdot V_{acLL} \cdot V_{out} \cdot \eta^2} - \left(\frac{P_{out}}{V_{out}}\right)^2}$$

However, in a traditional CCM or FCCCM PFC, it was observed:

$$I_{Cout(rms)} = \sqrt{\frac{32 \cdot \sqrt{2} \cdot P_{out}^2}{9 \cdot \pi \cdot V_{acLL} \cdot V_{out} \cdot \eta^2} - \left(\frac{P_{out}}{V_{out}}\right)^2}$$

For the second half-line cycle (when "PH2" is high), the "PH2 PFC stage" branch is operating and "PH1 PFC stage" is having no input voltage is inactive.

IV. RESULTS AND PERFORMANCE CURVES FOR 300 WATTS:

Detailed performance proposed 300-W interleaved PFC stage. However, this is the paper's main findings. Figure 6 shows the input current at low and high line. As expected, the input current looks like a CCM. The high line, a slight increase in the frequency of the input current ripple clamp. Bottom waveform is magnified views. Shows a drive signal determine whether the right to get, 180 ° phase shift. At low line (left), the branches in the CCM operation. High line, they work in DCM (R) near the valley proved oscillating

current at rated load (at light loads determined frequency fold back function at a lower level in order to improve efficiency, is set to 130 kHz frequency clamp). It is worth recalling, NCP1631 like other FCCCM circuit automatically adjusts the MOSFET conduction time, still showing near unity power factor DCM. Long PF and THD performance [4].

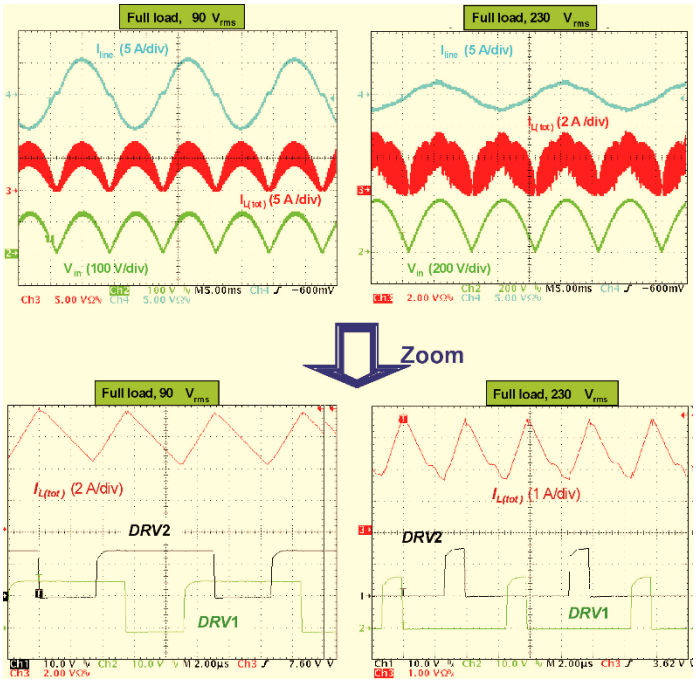

Figure 6: Waveforms at full load

As shown in Figure 7, particularly over the load efficiency characteristic is flat. This is because the interleaved PFC restricted by sharing stress between the two branches conduction losses full weight of the load. At light loads, frequency clamp and frequency fold back function, reduce switching losses, therefore, effectively limiting the attenuation at light load efficiency is usually observed.

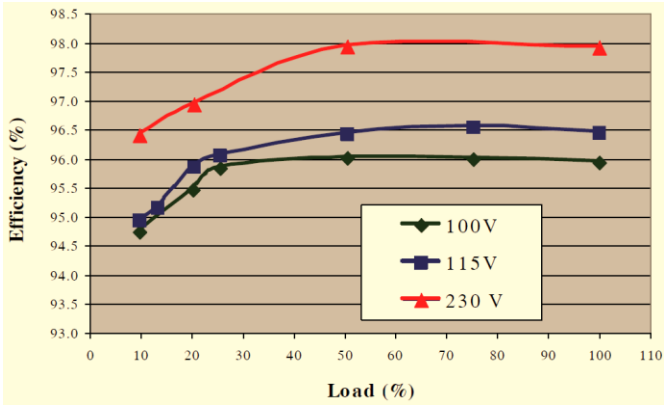

Figure 7: Efficiency vs. Load

These efficiency performance were obtained using a typical frequency fold back characteristics. Excellent light-load efficiency than is required, frequency fold back can be adjusted. For example this results can obtain how to add a simple resistor, when the power suddenly goes down below a set level, the switching frequency. Figure 7 shows that such a technique can further improve the efficiency of between 10% and 20% of the load, forcing the power level the operation of 20 kHz. PFC stage to keep running in CRM required for the operation of an efficient load between 50% and 100%.

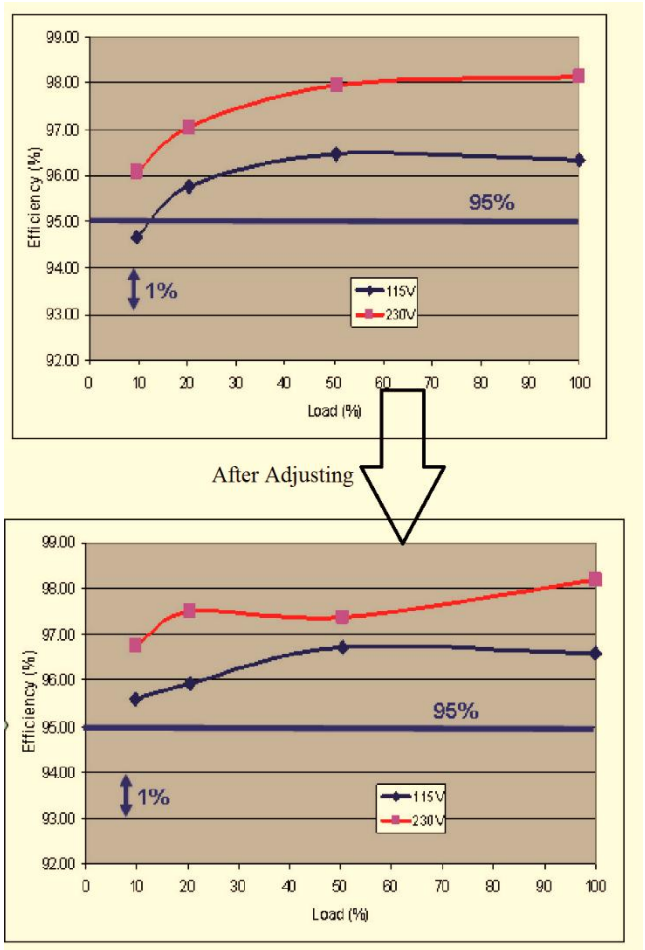

Figure 8: Adjust the frequency fold back feature can help improve light load efficiency

V. CONCLUSION AND FUTURE SCOPE:

Interleaved power factor correction with a 300 W load technique has several advantages, which has a simple control or in case high-frequency noise is injected into the list of beneficial EMI line, especially in the strict form factors have been met. In this paper, interleaving the basics and loosely cover an abstract design. Prototyping, at full load of 300 W has been tested that such techniques can further improve efficiency of 10% and 20% of the load, forcing the power level the operation of 20 kHz. THD is very low. PFC technology is a very effective solution of choice for high-performance applications. However, this option should be devoted to higher power applications (one kilowatt or more).

It should be noted that traditional topology, a 300 - W high scale, they have some design challenges in the size and power consumption of the components. Therefore, this topology is such a staggered, may spread heat and provide many other benefits that can correctly implemented.

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VI. BIOGRAPHIES

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