Design of Processor Interface Module for P1750A Processor Using VHDL

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***Abstract* - The paper describes Design of processor interface module for P1750A used in satellite subsystems. The embedded software was designed to receive input from various sensors and down linked to the Command and Data Acquisition (CDA) Station and sent to the Satellite Operations Control Center (SOCC) and initiate corrective action form earth control station when required. This methodology was not compromised with respect to the application and execution time. The advent of Field Programmable Gate Arrays (FPGAs) has made compact realization of embedded system possible. As FPGAs are high density logic devices. It is possible to realize certain software functions in hardware in an efficient way. In this paper it is an approach of designing processor interface module for processor P1750A in hardware.**

Entire Design is carried out using Very High Speed Integrated circuit (VHSIC) Hardware Description Language.

***Keywords* – MA31750 processor, P1750A, Decoding, Error detection and correction (EDAC), Bus Management Unit.**

I. Introduction

The satellite control system in general is designed to monitor the various health parameters of the satellite and initiate corrective actions whenever required [1]. The control system receives data from various monitoring sensors and beams them down to the earth control station for processing. Many standalone electrical systems can be integrated into a single system with advances in spacecraft technologies resulting in miniaturization in spacecraft electronics. Hence the design of spacecraft electronics is governed by overriding concern to reduce power, weight and volume. With high speed processors, Application Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs), several subsystems are integrated into a single Bus Management Unit (BMU). Several stand-alone systems like Master Data Acquisition system, On-board storage and playback logic, Timer control, Sensor electronics, Temperature controller, 1553 bus protocol, Attitude and Orbit Control Electronics (AOCE) and Telemetry (TM) are integrated into a single BMU.

Bus management system is a centralized information processing system. Thus, the design of the BMU is governed by compact realization at package level, minimal interfaces at spacecraft level and operational consideration at mission level [1].

BMU does command, monitoring, data acquisition functions in addition to Attitude and Orbit Control functions.

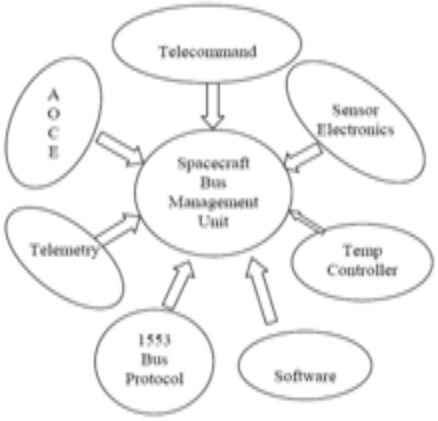


Fig 1: Integration of stand alone sub system into spacecraft MMU

The note is organized as follows: Section II describes Bus Management System; Section III describes processor interface module for MA31750; Section IV describes processor interface module for P1750A; Section V gives the implementation of clk generation and IO block using VHDL with Modelsim simulation results.

II. Bus Management Unit

1. Motherboard Configuration

BMU is realized as a Mother-board Daughter board package. A standard bus is present on the Mother-board of BMU to simplify the design of daughter boards and to have flexibility of slot independency. A few new technologies introduced are Bus Management Unit for carrying out functions such as Command, Telemetry, Attitude and Orbit Control, Sensor Processing [1]. A common bus is used for all the Daughter cards, which is routed through the motherboard. This is done to simplify the design of the daughter cards.

2. Daughter card configuration

Signals from other systems of the spacecraft are routed to the appropriate Daughter card directly. The Daughter card is housed in a tray. The design of the tray is such that the PCB is not exposed to the external world to minimize effects of EMI/radiation. It also allows double side mounting of components. The design of the tray is standardized to simplify the fabrication process. Figure 2 shows the Motherboard-Daughter-board configuration. On the spacecraft deck, one side of the tray is flush mounted, as it leads to better thermal conduction.

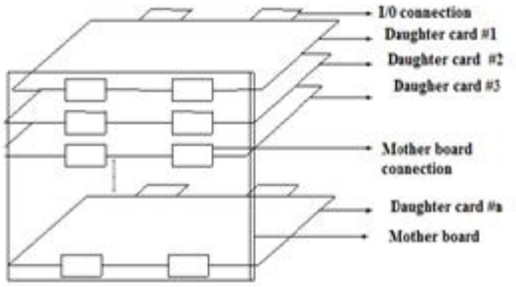


Fig 2: Mother board daughter board configuration

III Processor interface module for MA31750

The GEC Plessey MA31750 is a single chip microprocessor that implements the full MIL-STD-1750A Instruction set architecture and option 2 of Draft MIL-STD-1750B. The MA-31750 offers a considerable performance by using a 32-bit internal bus structure with a 24*24 bit multiplier and 32-bit ALU. The processor can directly access 64Kwords of memory in full accordance with MIL-STD-1750A mode. This increases to 1 MW when used with the optional MA31751 Memory Management Unit (MMU) and the 1750B mode allows the system memory to be expandable to 8MW.The MA31750 uses system Configuration Register that allows the processor to function with a variety of different system designs. Implemented features such as MMU should be indicated as present by setting bits in an externally implemented 16-bit latch as explained ahead. The Latch must be placed in I/O space at the address defined by XIO RCW. The processor decodes this command internally and generates a discrete output signal CONFWN, which may be used as external register output Enable control.

The MA31750 Supports a 64 kW addressing space dedicated to I/O control &communication in accordance with MIL-STD-1750.The control line MION asserted low when accessing I/O space. One of the two commands XIO or VIO is used to specify both data for the transfer and port address. The CPU contains logic, which decodes all internally supported XIO commands and generates the control signals necessary to carry out the command action. The processor also uses a 16-bit STATUSWORD (SW) for implementing expanded memory with external MMU & to hold the condition of various flags set by the result of previous arithmetic/logic operations.

This Processor Interface contains.
(a) Configuration Register Unit (config_word)
(b)I/F without MMU (latch_not_mmu)
(c) I/F with MMU (latch_mmu)
(d) I/O Data Latch (io_port)
(e) EDAC & FLAG LOGIC (edac_inf)
(f) Wait State logic (wait_st_logic)
(g) Clock Generation (clk_gen)
(h) ADD Bus Selection & Decoding Logic for Memory (mem_decoder)
(i) Decoding Logic for I/O (io_dec)
(j) DPRAM (dp_RAM)
(k) Data Bus routing (data_bus_routing)
(l) Interface to Mil Std 1553 protocol chip (inf_1553)
(m) Miscellaneous Signals

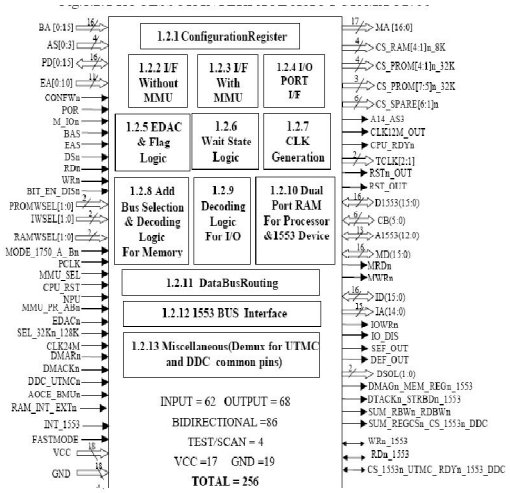


Fig 3 Processor interface module for MA31750

IV. Processor Interface Module for P1750A

The PACE1750A is a general purpose, single chip, 16-bit CMOS microprocessor designed for high performance floating point and integer arithmetic, with extensive real time environment support. It offers a variety of data types, including bits, bytes, 16-bit and 32-bit integers, and 32-bit and 48-bit floating point numbers. It provides 13 addressing modes, including direct, indirect, indexed, based, based indexed and immediate long and short, and it can access 2MWords of segmented memory space (64KWords segments).

The PACE1750A offers a well-rounded instruction set with 130 instruction types, including a comprehensive integer, floating point, integer-to-floating point and floating point-to-integer set, a variety of stack manipulation instructions, high level language support instructions such as Compare Between Bounds and Loop Control Instructions. It also offers some unique instructions such as vectored l/O, supports executive and user modes, and provides an escape mechanism which allows user-defined instructions using a coprocessor. The chip includes 16 general purpose registers, 8 other user-accessible registers, and an array of real time application support resources, such as 2 programmable timers, a complete interrupt controller supporting 16levels of prioritized internal and external interrupts, and a faults and exceptions handler controlling internally and externally generated faults.

The microprocessor achieves very high throughput of 2.6MIPS for a standard real time integer/floating point instruction mix at a 40 MHz clock. It executes integer Add in 0.1 us, integer Multiply in 0.575 us, Floating Point Add in 0.7 us, and Floating Point Multiply in 1.075 us, for register operands at a 40 MHz clock speed. The PACE1750A uses a single multiplexed 16-bit parallel bus. Status signals are provided to determine whether the processor is in the memory or I/O bus cycle, reading and writing, and whether the bus cycle is for data or instructions. The basic bus cycle is 4 clocks long. The PACE1750A will extend the cycle by insertion of wait states in the address and data phases (in response to RDYA and RDYD signals, respectively) and will hold the machine in HI-Z if this CPU has not acquired the bus. A typical non-bus cycle is three clocks long. However, variable length cycles are used for such repetitive operations as multiply, divide, scale and normalize, reducing significantly the number of CPU CLOCKS per operation step and resulting in very fast integer and floating point execution times.

This Processor Interface module contains.

- Configuration Register Unit (config_word)
- Address and data Demux
- I/F with MMU (latch_mmu)
- I/O Data Latch (io_port)
- EDAC & FLAG LOGIC (edac_inf)
- Wait State logic (wait_st_logic)
- Clock Generation (clk_gen)
- ADD Bus Selection & Decoding Logic for Memory (mem_decoder)
- Decoding Logic for I/O (io_dec)
- Data Bus Routing (data_bus_routing)
- Interface to Mil Std 1553 protocol chip (inf_1553)
- Miscellaneous Signals

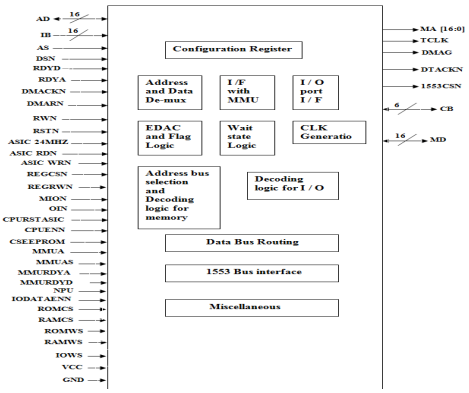


Fig 4 Processor interface module for P1750A

V Functional modules in P1750A processor

Address and Data De-multiplexer

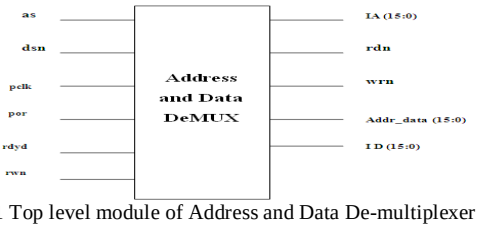
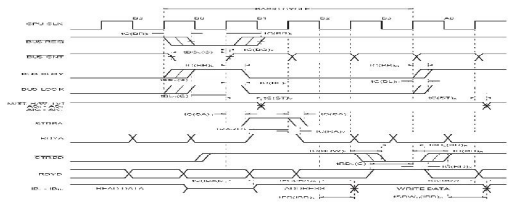


Fig 5.1 Top level module of Address and Data De-multiplexer

Address and Data De-multiplexer is single multiplexed 16-bit parallel bus. It performs write and read operation on a single bidirectional bus. By using this single multiplexed bus we can reduce the input output peripherals and which optimizes the size of the processor. Fig 5.1 shows top level module of address and data de-multiplexer.

At the positive edge of the processor clock an address can be write into IA only when address strobe must be high and data strobe must be low and ready signal should be activated. When to read a data from processor address strobe will be low and data strobe will be high and also ready signal must be activated then data can be read in ID. Fig 5.2 shows timing diagram of address and data de-multiplexer for minimum write and minimum read operation.

Minimum Write Bus Cycle Timing Diagram



Minimum Read Bus Cycle Timing Diagram

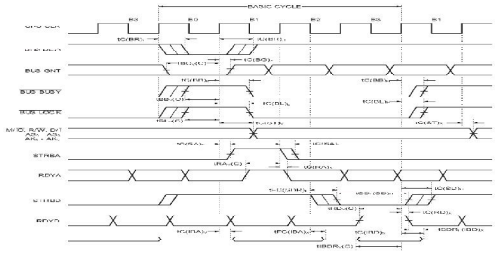


Fig 5.2 Timing diagram for read and write operation

Input Output Block

Input output block works like a simple flip flop. At the positive edge of the clock input data sent to the output only when enable pin is activated. Fig 5.3 shows top level diagram of input output block. Fig 5.4 shows internal structure of input output block.

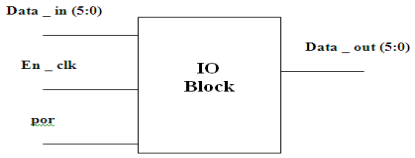


Fig 5.3 Top level module of Input Output block

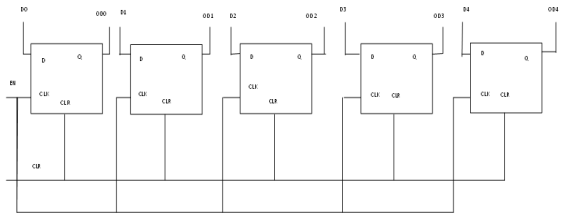


Fig 5.4 Internal structure of input output block

Wait State logic

This block generates the Wait state signal, CPU_RDYn, START_CYCLE, MWRn, MRDn, IOWRn and DPRAMWRn. This logic helps Processor to Interface Slower Memory and I/O Devices. Four Selectable Wait State Provisions has been provided for memory and I/O. Due to EDAC, automatically extra one wait-state is exerted for RAM write/read operation.

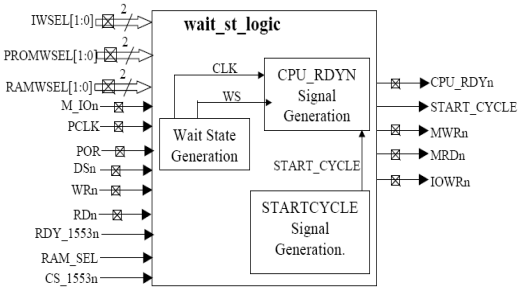


Fig 5.5 Functional schematic of wait state logic

Fig 5.5 shows functional schematic of wait state logic. Fig 4.6 shows internal structure of wait state logic.

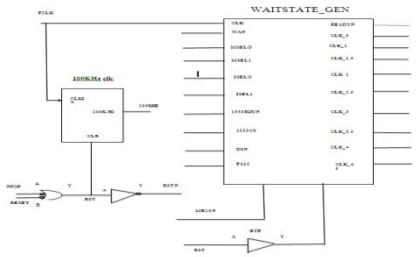


Fig 5.6 Internal structure of wait state logic

Clock Generation

This block generates 12MHz clock. 24MHz clock is converted to 12MHz clock at the positive edge of the clock. Fig 5.7 shows top level module of clock generation. Fig 5.8 shows internal structure of clock generation. Some of the intermediate blocks may not support for 24MHz clock so conversion needed to 12MHz.

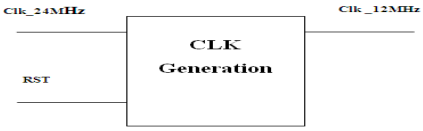


Fig 5.7 Top level module of clock generation

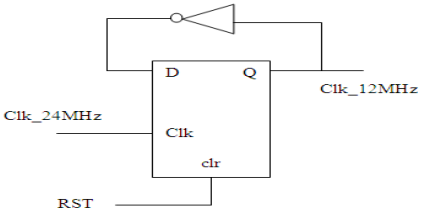


Fig 5.8 Internal structure of clock generation

PROM Decoder

This block generates chip select signals. Chip select CS0, CS1, CS2 and CS3 are generated. At the particular address these chip select signals will be selected. CS0 will be selected at 64000-67FFF and 0X000-X3FFF. CS1 will be selected at 04000-07FFF and 14000-17FFF. CS2 will be selected at 24000-27FFF and 34000-37FFF. CS3 will be selected at 44000-47FFF and 54000-57FFF.

Fig 5.9 shows top level module of PROM decoder. Fig 5.10 shows internal structure of PROM decoder.

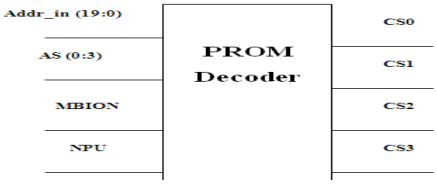


Fig 5.9 Top level module of PROM decoder

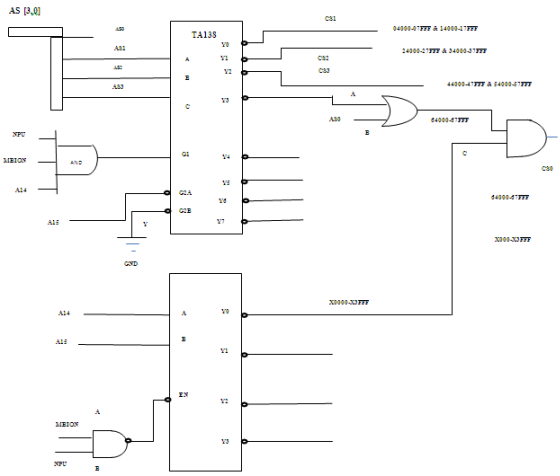


Fig 5.10 Internal structure of PROM decoder

RAM Decoder

This block generates chip select signals. The signal CS_1553n is generated to access the 1553 Bus. Chip select CS0, CS1, CS2, CS3 and CS1553 are generated. At the particular address these chip select signals will be selected. CS0 will be selected at XA000-XBFFF. CS1 will be selected at XC000-XDFFF. CS2 will be selected at XE000-XFFFF. CS1553 will be selected at 08000-08FFF only when EXT_RAM_EN is high. CS3 will be selected only when EXT_RAM_EN is low.

Fig 5.11 shows top level module of RAM decoder. Fig5.12 shows internal structure of RAM decoder.

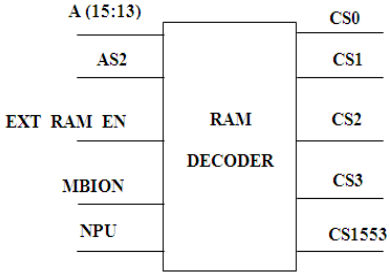


Fig 5.11 Top level module of RAM decoder

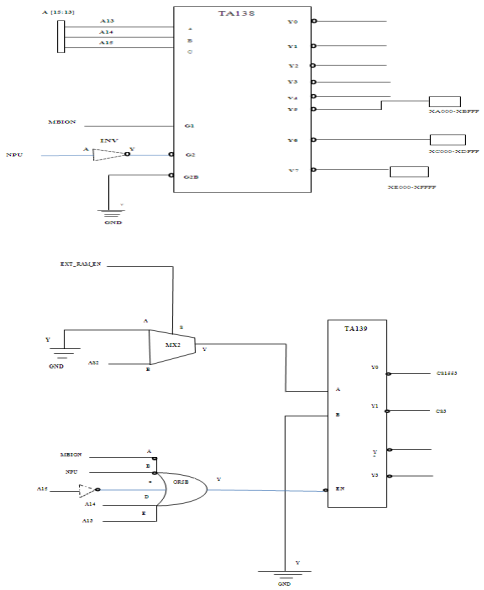


Fig 5.12 Internal structure of RAM decoder

Input Output decoder

Input output decoder decodes the address for BMU and AOCE. If select line is zero then decoder selects BMU only at the address 002Dh and if select line is one decoder selects AOCE only at the address 0100h.

Fig 5.13 shows top level module of Input Output decoder. Fig 5.14 shows internal structure of Input Output decoder.

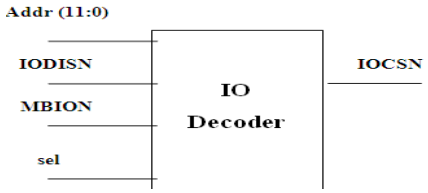


Fig 5.13 Top level module of Input Output decoder

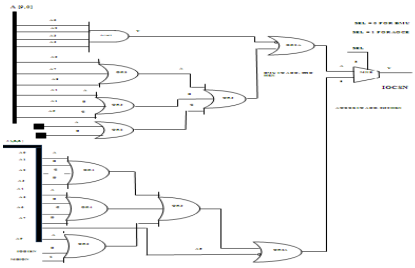


Fig 5.14 Internal structure of Input Output decoder

Interface with MMU

This block generates 20-Bit Address bus, which is used when Memory Expansion through MMU is enabled. Here, Extended Address lines MMUA [7:0] from the MMU are used in addition to ADDR [11:0] to derive the 20-Bit Address Bus, MMUA_ADDR [19:0].

Fig 4.15 shows top level module of Input Output decoder. Fig4.16 shows internal structure of Input Output decoder.

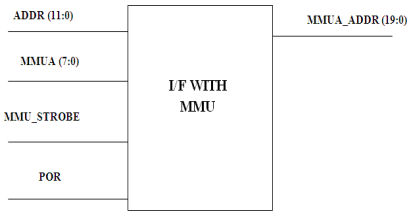


Fig 5.15 Top level module of Interface with MMU

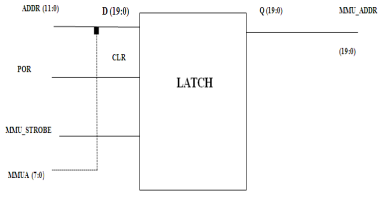
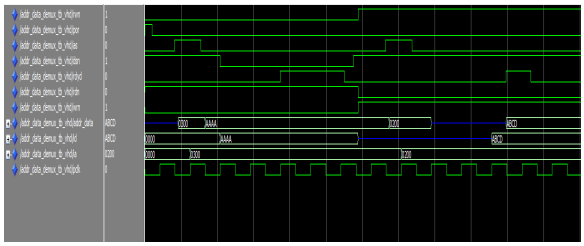


Fig 5.16 Internal structure of Interface with MMU

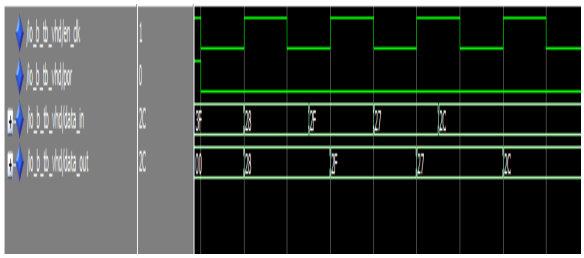
VI Simulation Results

Address and Data De-multiplexer



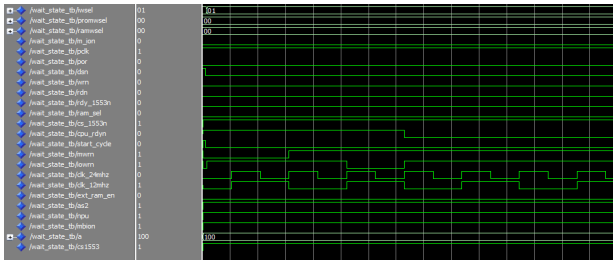
At the positive edge of the processor clock an address can be writing into IA only when address strobe must be high and data strobe must be low and ready signal should be activated. When to read a data from processor address strobe will become low and data strobe will be high and also ready signal must be activated then data can be read in ID.

Input Output Block



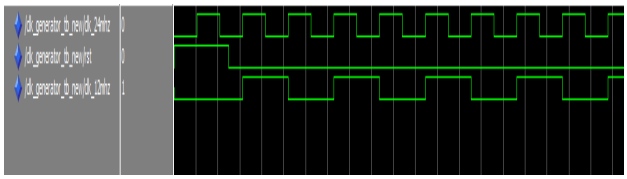
At the positive edge of the clock input data sent to the output only when enable pin is activated as high.

Wait State Logic

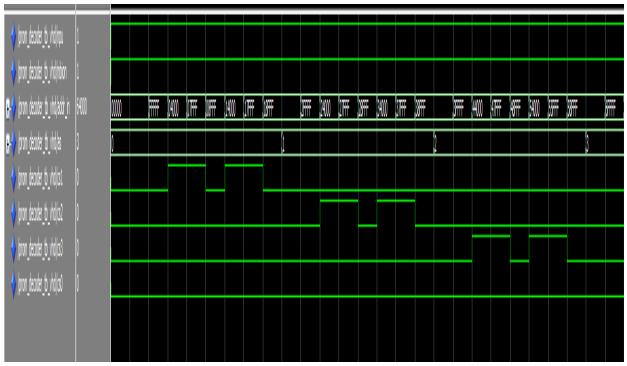


Here with respect to the IO, PROM, RAM selection bits the chip select CS1553 will be selected only when processor clock will be high and ready, por, wrn should be low.

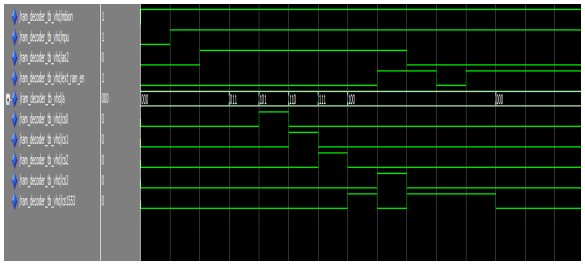
Clock Generation



PROM Decoder



RAM Decoder

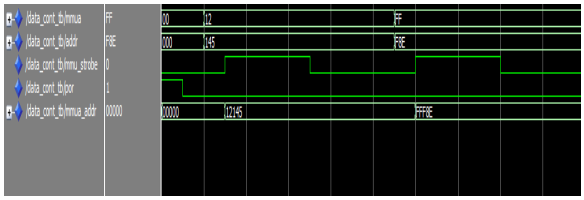


Chip select CS0, CS1, CS2, CS3 and CS1553 are generated at the particular address. CS0 will be selected at XA000-XBFFF. CS1 will be selected at XC000-XDFFF. CS2 will be selected at XE000-XFFFF. CS1553 will be selected at 08000-08FFF only when EXT_RAM_EN is high. CS3 will be selected only when EXT_RAM_EN is low. For all chip select MBION and NPU should be high.

Input Output Decoder

When select line is zero then decoder selects BMU only at the address 002Dh and if select line is one decoder selects AOCE only at the address 0100h. These BMU and AOCE output can be seen in IOCSN.

Interface with MMU



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