

An improved energy stored q-ZSI connected with a Constant DC Link peak voltage Photovoltaic power system

B. Kavya Santhoshi¹, Dr. M. Sasi Kumar²

P.G Scholar¹, Professor², Jeppiaar Engineering College, Chennai, Tamilnadu, India.

E-Mail:- kavyabe2010@gmail.com, pmsasi77@yahoo.co.in

ABSTRACT

Power generation using Photovoltaic cells is a promising form of sustainable energy. A quasi-Z source inverter (qZSI) can minimize the fluctuations from the power generated by a PV panel. In the existing system, during the discharge of battery, discontinuous mode of conduction has a wider range of operation. Hence there is a limitation on power. Constant DC-link peak voltage is achieved thereby improving the power and reducing the distortion in load. The new topology enables an improved ability to compensate power while maintaining a constant dc-link peak voltage with minimum harmonics. Thus the proposed system provides an efficient means of PV power generation.

Keywords – Energy storage, photovoltaic (PV), power generation, quasi-Z source inverter (qZSI), renewable energy.

I. INTRODUCTION

Power generation using photovoltaic cells has gained its importance over the years due to sustainability. Two-stage and single-stage inverters are used in this area [2], [3], [4], [5] and [6]. The size of a traditional single stage topology must be more to handle the wide variation in PV voltage. Two-stage structure has the drawback of increased cost and reduced efficiency. Hence, as an alternate to these topologies, Z-source inverter (ZSI) is used. It has a single-stage structure that can achieve a two-stage inverter's role [11]. The wide range of variation in PV voltage can be handled by the ZSI thus leading to reduced capacity of inverter and lesser components thereby reducing the system cost. Quasi-Z source inverters are highly suitable to be applied in PV systems [9]. They have the following benefits 1) lower capacitor rating 2) Reduced ripples while switching 3) Constant current can be drawn from the PV panel (There is no need for extra capacitors).

In general, solar power has problems like fluctuations and intermittency. A real solution to this problem is Energy storage (ES) [12] to [15]. Any alternating form of load or grid can be supplied continuously with stable and smooth power from an Energy stored PV system. Usually, bidirectional dc-dc converters are used in order to manage the batteries. Thus, the system becomes less economical and complex with lower efficiency.

II. EXISTING SYSTEM WITH Q-ZSI

The block diagram for the system with q-ZSI is shown in figure 1.

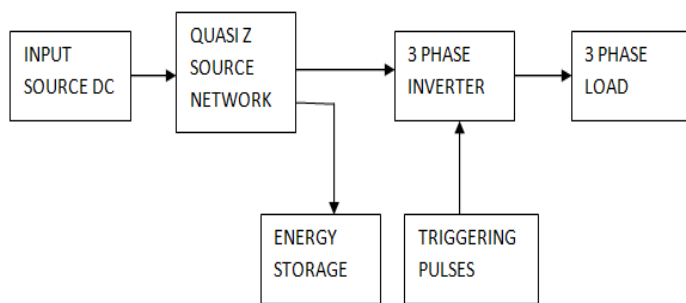


Fig. 1. Block diagram of the system

A qZSI with energy storage was proposed for power generation using PV [7] and [8]. The circuit as shown in fig. 2, has a battery connected to a capacitor C_2 in parallel in order to balance the power consumption and production. This method has some demerits. Battery discharging ability is limited due to discontinuous conduction mode (DCM). DCM was avoided using an active switch [7] but by using an active switch the cost and power loss have to be compromised with.

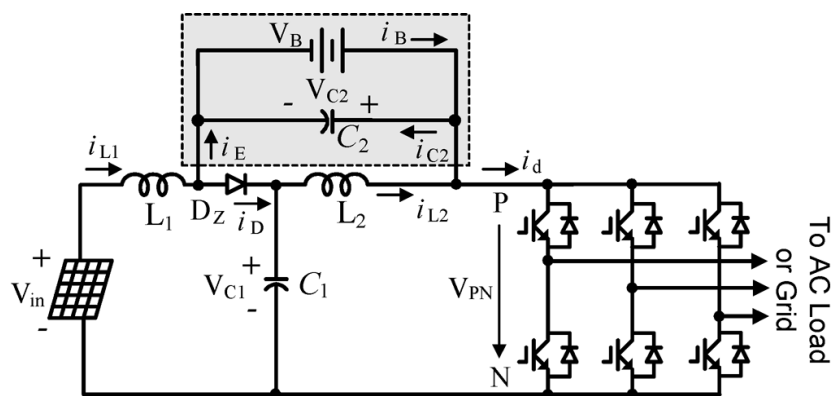


Fig. 2. Existing qZSI with battery for PV power generation

III. IMPROVED QZSI AND ITS MERITS OVER THE PREVIOUS TOPOLOGY

A new topology that overcomes these drawbacks has been proposed . In Fig 3, there are three power sources. They are 1. PV panels 2. Battery and 3. Grid/Load. By controlling the flow of power in two sources, there will be a match in the power of third source by the equation :

$$P_{in} - P_{out} + P_{bat} = 0 \tag{1}$$

Where P_{in} denotes the Input power from PV

P_{out} denotes the Output from inverter and

P_{bat} denotes the power from battery

P_{in} is unidirectional P_{bat} is bidirectional (positive during discharging interval and negative while the power is delivered to the grid by inverter).

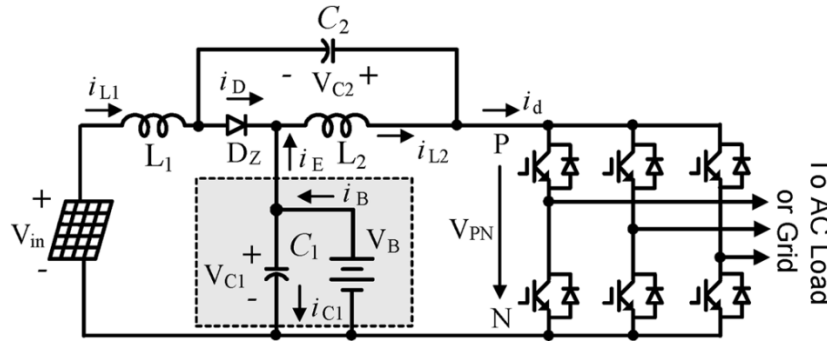


Fig. 3. An improved energy stored qZSI for PV power generation.

A. OPERATING PRINCIPLE

Like the qZSI in the existing system, it has two states, namely, Shoot-through and Non-shoot through states. Shoot-through state is produced by any one phase leg, combinations of any two phase legs and all three legs. During this state the diode Dz is turned OFF as there is reverse-bias voltage across it. The equivalent circuit of this mode is shown in fig 4.a). The circuit equations for this mode are

$$CdV_{C1}/dt = i_B - i_{L2} \quad (2)$$

$$CdV_{C2}/dt = -i_{L1} \quad (3)$$

$$L di_{L1}/dt = V_{in} + V_{C2} \quad (4)$$

$$L di_{L2}/dt = V_{C1} \quad (5)$$

Where i_{L1} and i_{L2} are the currents of inductors $L1$ and $L2$ respectively;

V_{C1} , V_{C2} and V_{in} are the voltages of capacitors C_1 , C_2 and PV panel respectively;

C is the capacitance of capacitors C_1 and C_2 ;

L is the inductance of inductors L_1 and L_2 .

Non-shoot through state corresponds to one of the six active states and two traditional zero states. The equivalent circuit of this mode, when continuous current flows through the diode Dz is shown in fig 4.b). The circuit equations are

$$CdV_{C1}/dt = i_B + i_{L1} - i_d \quad (6)$$

$$CdV_{C2}/dt = i_{L2} - i_d \quad (7)$$

$$L di_{L1}/dt = V_{in} - V_{C1} \quad (8)$$

$$L di_{L2}/dt = -V_{C2} \quad (9)$$

B. MODES OF OPERATION

During mode 1, switches S1 and S6 conduct. At that time, Phase voltages are

$$V_{an} = V_{dc}/2$$

$$V_{bn} = -V_{dc}/2$$

$$V_{cn} = 0$$

Line voltage is $V_{ab} = V_{an} - V_{bn}$

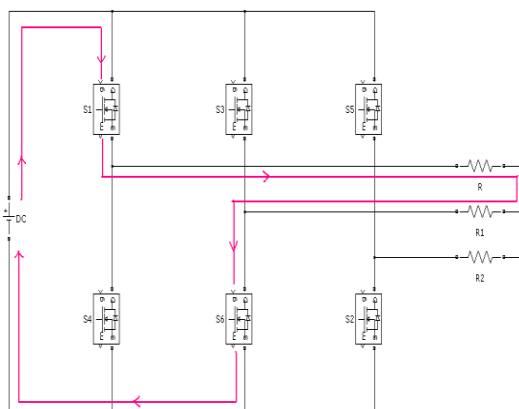


Fig. 4. (i) Mode I

During mode 2, switches S1 and S2 conduct. At that time, phase voltages are

$$V_{an} = V_{dc}/2$$

$$V_{bn} = 0$$

$$V_{cn} = -V_{dc}/2$$

Line voltage is $V_{ac} = V_{an} - V_{cn}$

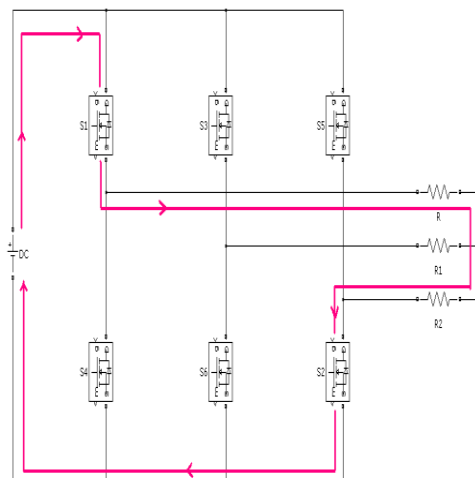


Fig. 4. (ii) Mode II

During mode 3, switches S2 and S3 conduct. At that time, Phase voltages are

$$V_{an} = 0$$

$$V_{bn} = V_{dc}/2$$

$$V_{cn} = -V_{dc}/2$$

Line voltage is $V_{bc} = V_{bn} - V_{cn}$

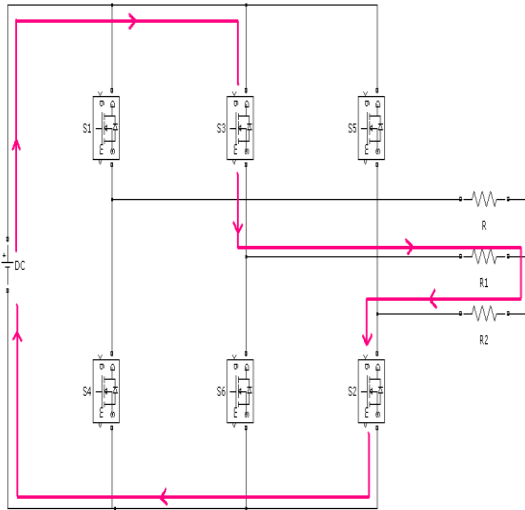


Fig. 4. (iii) Mode III

During mode 4, switches S3 and S4 conduct. At that time, Phase voltages are

$$V_{an} = -V_{dc}/2$$

$$V_{bn} = V_{dc}/2$$

$$V_{cn} = 0$$

Line voltage is $-V_{ab} = V_{an} - V_{bn}$

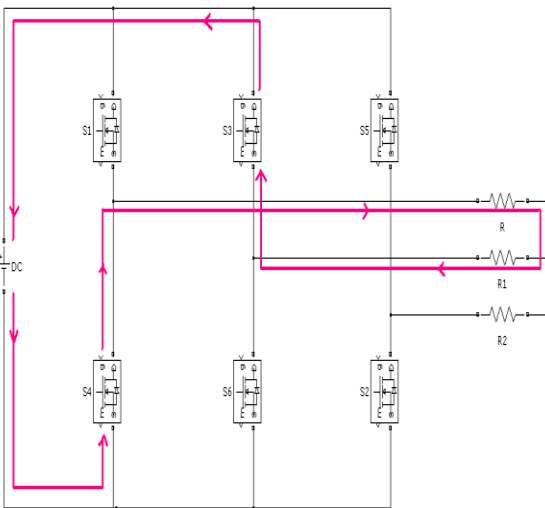


Fig. 4. (iv) Mode IV

During mode 5, switches S4 and S5 conduct. At that time, Phase voltages are

$$V_{an} = -V_{dc}/2$$

$$V_{cn} = V_{dc}/2$$

$$V_{bn} = 0$$

Line voltage is $-V_{ac} = V_{an} - V_{cn}$

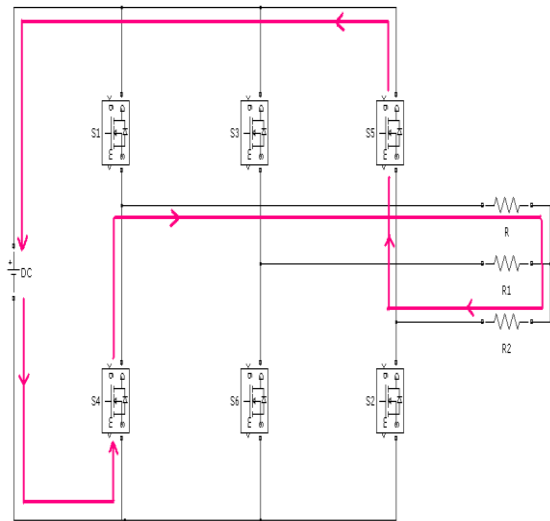


Fig. 4. (v) Mode V

During mode 6, switches S5 and S6 conduct. At that time, Phase voltages are

$$V_{an} = 0$$

$$V_{bn} = -V_{dc}/2$$

$$V_{cn} = V_{dc}/2$$

Line voltage is $-V_{bc} = V_{bn} - V_{cn}$

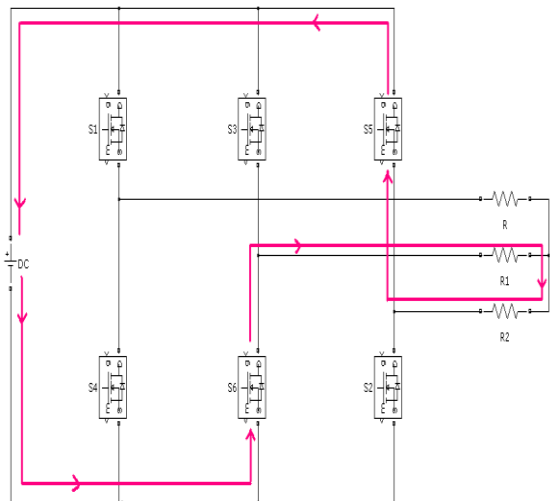


Fig. 4. (vi) Mode VI

C. COMPARISON WITH THE EXISTING CIRCUIT

In fig 2, the average of currents across inductors and battery meet

$$i_{L2} - i_{L1} = -i_B \quad (10)$$

According to [1] and [11], a summary of the circuits' working modes has been provided in Table I. For charging and discharging of battery, there exists different relationships between inductor currents. Fig. 3. will work in Continuous Conduction Mode (CCM), if

$$i_D = i_{L2} + i_{C1} - i_B > 0 \quad (11)$$

during the non-shoot through states; else, it works in Discontinuous Conduction Mode (DCM).

In steady state, the average current of capacitor C_1 is zero, and equation (11) becomes

$$i_B < i_{L2} \text{ or } i_{L1} > 0 \quad (12)$$

The power equation should be

$$P_B < P_{out} \quad (13)$$

Fig. 2 will work in CCM, if

$$i_D = i_{L1} + i_{C2} - i_B > 0 \quad (14)$$

during non-shoot through states. In steady state, the average current of capacitor C_2 is zero, and equation (14) will become $i_B < i_{L1}$ (15)

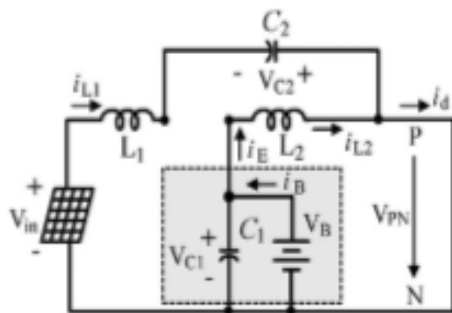
The power equation will meet

$$P_B < (D/1-2D) P_{in}, P_B < (D/1-D) P_{out} \quad (16)$$

From (13) and (16), we infer that Fig. 2. and Fig. 3. Always operate in CCM while the battery is charging. When the battery is discharging, both the circuits perform differently.

Fig. 5. a) shows the maximum discharging power of existing circuit's battery over the output power from inverter and the resultant limited inverter output power is shown in Fig. 5. b). DCM occurs when the battery discharging power exceeds its limitation curve.

From (13), (16) and Fig. 5, we infer that for the same inverter output power P_{out} , Fig. 3 has a wider range for battery discharging than that of Fig. 2.



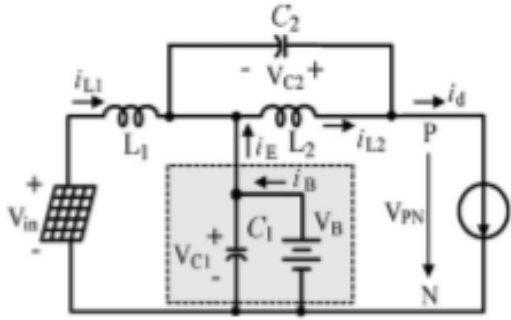


Fig. 4. Equivalent circuit of improved energy stored qZSI. (a) Shoot-through state; (b) nonshoot-through state.

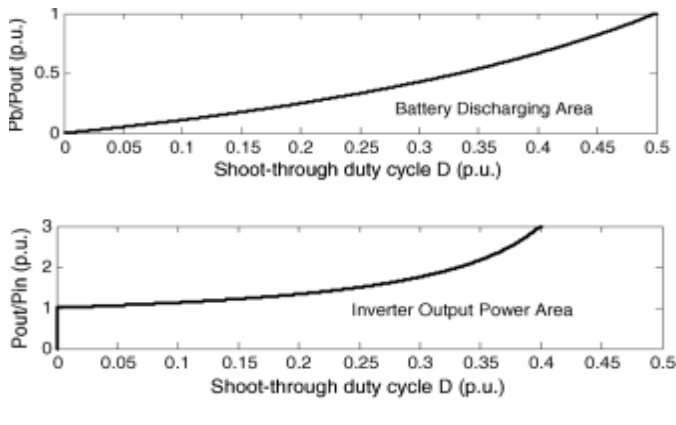


Fig 5. Battery discharging power and inverter output power limitations of Fig. 1. (a) Ratio of battery discharging power over the inverter output power; (b) ratio of inverter output power over the PV power.

TABLE I

COMPARISON OF WORKING MODES FOR TWO CIRCUITS

Power Relationship	Battery Power and Status	Inductor Currents	
		Fig. 1	Fig. 2
$P_{in} < P_{out}$	$P_B > 0$, discharge	$i_{L2} < i_{L1}$	$i_{L2} > i_{L1}$
$P_{in} > P_{out}$	$P_B < 0$, charge	$i_{L2} > i_{L1}$	$i_{L2} < i_{L1}$
$P_{in} = P_{out}$	$P_B = 0$, no exchange	$i_{L2} = i_{L1}$	$i_{L2} = i_{L1}$

IV. CONTROL METHOD

A. To achieve Constant DC-Link Peak Voltage

During a standard test condition, i.e., generally solar irradiation of 1000W/m, temperature of 25⁰ C, the PV panel has a voltage $V_{in,N}$, current $I_{in,N}$, and power $P_{in,N}$ at the Maximum Power Point. The dc-link peak voltage is

$$V_{PN}^* = 2 V_{C2}^* + V_{in,N} \quad (17)$$

Where V_{PN}^* is the desired value of dc-link peak voltage and V_{C2}^* is the desired value of capacitor C2 voltage related to V_{PN}^* .

Since there will be variations in solar irradiation and temperature, the PV panel has to have a new MPP, i.e., voltage $V_{in,N} + \Delta V_{pv}$, current $I_{in,N} + \Delta I_{pv}$, and power $P_{in,N} + \Delta P_{pv}$, then the dc-link peak voltage will be

$$V_{PN} = 2V_{C2} + V_{in,N} + \Delta V_{pv} \quad (18)$$

Equating equations (17) and (18), for achieving constant dc-link peak voltage, we obtain a condition,

$$i_B = - (V_{C2}^* - V_{C2})/R_b \quad (19)$$

When equation (19) is satisfied, we achieve constant dc-link peak voltage.

B. Closed loop control

PI controller is used to achieve closed loop control here. Using this, desired small variation of the shoot-through duty ration can be found.

$$D = k_p (i_B^* - i_B) + k_i \int (i_B^* - i_B) dt \quad (20)$$

Where k_p and k_i are the proportional and integral constants.

$$E_B = i_B^* - i_B \quad (21)$$

A feed-forward control will speed up the response by a steady state shoot-through duty ratio value,

$$D = (V_B - V_{in})/2 V_B - V_{in}$$

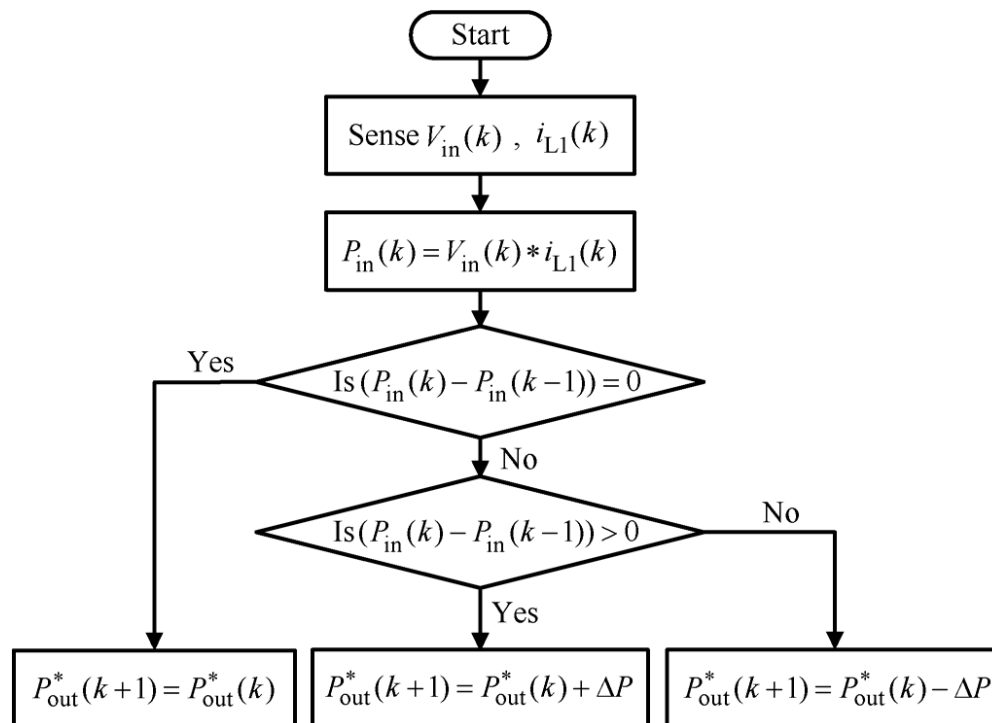


Fig. 6. MPPT algorithm

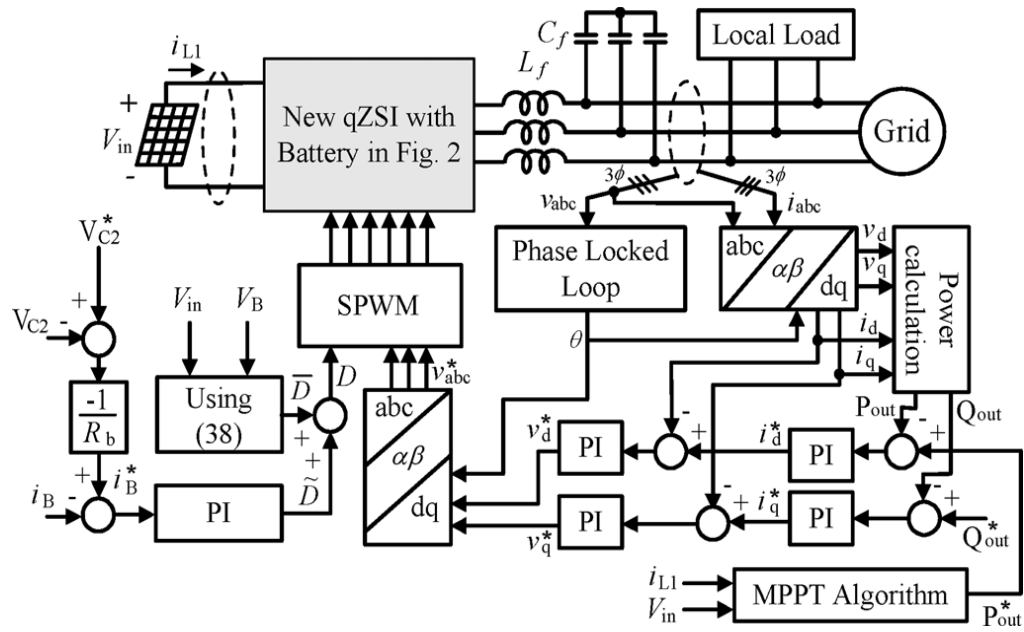


Fig. 7. Improved energy stored qZSI- based PV power system with constant dc-link peak voltage

V. SIMULATION RESULTS AND DISCUSSION

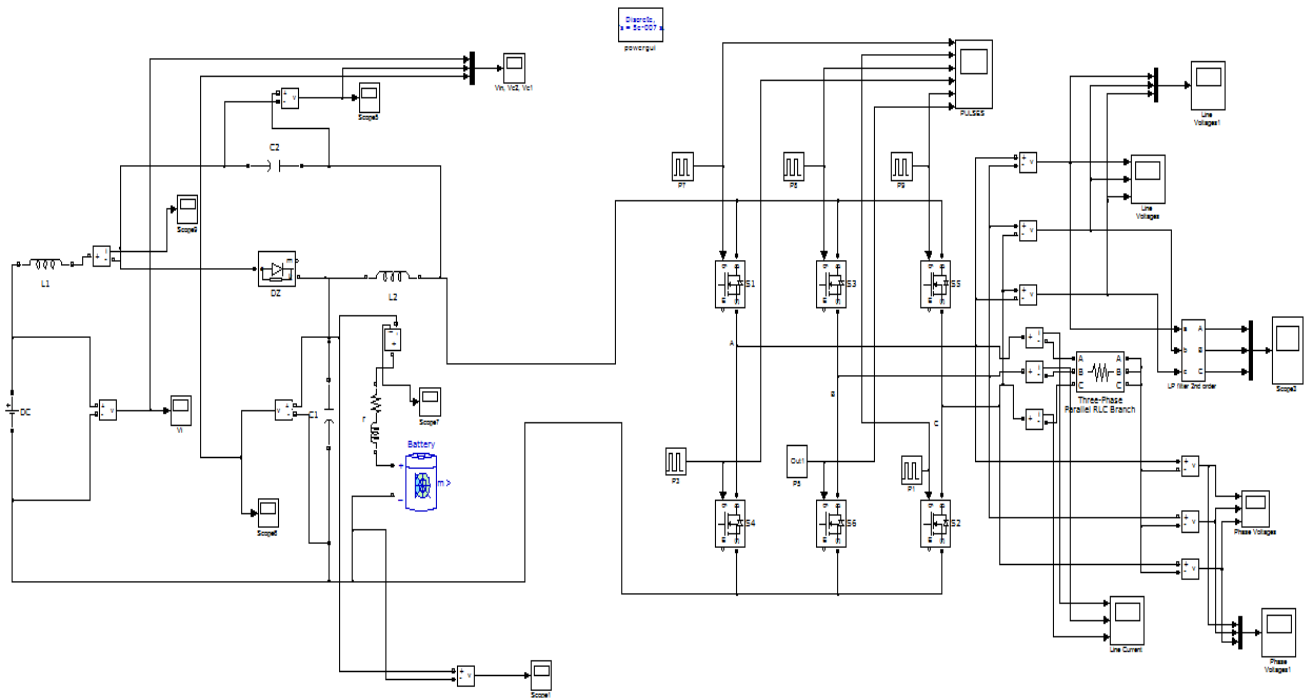


Fig. 8. Simulation of the improved qZSI

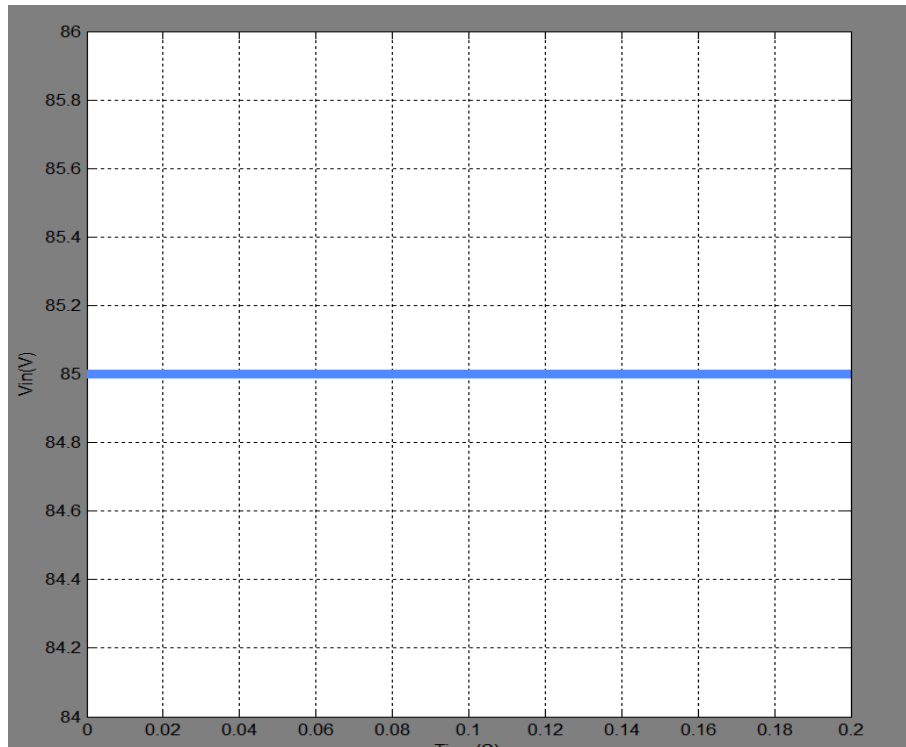


Fig. 9. Input voltage

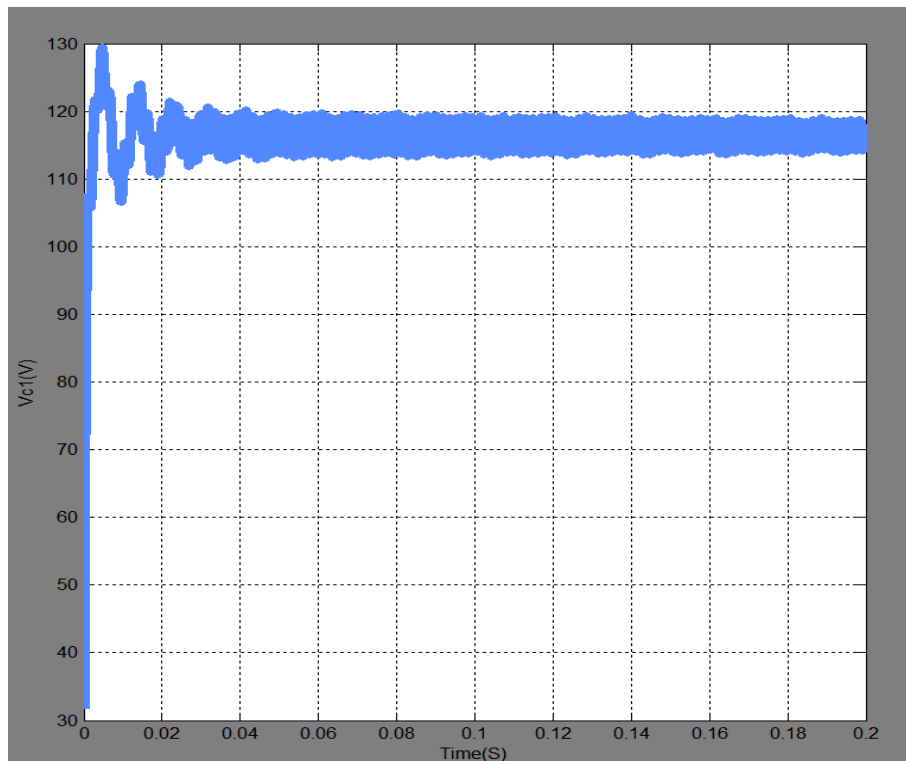


Fig. 10. Voltage across capacitor C1

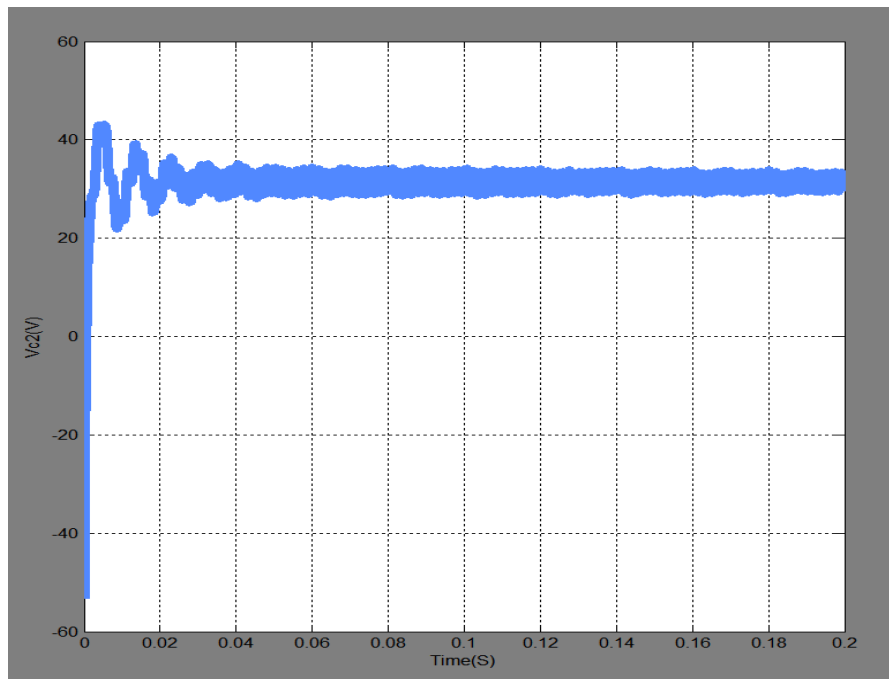


Fig. 11. Voltage across capacitor C2

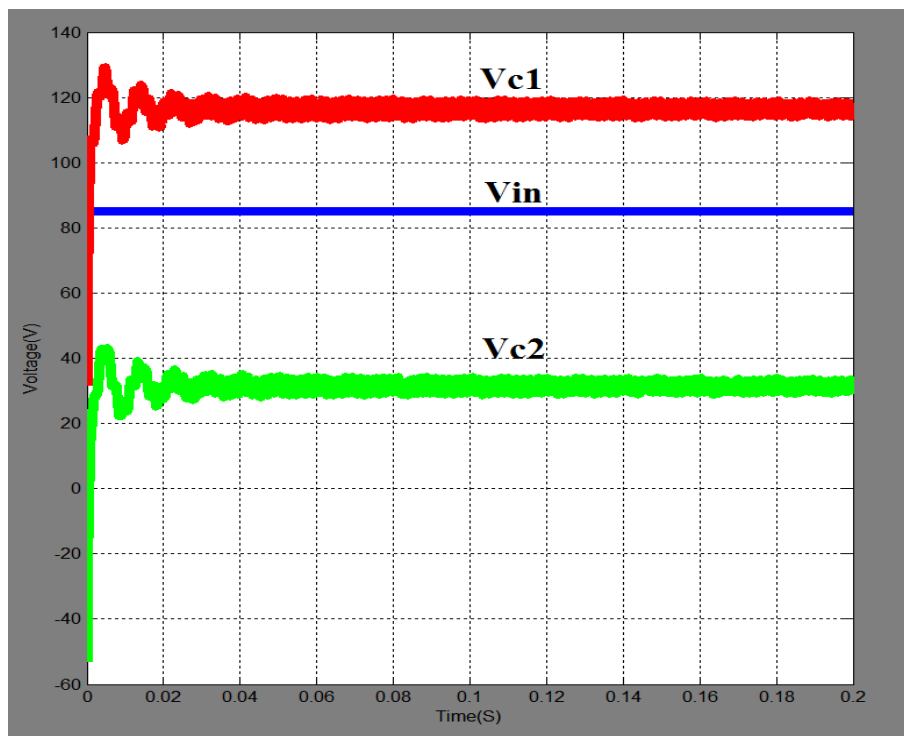


Fig. 12. Comparison between Input voltage and voltage across C₁, C₂

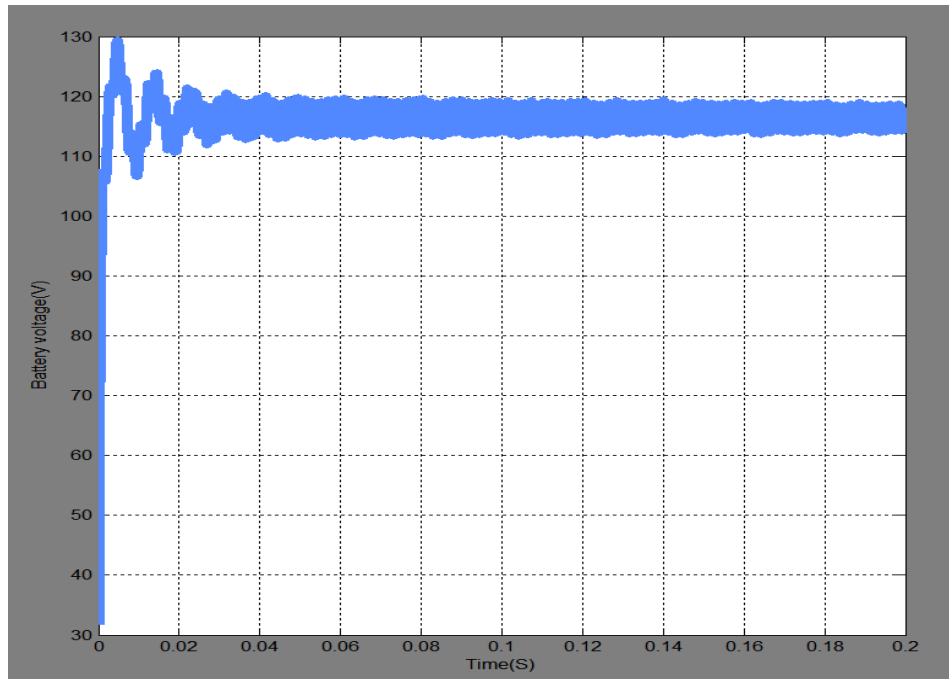


Fig. 13. Voltage across the battery

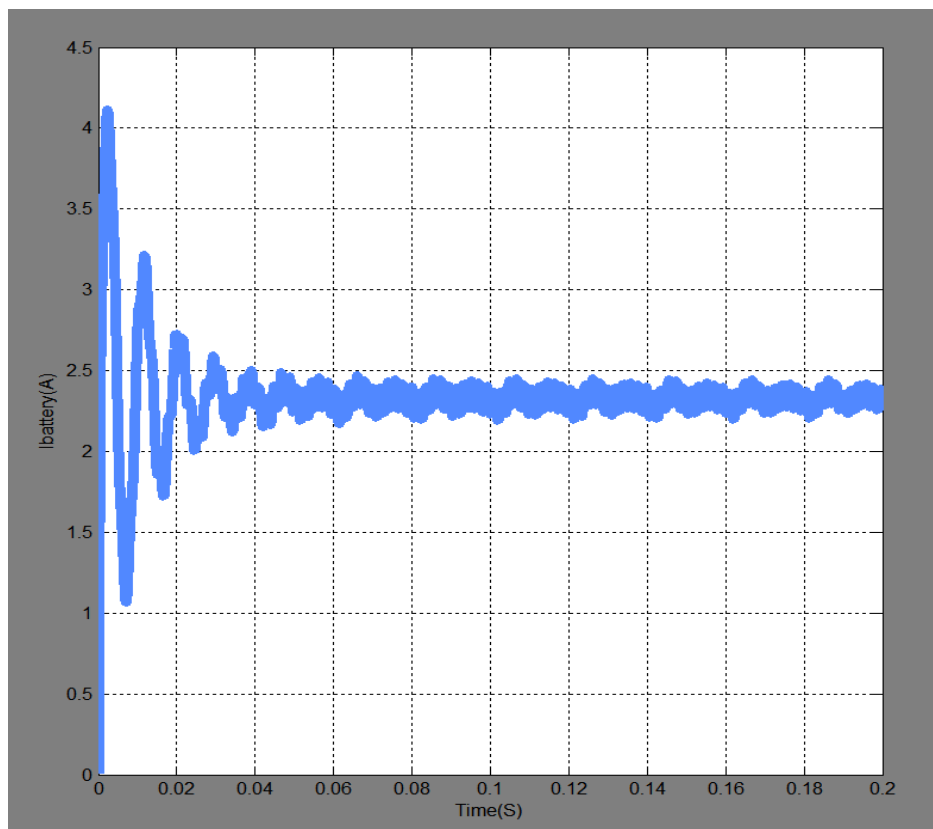


Fig. 14. Current across the battery

TRIGGERING PULSES:

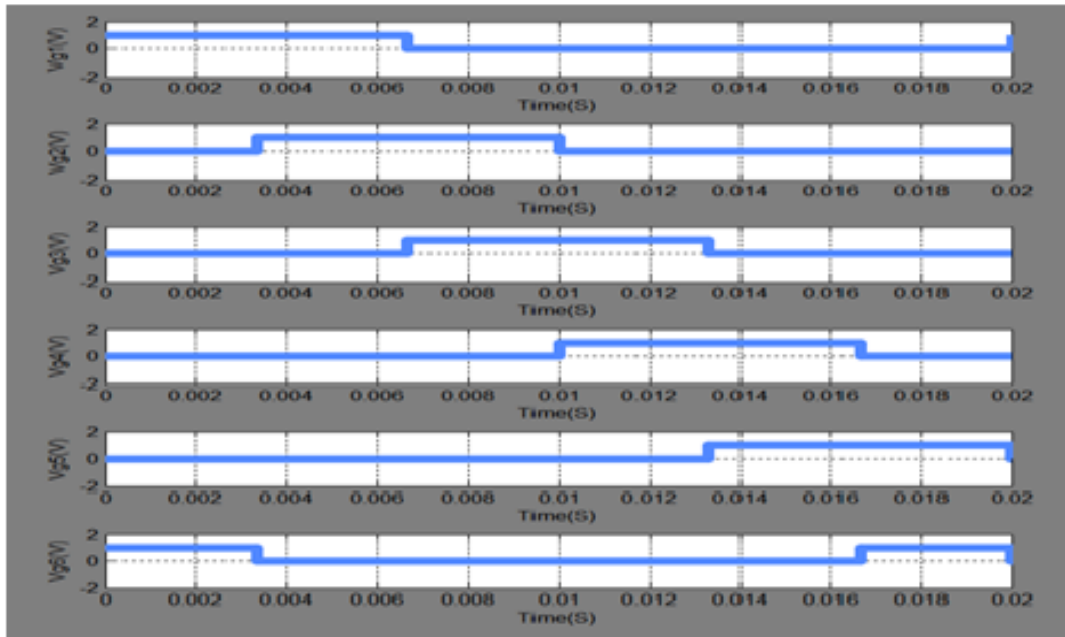


Fig. 15. Triggerring pulses for qZSI

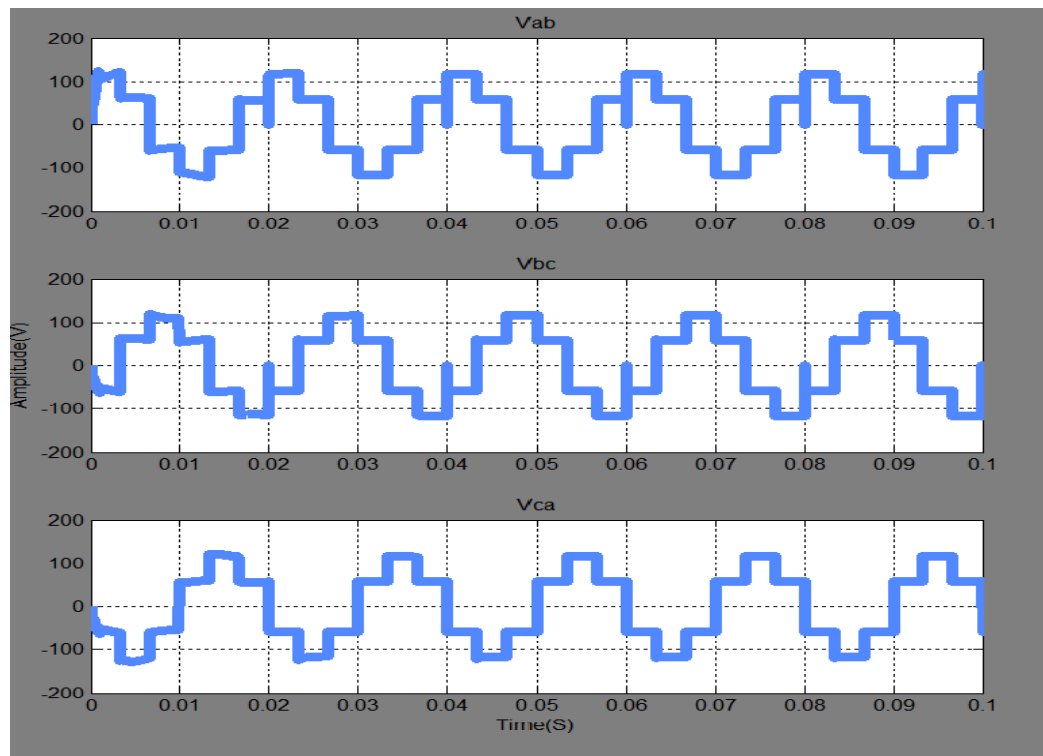


Fig. 16. Output Line voltages

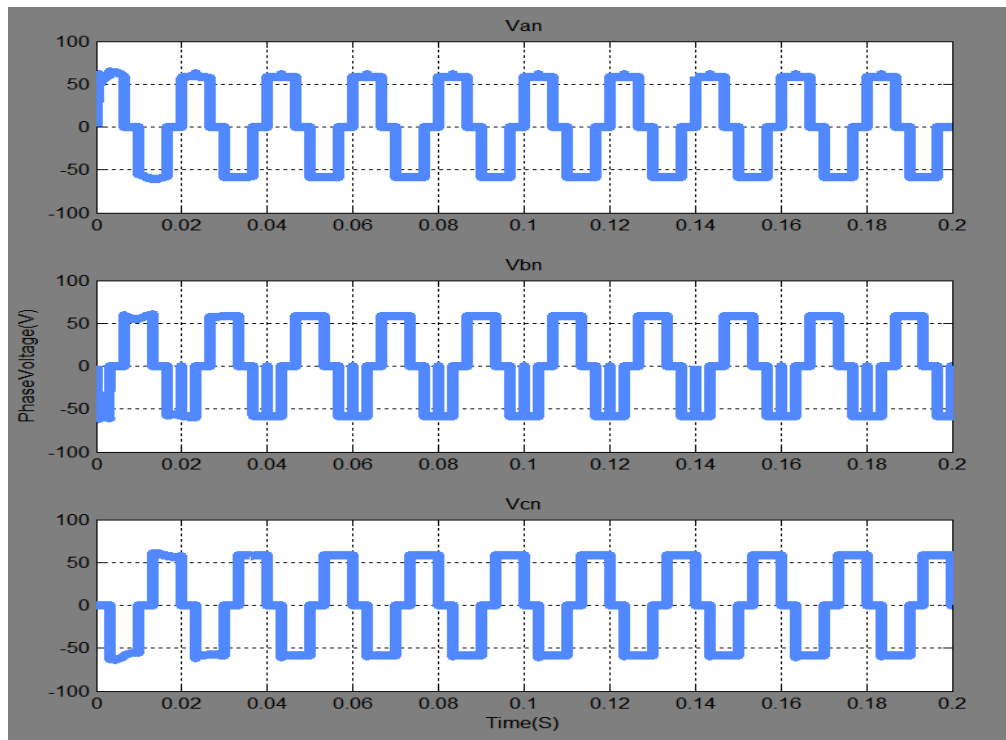


Fig. 17. Output phase voltages

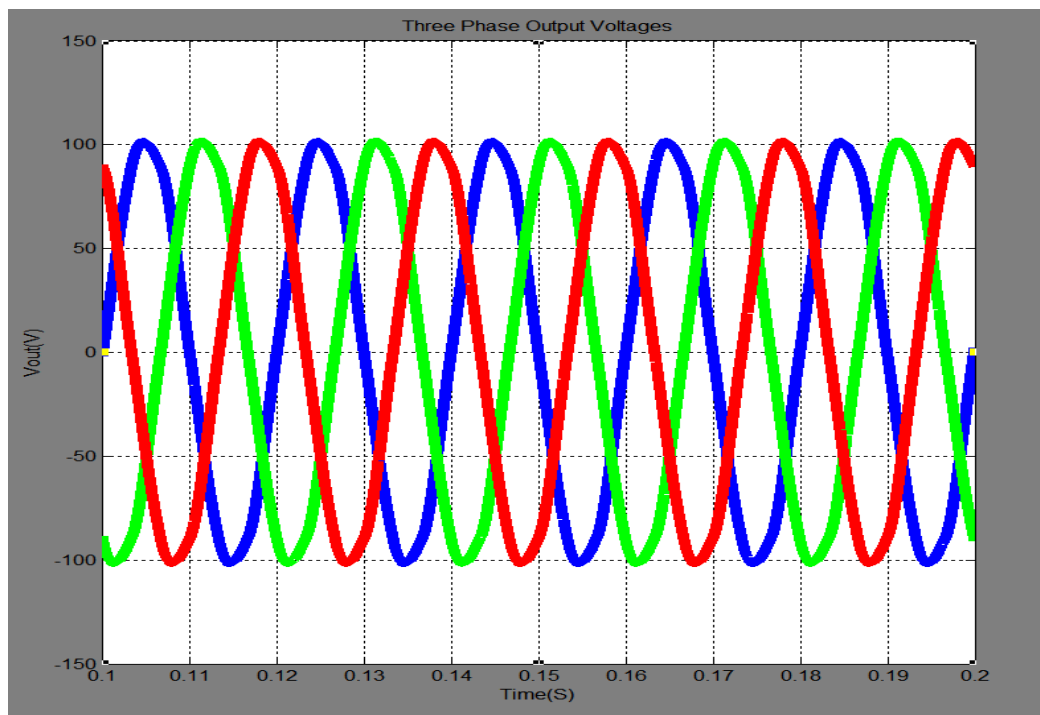


Fig. 18. Output voltage

VI. CONCLUSION

An improved qZSI based power generation system for PV applications with constant dc-link peak voltage was proposed. The shortcoming of narrow range of CCM was overcome. The new topology enables an improved ability to compensate power while maintaining a constant dc-link peak voltage with minimum harmonics.

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BIOGRAPHY OF AUTHORS

B. Kavya Santhoshi was born in Tamil Nadu, India on April 10, 1989. She has received the BE degree in Electrical and Electronics Engineering from Saveetha Engineering College, Anna University, Chennai, India in 2010. She is currently pursuing ME degree in Power Electronics and Drives at Jeppiaar Engineering College, Anna University, Chennai. She has participated and presented papers in national conferences. Her research areas are Renewable energy, industrial drives and power electronics.

Dr. M. Sasikumar was born in Tamil Nadu, India on June 17, 1977. He received the B.E degree in Electrical and Electronics Engineering from K.S. Rangasamy College of Technology, Madras University, India in 1999, and the M.Tech degree in Power Electronics from VIT University, in 2006. He has obtained his Ph.D. degree from Sathyabama university, Chennai, Tamil Nadu, India. Currently, he is working as a Professor in Jeppiaar Engineering College, Anna University, Chennai and is The Head of M.E Power Electronics and Drives department. He has 13 years of teaching experience. He has published over 30 technical papers in National and International Conferences / proceedings / journals. His research areas are power electronics drives and wind energy systems.