An Innovative Control Method of Solar Grid-connected Inverter with Effective Utilization of DC Power Source

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Abstract

The main disadvantages of current cascade multilevel inverter, it requires a lot of independent DC source, but a new type of cascade multilevel inverter, which decreases the number of DC sources by increasing the usage of DC sources. The new type of inverter is not only simple in structure, but also simple and effective in control algorithm that the simulation results certify that this new type of cascade inverter is feasible.

Keywords —switching pulse; inverter; cascade; energy storage capacitor.

1. Introduction

The main circuit structure of diodeclamped tri-level inverter, the multi-level inverter has entered a new stage of development, there have been a variety of topologies that the topology can be summed up in three kinds that divided into the following ways: diodeclamped structure, and capacitor-clamped structure and Hbridge cascade structure, the three inverter topologies have their own advantages and disadvantages, from the current point of view, since the cascade inverter needs the least components when the power level is the same that it is easy to implement scalable module with simple control, and each level could be independently controlled and can be mixed to achieve a combined application of a variety of devices that it is most viable under high-voltage output.

But a separate DC source is needed for each inverter unit of the H-bridge cascade inverter, therefore a large number of separate DC sources are needed when there are many output levels, which will make the structure of input transformer very complicated that it is not conducive to energy feedback, and the fault detection and diagnosis will become more difficult when

there are many cascade units. But the inverter mentioned in this paper only has one inverter with a separate DC source, it is very suitable for capacitor C to work as electrical energy storage component so as to reduce the number of DC sources.

1.1 Single-phase H-bridge Inverter Circuit:

Figure 1 is a single-phase H-bridge inverter circuit, assuming that the inverter adopts unipolar sinusoidal pulse width modulation SSPWM, inductive load current i and voltage and the direction of voltage $\lfloor u$ is as shown as follows



Figure 1 Single-phase H-bridge

Assuming S_1 , S_2 , S_3 , S_4 is two pairs of complementary switch sets, at the positive half-circle of the load current, if S2,S3 are conducted, load voltage U l=U dc, the DC power source outputs electrical energy to the load; if S₂, S₄ or S₁, S₃ are conducted, load voltage U 1=0, the DC source is does not output any electrical energy; If S₁, S₄ are conducted, load voltage U l=-U dc, the load feedbacks electrical energy to the DC source. In the negative half-cycle of load current i, if S₂, S₃ are conducted, load voltage Ul=Udc , the load feedbacks electrical energy to the DC source; if S₁,S₃ orS₂,S₄, are conducted, load voltage Ul=0 , the DC source does not output any electrical energy; if S1, S4 are conducted, load voltage Ul= -Udc , the DC source outputs electrical energy. To sum up, when the load voltage Ul=Udc is 0, the DC power source does not output any electrical energy; when the load feedbacks electrical energy to the DC source, the DC source absorbs the electrical energy, therefore, the DC source utilization is relatively low. Certain measures can be taken, when the load voltage is zero, to make sure that a part of electrical energy of singlephase H-bridge DC source shift to other energy storage devices to store up; when the load feedbacks, to make the

whole or most part of the electrical energy absorbed by DC source shift to other energy storage devices to store up and when it needs to output electrical energy to the load, the stored electrical energy then can be outputted together with the DC source, so as to improve the utilization of DC sources, which is the working principle of the new type of cascade inverter. Figure 2 is the circuit topology of improved H-bridge cascade inverter, the load section is connected to grid, the capacitance C in the figure is a storage component used to store electrical energy. We define the inverter composed of $S_1 \sim S_4$ as main inverter, and the inverter consisting of $S_5 \sim S_8$ as additional inverter.

2. New Multilevel Inverter Architecture

To operate a cascade multilevel inverter using a single DC source, it is proposed to use capacitors as the DC sources for all but the first source here solar grid is act as a DC sources. Consider a simple cascade multilevel inverter with two H-bridges as shown in Fig. 1. The DC source for the first H-bridge (H1) is a DC power source with an output voltage of Vdc, while the DC source for the second H-bridge (H₂) is a capacitor voltage to be held at Vdc/2 and the third H-bridge (H3) is a capacitor voltage to be held at 3Vdc/4. The output voltage of the first H-bridge is denoted by V1 and the output of the second H-bridge is denoted by V2 ,third Hbridge is denoted by V₃ so that the output of this two DC source cascade multilevel inverter is $V(t) = V_1(t)+V_2(t)+$ V3(t).

By opening and closing the switches of H1 appropriately, the output voltage V1 can be made equal to -Vdc ,0, or Vdc while the output voltage of V2 can be made equal to -Vdc/2 ,0, or Vdc/2 and output voltage of V3 can be made equal to -3Vdc/4 ,0, or3 Vdc/4 by opening and closing its switches appropriately. Therefore, the output voltage of the inverter can have the values -Vdc ,0, Vdc, -Vdc/2 , Vdc/2 , -3Vdc/4 , 3Vdc/4 which is seven levels Table I shows how a waveform can be generated using the topology of Fig2.



Figure2 new cascade inverter 2.1 Pulse Details With Output Wave Form

	Pulse Width	Phase Delay
Level I S2 & S3	45	0.0005
Level I SI & S4	45	0.01+0.0005
Level I I S2 & S3	30	0.002
Level II SI & S4	30	0.01+0.002
Level II I S2 & S3	10	0.004
Level II I SL & S4	10	0.01 ± 0.004

Level II I SI & S4



Total Out put Voltage Calculation

$$Vao = \sum_{n=1}^{m} (En)$$

- Vao=E1+E2+E3
- E1= 100V
- E2= 50V
- E3= 25V
- So Vao=175v

Here Vao is the total output level of our inverter.assume H1 level input voltage E1=100v, H2 level input voltage E2=50v and H3 level input voltage E3=25v.so total output Vao=175v.

2.2 Pulse Wave Form Simulation Output

Scope1									-	□ * ×
				Р	ULSE SEQUENCI	5				
0.5	1	1	!				!		ļ	
	i	i		i		i i	i i	i i	i	
1	1		i	!		!		ļ		
0.5					·····				i i	
0.										
1					<u> </u>					
0.5										
0										
1	!								1	
0.5	·····	·····								
0										
1		1	l i				1		1	
0.5										
0										_
1	1									_
0.5	·····									
0	0.01	0.02	0.03	0.04	0.05	0.06	0.07	0.08	0.09	0.1
Time offs	st: 0									

the above figure is pulse sequence ,as per follow the above mentioned pulse details to given to the pulse generator and given this pulse generator to scope ,run and get this pulse sequence.







Source Block Parameters: Pulse Generator3 Pulse Generato Output pulses: if (t >= PhaseDelay) && Pulse is on Y(t) = Amplitude Y(t) = 0 end Pulse type el using a var sten s ofan Parameters Pulse type: 🔟 -Time (t): Use simulation time -Amplitude: Period (secs): 0.02 Pulse Width (% of period): 45 Phase delay (secs): 0.0005 Interpret vector parameters as 1-D Cancel ок Help

Pulse generator level II Positive Cycle

Source Block Parameters: Pulse Generator6	5	×
Pulse Generator		-
Output pulses:		
if (t >= PhaseDelay) && Pulse is on Y(t) = Amplitude else $Y(t) = 0end$		
Pulse type determines the computational techniqu	ue used.	
Time-based is recommended for use with a variab based is recommended for use with a fixed step s of a model using a variable step solver.	ble step solver, while Sample- solver or within a discrete portio	m
Parameters		
Pulse type: Time based		-
Time (t): Use simulation time	-	-
Amplitude:		-
1		
Period (secs):		
0.02		
Pulse Width (% of period):		
45		
Phase delay (secs):		
0.0105		
Interpret vector parameters as 1-D		-
ОК	Cancel He	alp

2.4 Code for pulse generating using microcontroller

#include<reg51.h> int i,j,k; void delay(int a); void main() { P1=0x01; delay(1000); P1=0x03; delay(1000); P1=0x07; delay(1000); P1=0x03; delay(1000); P1=0x01; delay(1000); P1=0x00; delay(1000); P1=0x00;

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```
delay(1000);
P1=0x00;
delay(1000);
P1=0x00;
delay(1000);
P1=0x00;
delay(1000);
while(0);
}
void delay(int a)
{
for(i=0;i<=a;i++)
{
for(j=0;j<=1530;j++)
{
//for(k=0;k<=50;k++);
}
}
```

Conclusion:

The new cascade inverter can effectively reduce the number of DC sources by increasing utilization rate of DC sources, which makes the system more simple and with higher application value. Its disadvantages of old cascade inverter the capacitance of the energy storage capacitor is very large, and as compared with the normal cascade inverter, the output voltage effective value of new cascade inverter is relatively lower, but new cascade inverter overcomes all above disadvantages using the structure.

Reference

- Edited by Liu Fengjun Liu. Modern Inverter Technology and Its Applications [M]. Beijing: Electronic Industry Press ,2006:116-117.
- [2] Xiong Yu, Hu Changsheng and etc.. Topology Study of a New Type of

Triphase Direct-type Current-mode Multilevel Inverter [J]. 2004, 24 (1):163-167.

- [3] F. Zare, G. Ledwich. A Hysteresis Current Control for Singlephase Multilevel Voltage Source Inverters: PLD Implementations[J]. IEEE Trans. on Power Electronics, 2002, Vol.17(5):731-738.
- [4] K. Imaie, et. al. Control Strategies for Multiple Parallel Currentsource Converters of SMES System[J]. IEEE Transitions on Power Electronics, 2000, Vol.15(2):377-385
- [5] M. Lafoz, C. Veganzones, M. Visiers. A Novel Double Hysteresisband Current Control for a Three-Level Voltage Source Inverter[C]
 Proc. of PESC'00 Jun.2002, Vol.1: 21-26.
- [6] F. M. Antunes, H. A. C. Braga, I. Barbi. Application of a Generalized Current Multilevel Cell to a Current Source Inverter[C] Proceedings of IEEE International Conference on Industrial Electronics, Control and Instrumentation, 1995, Vol. 1:278-283.
- [7] Yu Xiong, et al. A New Single-phase Multilevel Current-source Inverter[C]. IEEE Conference on APEC04, 2004, Vol.3:1682-1685
- [8] R.W.Menzies, P.Steimer, J.K.Steinke. Five-level GTO Inverter for

Large Induction Motor Drives[J]. IEEE Trans. IA, 1994, Vol.30(4):938-944

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