Design of Low Power SRAM Memory Using 9T SRAM Cell

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Abstract—High integration density, low power and fast performance are all critical parameters in designing of memory blocks. Static Random Access Memories (SRAMs)'s focusing on optimizing dynamic power concept of virtual source transistors is used for removing direct connection between V_{DD} and G_{ND}. Also stacking effect can be reduced by switching off the stack transistors when the memory is ideal and the leakage current using SVL techniques This paper discusses the evolution of 9t SRAM circuits in terms of low power consumption, The whole circuit verification is done on the Tanner tool, Schematic of the SRAM cell is designed on the S-Edit and net list simulation done by using T-spice and waveforms are analyzed through the W-edit.

Keywords—Leakage Current; Low Power; SRAM; Stack tech; SVL; VLSI; USVL; LSVL; VTCMOS; MTCMOS.

I. INTRODUCTION

A SRAM cell involves of a latch, therefore the cell data is kept as long as power is turned on and refresh operation is not compulsory for the SRAM cell. SRAM is mainly used for the cache memory in microprocessors, mainframe computers, engineering workstations and memory in hand held devices due to high speed and low power consumption. For nearly 40 years CMOS devices have been scaled down in order to achieve higher speed, performance and lower power consumption. Technology scaling results in a significant increase in leakage current of CMOS devices. Static Random Access Memory (SRAM) continues to be one of the most fundamental and vitally important memory technologies today. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. High-performance on chip caches is a crucial component in the memory hierarchy of modern computing systems. In this technique each NMOS and PMOS transistor in the logic gates is split into two transistors are called Stack Technique, The proposed SRAM memory cell consumes lower power during read and writes operations compared to 6T conventional circuit. Also, a new 9T SRAM combining the advantages of these circuits is proposed in the paper. Also nine transistors (9T) SRAM cell configuration is proposed in this paper leakage is the only source of energy consumption in an idle circuit, a 9T SRAM which provides low leakage power is designed in this paper. A new leakage current reduction circuit called "improved Self-controllable Voltage Level (SVL)" circuit is developed and included to reduce the leakage power of 9T SRAM. Leakage is the only source of energy consumption in an idle circuit, A new nine-transistor (9T) SRAM cell with reduced leakage power consumption and enhanced data stability is proposed in this paper. The leakage power consumption of the new SRAM cell is reduced by 99.99% as compared to the conventional nine-transistor (9T) SRAM cells. The 9T SRAM cell provides two separate data access mechanisms for the read and write operations. During a read operation, the data storage nodes are completely isolated from the bit lines.

II. LITERATURE REVIEW OF DIFFERENT SRAM CELL

In this section the different types of SRAM circuits are discussed.

A. 6T SRAM Cell

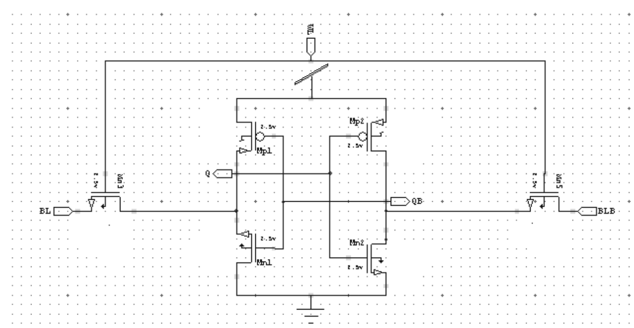


Fig.1 Schematic of 6T SRAM Cell

The schematic diagram of 6T SRAM cell is shown in Fig.1 During read, the WL voltage VWL is raised, and the memory cell discharges either BL (bit line true) or BLB (bit line complement), depending on the stored data on nodes Q and BQ. A sense amplifier converts the differential signal to a logic-level output. Then, at the end of the read cycle, the BLs returns to the positive supply rail. During write, VWL is raised and the BLs are forced to either VDD (depending on the data), overpowering the contents of the memory cell. During hold, VWL is held low and the BLs are left floating or driven to VDD. Each bit in an SRAM is stored on four transistors that form two cross-coupled. This storage cell has two stable states, which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations. A typical SRAM uses six MOSFETs to store each memory bit and the explanation here is based on the same. Access to the cell is enabled by the word line which controls the two access transistor M5 and M6 which, in turn, control whether the cell should be connected to the bit lines: BL and BLB. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided to improve noise margins. During read accesses, the bit lines are actively driven high and low by the inverters in the SRAM cell. This improves SRAM bandwidth compared to DRAMs. A SRAM cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested and writing when updating the contents

B. 6TSRAM Cell Using Stacking Technique

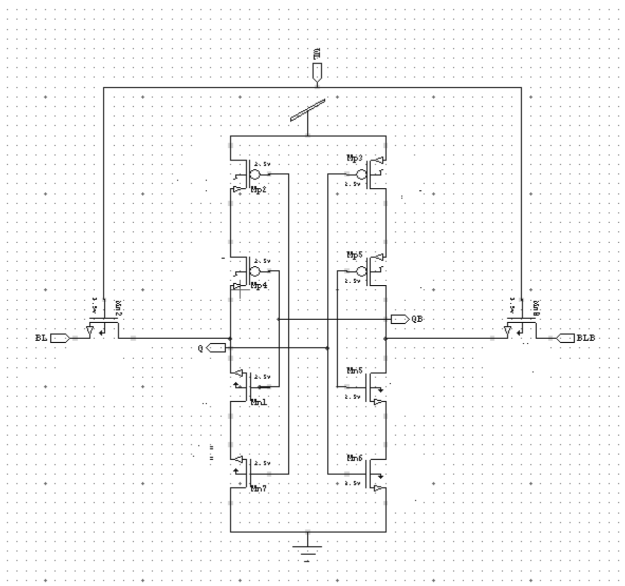


Fig.2 Schematic of Modified 6T SRAM Cell

In the Modified SRAM cell, is shown in Fig.2 the transistors M8, M4, M10 and M6 form cross coupled inverters. The basic idea behind our approach for reduction of leakage power is the effective stacking of transistors in the path from supply voltage to ground. A state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path." In our method, we introduce two leakage control transistors in each inverter pair such that one of the leakage control transistor is near its cutoff region of operation. Two leakage control transistors (PMOS) and (NMOS) are introduced between the nodes and of the pull-up and pull-down logic of the inverter. The drain nodes of the transistors and are connected together to form the output node of the Inverter. The source nodes of the transistors are connected to nodes of pull-up and pull-down logic, respectively. The switching of transistors is controlled by the voltage potentials at nodes respectively. This wiring configuration ensures that one of the leakage control transistor is always near its cutoff region, irrespective of the input. Hence the resistance of will be lesser than it's OFF resistance, allowing conduction. Even though the resistance of is not as high as it's OFF state resistance, it increases the resistance of to ground path, controlling the flow of leakage currents, resulting in leakage power reduction. Thus, the introduction of leakage control transistors increases the resistance of the path from supply voltage to ground.

C. 9T SRAM Cell

Schematic of 9T SRAM cell is shown in the Fig. 3. This circuit shows reduced leakage power and enhanced data stability. The 9T SRAM cell completely isolates the data from the bit lines during a read operation. The idle 9T SRAM cells are placed into a super cutoff sleep mode, thereby reducing the leakage power consumption as compared to the standard 6T SRAM cells.

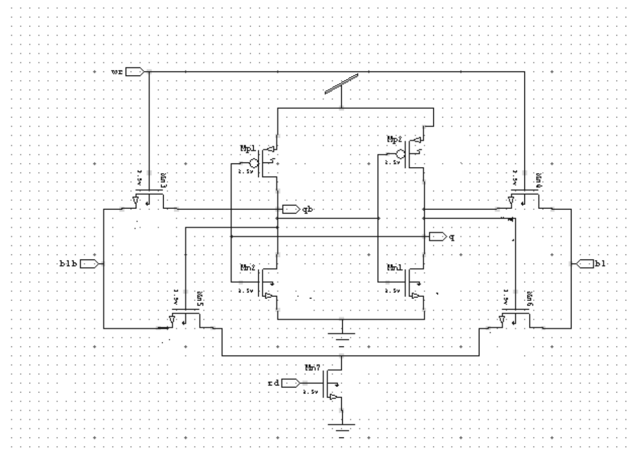


Fig.3 9T SRAM Cell

The upper sub-circuit of the new memory cell is essentially a 9T SRAM cell with minimum sized devices (composed of N1, N2, N3, N4, N5, N6, N7, P1, and P2 with W=Wmin and L=Lmin). The two write access transistors (N3 and N4) are controlled by a write signal (WR).The data is stored within this upper memory sub-circuit. The lower sub-circuit of the new cell is composed of the bit-line access transistors (N5 and N6) and the read access transistor (N7). The operations of N5 and N6 are controlled by the data stored in the cell. N7 is controlled by a separate read signal (RD).

1) 9T SRAM CELL Operation Table:

TABLE I. 9T SRAM CELL OPERATION

wr	rd	bl	blb	qbar	q	operation
0	0	x	x	0/1	1/0	hold
0	1	1	1	0/1	1/0	read
1	0	0	1	1	0	Write0
1	0	1	0	0	1	Write1

2) Write operation of 9T SRAM cell

During a write operation, WR signal transitions high while RD is maintained low, as shown in Fig. below N7 is cutoff. The two write access transistors N3 and N4 are turned on. In order to write a —0□ to Node1, BL and BLB are discharged and charged, respectively. A —0□ is forced into the SRAM cell through N3. Alternatively, for writing a —0□to Node2, BL and BLB are charged and discharged, respectively. A—0□is forced onto Node2 through N4.

3) Read operation of 9T SRAM cell

During a read operation, RD signal transitions high while WR is maintained low, as illustrated in Fig. below. The read access transistor N7 is activated. Provided that Node1 stores —1□, BL is discharged through N5 and N7. Alternatively, provided that Node2 stores—1□, the complementary bit line (BLB) is discharged through N6 and N7.

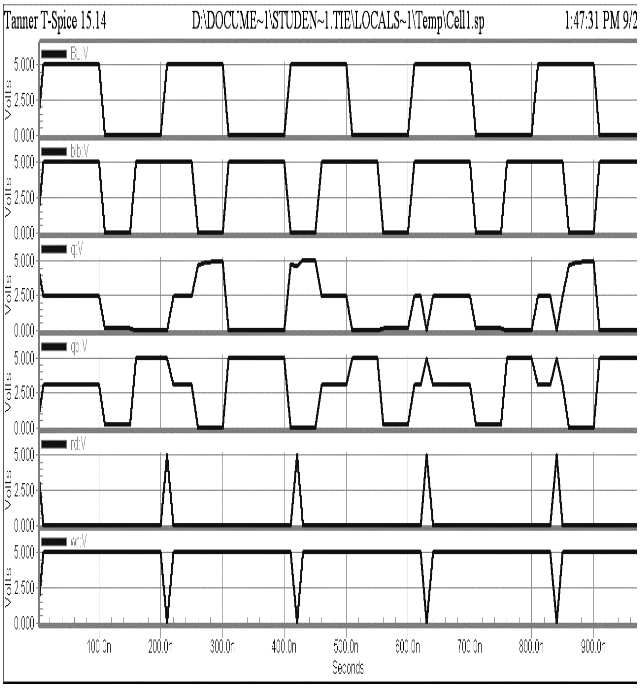


Fig 4. Simulation of 9T SRAM cell

D. 9TSRAM Cell Using Stacking Technique

Power consumption has become a critical design concern for many VLSI systems. Leakage current flowing through the NMOS transistor stack reduces due to the increase in the source to substrate voltage in the top NMOS transistor and also due to an increase in the drain to source voltage in the bottom NMOS transistor

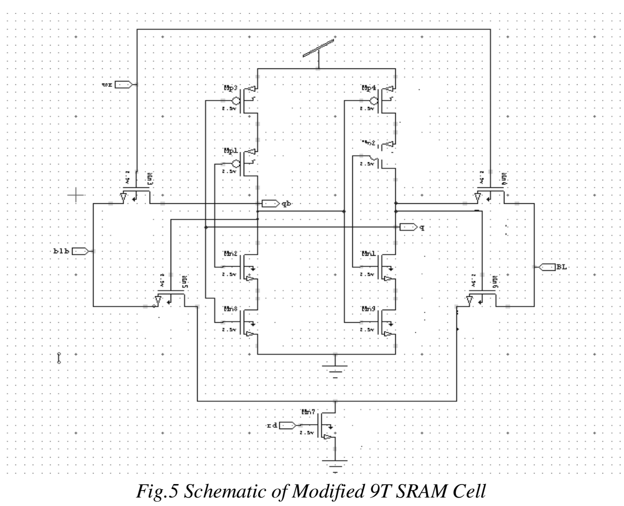


Fig.5 Schematic of Modified 9T SRAM Cell

This reduces the power dissipation in logic circuits. In this technique each NMOS and PMOS transistor in the logic gates are split into two transistors. A state with more than one transistor is off condition from a path from supply voltage to ground path consist of less leakage equated to the only one transistor off condition from a path from supply voltage to ground path.

E. Self-Controllable Voltage Level

There are two well-known techniques that reduce leakage power (Pst). One is to use a multi-threshold-voltage CMOS (MTCMOS). It effectively reduces Pst by disconnecting the power supply through the use of high *Vt* MOSFET switches. However, there are serious drawbacks with the use of this technique, such as the fact that both memories and flip-flops based on this technique cannot retain data. The other technique involves using a variable threshold-voltage CMOS (VTCMOS) that reduces PST by increasing the substrate-biases. This technique also faces some serious problems, such as a large area penalty and a large power penalty due to the substrate-bias supply circuits requires low leakage power.

F. Improved self-controllable voltage level circuits:

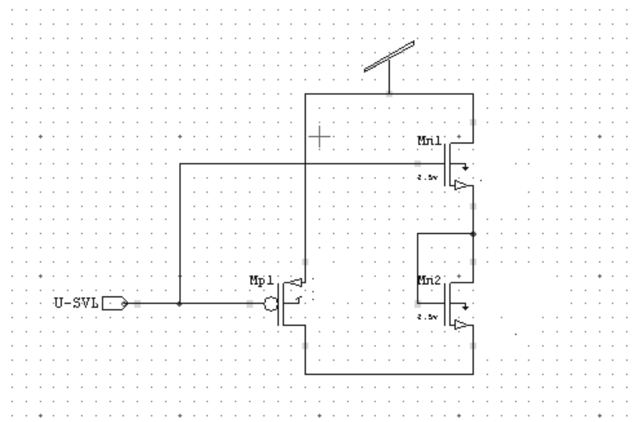


Fig 6. Upper SVL circuit

In the above figure shows Upper SVL circuit. The impedance of a MOS transistor increases with the width of the transistor.pmos1 in the above circuit having width means it offers very high resistance in that path between VDD and VSS. So that leakage in this SVL mode is very less. And also nmos1 and nmos2 forms a working in normal mode of the cell.nmos2 acts as a resister to reduce current in active mode by connecting above way the leakage is further reduced.

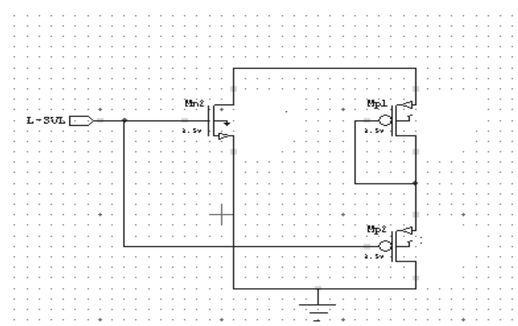


Fig.7 Lower SVL circuit

The above circuit represents lower SVL circuit. nmos3 work in the SVL mode and pmos2 and pmos3 work in the normal mode of the cell.pmos2 acts as a resister to reduce leakage. These two techniques reduce leakage current compared to the previous SVL.

TABLE II. 9T SRAM CELL SVL OPERATION

Mode	**Upper SVL Circuit**	**Lower SVL Circuit**
Active	pMOS switch is turned on	nMOS switch is turned on
	VDD is supplied	Vss is supplied
Stand-by Mode	nMOS switch is turned on	pMOS switch is turned on
	V_D (<V_{DD}) is supplied	V_S(>V_{SS}) is supplied

G. 9T SRAM Cell With Normal SVL Circuits

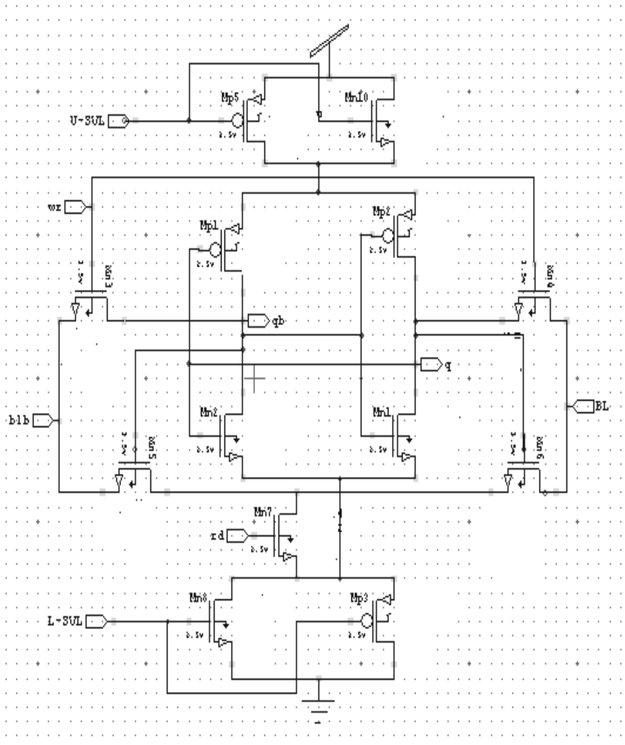


Fig8. 9T SRAM Cell With Normal SVL circuits.

The above circuits work with normal SVL circuits. The circuit consists of normal 9T SRAM cell and upper SVL circuit and lower SVL circuits and operation of the circuit explained with the table below.

TABLE III. 9T SRAM CELL OPERATION WITH SVL

u-svl	l-svl	wr	rd	bl	blb	qbar	q	operation
1	0	0	0	x	x	0/1	1/0	hold
0	1	0	1	1	1	0/1	1/0	read
0	0	1	0	0	1	1	0	Write0
0	0	1	0	1	0	0	1	Write1

The role of SVL circuits is to reduce leakage currents in standby mode or hold mode because so much leakage power in standby mode can destroy the cell. So we need to reduce that leakage. The proposed improved SVL circuits can reduce leakage more. By observing the table for inputs logic 1 and 0 to the SVL circuits we can say that the cell operates in hold mode. In this mode nmos8 on in upper SVL circuit and pmos4 on in lower SVL circuits to reduce the leakage.

H. 9T SRAM Cell With Improved SVL Circuits

The circuit in fig.9 reduces the leakage power in standby mode to protect the cell. The operation of the cell explained with the help of table above.nmos9 and pmos3 and also to reduce leakage further pmos4 and nmos10 is placed. In other modes the cell operates as normal operations read, write. In write mode SVL provides expansion of the noise margin.

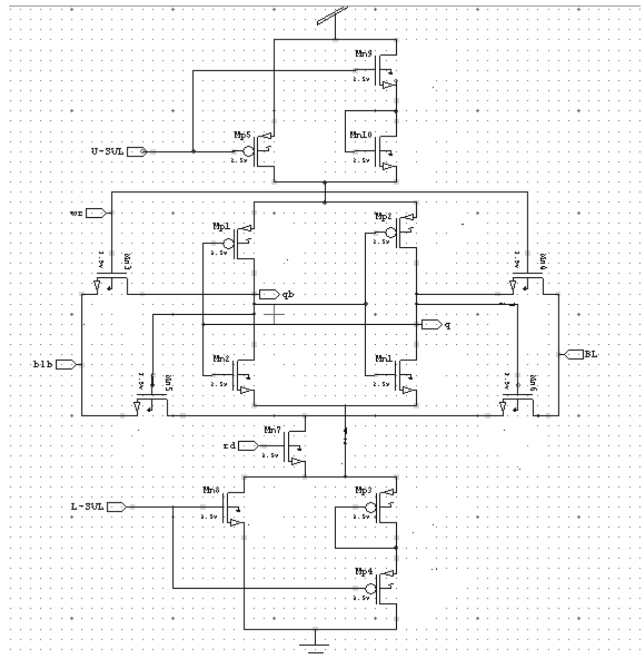


Fig9. 9T SRAM cell with Improved SVL circuits

I. 9TSRAM Cell With Normal SVL Circuits Using Stacking Technique

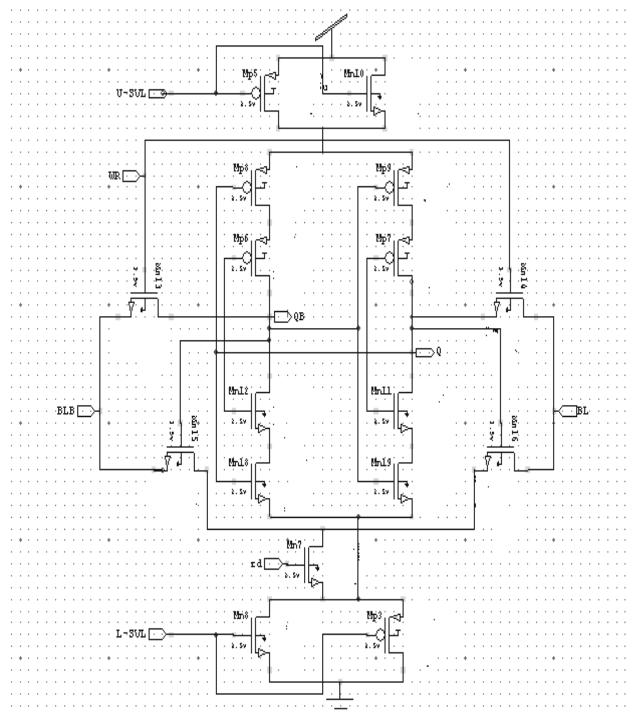


Fig10 .TSRAM Cell With Normal SVL Circuits Using Stacking Technique

The above circuits work with normal SVL circuits. The circuit consists of normal 9T SRAM cell Using Stacking Technique and upper SVL circuit and lower SVL circuits and operation of the circuit explained with the table below.

J. 9TSRAM Cell With Improved SVL Circuits Using Stacking Technique

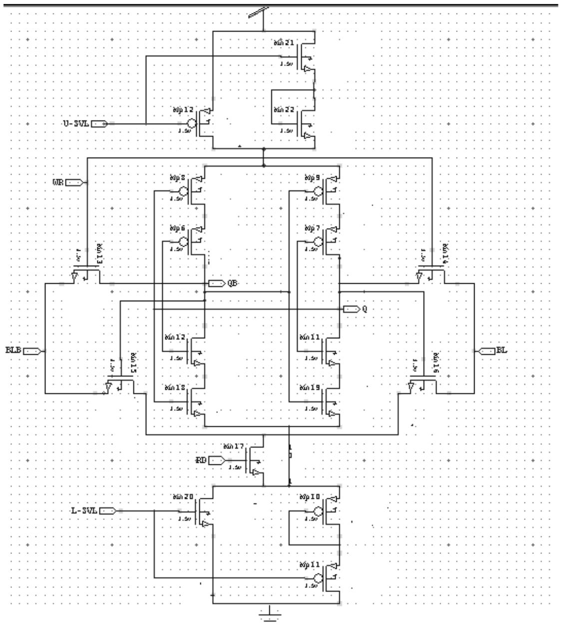


Fig11 .9TSRAM Cell With Improved SVL Circuits Using Stacking Technique

The above circuits work with Improved SVL circuits. The circuit consists of normal 9T SRAM cell Using Stacking Technique and upper SVL circuit and lower SVL circuits and operation of the circuit explained with the table below.

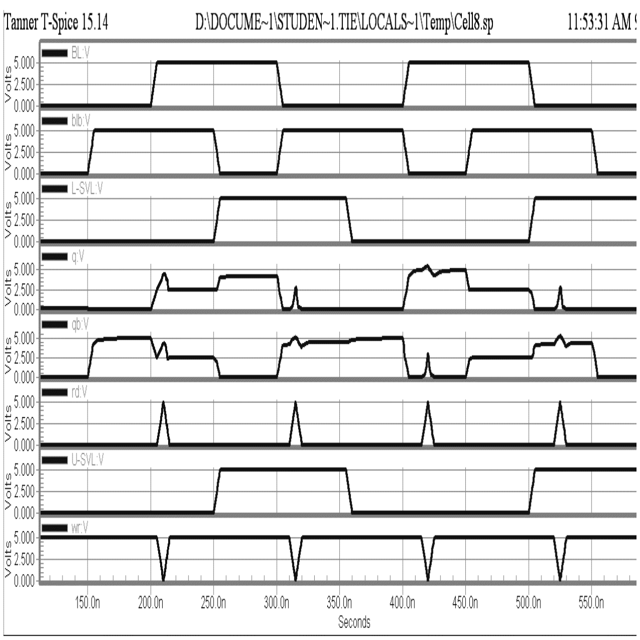
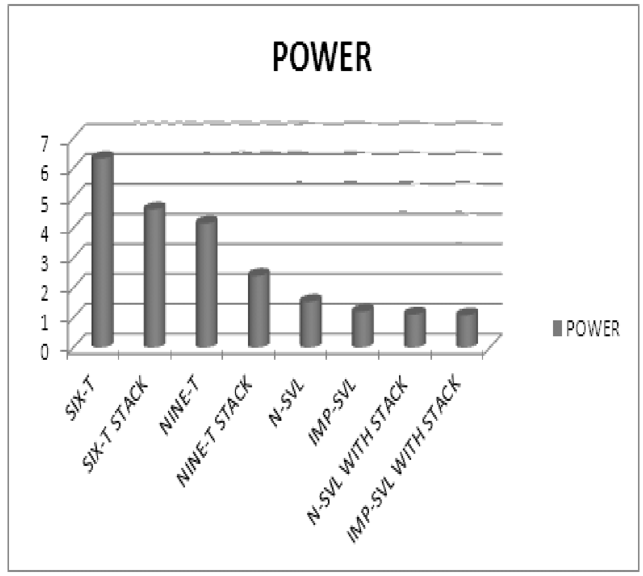


Fig 12. Simulation of 9T SRAM cell with Improved SVL circuits



III.SIMULATION RESULTS

A. power consumption:

TABLE IV. POWER CONSUMPTION

TECHNIQUE	POWER CONSUMPTION (e-003 watts)
6T SRAM	6.317031
6T SRAM With Stack	4.618457
9T SRAM	4.153286
9T SRAM With Stack	2.402564
9T SRAM Normal SVL	1.533267
9T SRAM Improved SVL	1.206302
9T SRAM Normal SVL With Stack	1.114284
9T SRAM Improved SVL With Stack	1.081955

IV .CONCLUSION AND FUTUREWORK

Improved SVL circuit will play a major role in future. The effect of the improved SVL circuit on the leakage current through the load circuit (i.e., reduction in current) was examined. The improved SVL circuit and the load circuit were designed using CMOS technology. Sub-threshold memory design has received a lot of attention in the past years, but most of them use large number of transistor to achieve sub threshold region operation. The new technique inherently process variation tolerant, this makes the new approach attractive for Nano computing in which process variations is a major design constraint. In this circuit we have several advantages in different modes that is in operating mode high Vds to load circuits for high speed operation, in stand-by mode high Vt through ―On MOS switches to load circuits for minimum stand-by leakage power, data retention, high noise immunity, small stand-by power dissipation, negligible speed degradation, negligible area overhead, high noise immunity, data retentions at stand-by mode. In this circuit the standby leakage power is reduced by which total average power also reduced.

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[5], Design a 5T SRAM by using self controllable voltage level leakage reduction technique with CMOS Technology Laxmi Singh1, Ajay Somkuwar2 1Department of Electronics & Communication, Corporate college of Technology, Bhopal, INDIA. 2Department of Electronics & Communication Bhopal, MP, INDIA .