A new current-mode min-max circuit

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***Abstract*— A low-voltage CMOS current-mode Winner take all and looser take all circuits are designed in 0.35 µm standard CMOS technology.Simulation results using HSPICE that verify the functionality of circuit with 1.5 V supply are presented. The circuit can find application in the implementation of Fuzzy and Neural Network circuits.**

***Keywords*— Analog processing circuit, WTA, LTA, Low Voltage.**

I. INTRODUCTION

Winner-Take-All (WTA) and Looser-Take-All (LTA) circuits are the analog important and major function building blocks. The function of WTA and LTA circuits identify the largest and the smallest input variable, respectively, and restrains the remaining ones. WTA and LTA are widely used in hardware implementation of fuzzy logic systems, nonlinear filters and self-organizing neural networks, vector quantization, Hamming network, competitive learning, etc.

WTA and LTA can be extensively categorized as the current mode and voltage mode structure. Using current mode analog circuit design has received wide attention due to the supply voltage scaling down and their potential of lower power consumption [1]-[3]. In addition existing voltage mode structures are larger than current mode structures in hardware and area.

In this paper we proposed a novel current mode WTA and LTA. There are several structures of current mode WTA and LTA circuit proposed on the literature [4]-[6]. Our proposed circuits can work under low voltage (1.5 V) that is lower in comparison with previous works.

Section II presents the proposed WTA circuit architecture and describes it operation. Section III presents the proposed LTA circuit architecture. Simulation results are presented in section IV. Conclusion is presented in section V.

II. WTA CIRCUIT DESCRIPTION

The function of the WTA is to accept input signals, compare their values and produce a high digital output value (logic ‘one’) corresponding to the largest input, while all other digital outputs are set to low output value (logic ‘zero’) [7].

Figure 1 shows the block diagram of the WTA circuit. The circuit includes a 2-input current maximum selector [8] with a voltage inverter.

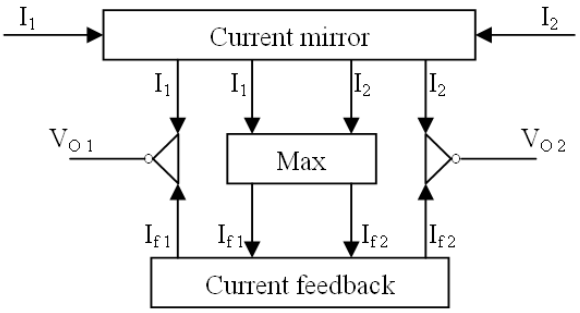

Fig 1. Winner Take All circuit

A. THE CURRENT MAX SELECTOR

The 2-input current maximum selector is shown in Figure 2. The proposed current max selector has 2 input branches and each branch consists of an FVF [14], formed by voltage follower Mai, and current sensing transistor Mci.

Transistor Mai in an FVF performs as an improved voltage follower and the Gate-Source voltage drop of this transistor is constant (neglecting second-order effect) and independent of the load.

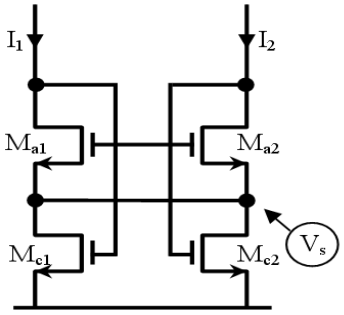

Fig 2. 2-input current max circuit

Transistor Mci operates as a current sensing device. It can sink large current by keeping its Drain voltage approximately constant. Moreover, the existing impedance at the Source of transistor Mai is very low due to the feedback loop.

The principle of operation of the circuit is as follow. The voltage at node “VS” follows the maximum of input currents I1 , I2, with a DC level shift VGSn where n denotes the maximum current.

In this condition the transistor (Ma1 or Ma2) which carrying the minimum current, have the greater Gate-Source

voltage than the value that should have to operate in saturation mode, at this condition this transistor operates in triode mode with Drain-Source voltage value close to zero, thus the current sensing transistor is turning off in this branch and minimum and maximum currents passed through current sensing transistor of winning branch due to properties of FVF cell.

B. THE OVERALL STRUCTURE OF WTA CIRCUIT

The circuit of the 2-input WTA is shown in Figure 3. The currents (I1, I2) are the inputs of the circuit.

Each current is mirrored into current max selector, as well as, into the feedback circuit due to PMOS current mirror M12, M22.

Thus the input current of each voltage inverter is:

$$I_{i1} = I_1 - I_{f1} \quad (1)$$

$$I_{i2} = I_2 - I_{f2} \quad (2)$$

We assume at the steady state, the current I1 is the largest input current I1=max (I1, I2)

So

$$I_{f1} = I_1 + I_2 \quad (3)$$

$$I_{f2} = 0 \quad (4)$$

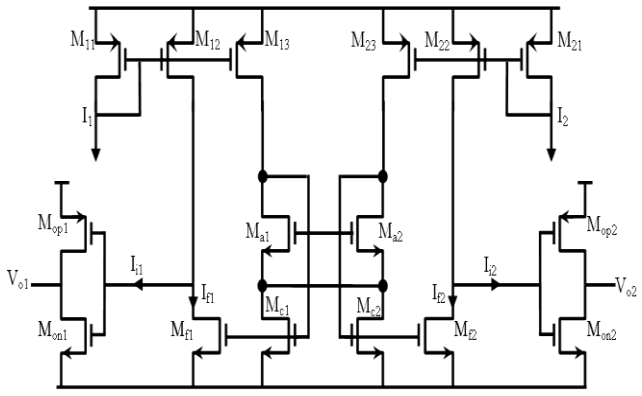

Fig 3. 2-input WTA circuit

From the "Eq. (1)" - "Eq. (4)" the input current of each voltage inverter is:

$$I_{i1} = I_1 - (I_1 + I_2) = -I_2 \quad (5)$$

$$I_{i2} = I_2 - 0 = I_2 \quad (6)$$

This means that only one input current of the voltage inverter corresponding to minimum current is positive and all the other currents are negative. Thus the digital voltage outputs of the circuit will be at logic.

$$\begin{cases} V_{o1} = \text{'one'} \\ V_{o2} = \text{'zero'} \end{cases} \quad (7)$$

III. LTA CIRCUIT DESCRIPTION

A LTA-Min circuit can be formed as shown in Fig.4. The basic structure of the proposed circuit consists of two branches. Each of these branches consists of a voltage follower transistor (MA_i) and a current sensing transistor (MC_i). The gate of the MA_is is connected to a fixed voltage V_b.

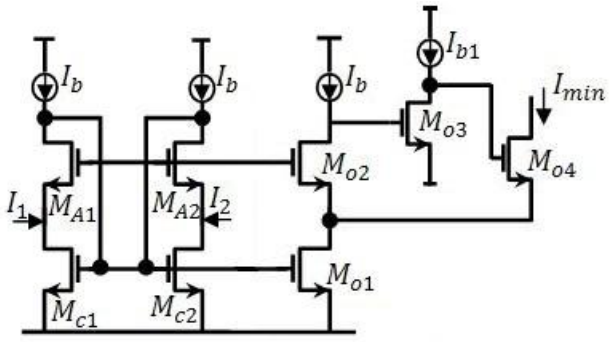

Fig. 4 The prposed Minimum current selector

The gate-to-source voltages of MC_is are equal and proportional to minimum currents I_1 and I_2 so that these transistors have the different drain-to-source voltages. In hence, voltage follower transistors of all of the branches will be turning off, except one, which is in the looser branch. This voltage follower transistor has the minimum current that transmits it to the output by using high quality and appropriate current mirror (MO_1 and MO_4).

Transistor $M_{O2,}$ current source I_b and V_b forces the Drain-to-source voltage of transistor M_{O1} to be a constant value to M_{ci} which is in the looser branch and carry the minimum current. To have the high output impedance, the output cascade transistor M_{o4} is driven by the drain of transistor M_{o3}. As the polarity in the drain of transistor M_{o2} is reversed, an inverting stage is required to drive the gates of transistor M_{o4} .This Inverting stage provides additional gain-boosting, which increases the output impedance. The inverter amplifier has been implemented by means of transistor M_{o3} and biasing current I_{b1}.

The minimum supply voltage is limited by the path formed by current source I_b, M_b and $M_{C,}$ so the minimum supply voltage is expressed as

$$V_{DD}^{\min} = V_{GSb} + V_{DSC,sat} + V_{DSb,sat} \quad (8)$$

Where V_{GSB} is the gate-to-source voltage of transistor M_b, $V_{DSC,sat}$ is the minimum operating voltage for the current source I_b and $V_{DSC,sat}$ is the minimum drain-to-source voltage

of transistor M_c that cause to operate it in saturation region and can be small as 0.15 V in 0.35 µm CMOS technology, V_{tn}=0.6 V. so, the minimum supply voltage is given by

$$V_{DD}^{\min} = V_{tn} + V_{DSsat} = 0.7 + (3 \times 0.115) = 1.15$$

In this paper corresponding to achieved results, we selected V_{DD}=1.5 V in order to have an appreciable voltage swing.

IV. Simulation Result

The proposed WTA and LTA were laid out in standard 0.35µm CMOS technology. Post layout simulations from extracted circuit were performed for a 1.5 V supply using HSPICE and level 49 parameters (BSIM3V3).

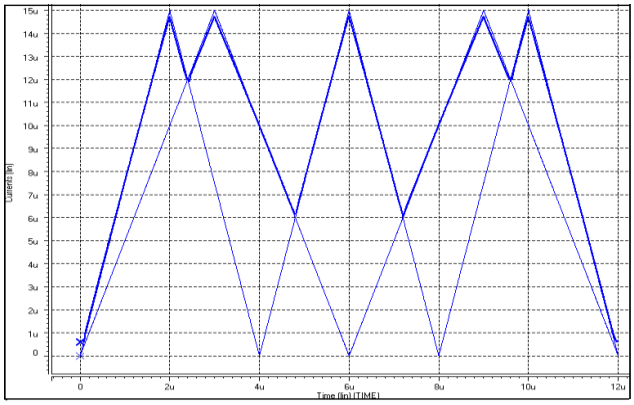

Fig .5 Transient simulation result for the proposed MAX circuit

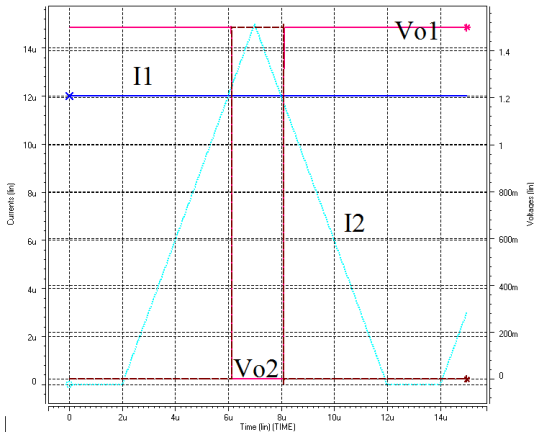

Fig. 6 Transient simulation result for the proposed WTA circuit

Transient simulation result for the proposed MAX circuit is shown in Fig.5 where the output is indicated with solid lines. Fig.6 shows the output transient response of the WTA circuit for two different currents.

Fig.7 shows the transient simulation result for the proposed Minimum current selector in 500 KHz. Fig. 8 shows the output of the proposed circuit in 50 MHz.

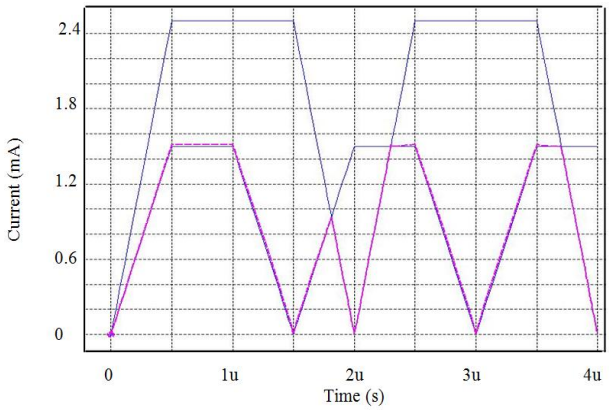

Fig. 7 Min circuit operation in 500 KHz

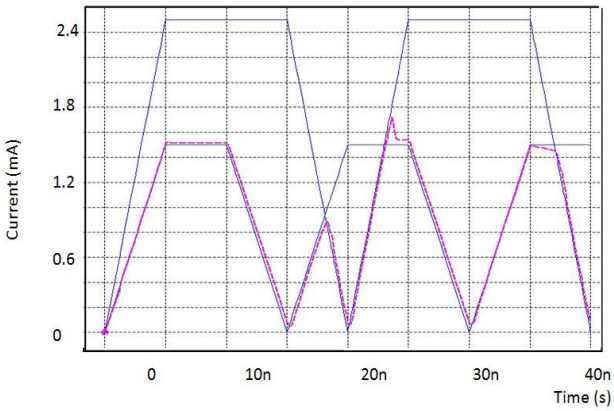

Fig. 8 Min circuit operation in 50 MHz

V. Conclusions

A new, Low-voltage current mode multi input WTA and LTA circuits are described. The proposed circuits work with a single 1.5V power supply which makes them suitable for low-voltage portable application.

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