Low-Voltage CMOS Defuzzifier Circuit for Using in Fuzzy Controller

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Abstract— in this paper, novel current-mode analog Defuzzifier circuit is presented. The proposed circuit is designed in 0.18 μm standard CMOS technology.Simulation result using HSPICE that verify the functionality of circuit with 1 V supply is presented. The circuit can find application in the implementation of defuzzifier in Fuzzy controller circuits.

Keywords Analog processing circuit, Translinear loop, Squarer, Low Voltage, Multiplier.

I. INTRODUCTION

In fuzzy systems there are three main steps (1)fuzzification or membership function generation, (2) fuzzy inference or fuzzy rule evaluation, and (3)defuzzification. Excellent tutorial overviews on a utility of a fuzzy system and its application have been reported in many articles.[1-3]
In this paper a new current-mode defuzzifier is presented. This application usually requires current-mode divider circuit to perform its operation [4-7].Consequently; a new current mode divider is designed to act as a defuzzifier.

Several techniques to design CMOS divider/multiplier circuits have been proposed in the literature.The first approach is to use the current-mode square root and squarer circuit based on the square-law characteristics of MOS transistors operated in the saturation region.[7] However, the power consumption by this approach is large; the square circuit requires bias currents for all input signals to make MOS transistors operate in the saturation region. The second approach is to use translinear principle of MOS transistor operated in the saturation or subthreshold region. [4, 5]

The translinear principle, introduced by Barry Gilbert in 1975 [4], is one of the most important circuit theory contributions in the electronics era. In its original formulation, the translinear principle provides a simple and efficient way to analyze and synthesize nonlinear circuits based on bipolar junction transistors (BJTs). Due to their exponential characteristics, the translinear principle can be extended to MOS transistors operating in saturation. This approach has the advantage of low power consumption.

In this paper we proposed a new low-voltage divider/multiplier circuit based on the properties of translinear loop which is work in saturation region. The proposed circuit work with a single power supply 1V which is lower than previous proposals and make it suitable for low-voltage and portable applications.

Section II reviews the properties of translinear loops. The proposed squarer circuit is described in section III. Section IV presents the proposed low voltage divider/multiplier and simulation result is presented in section V. Conclusion is presented in section VI.

II. VOLTAGE TRANSLINEAR LOOPS

Consider, for instance, the circuits of Figs. 1a and 1b. They represent a four-transistor voltage-translinear loop in stacked and up-down topology, respectively, with two MOSFETs connected clockwise and another pair connected counterclockwise. Applying the KVL, the following expression is obtained for both cases:
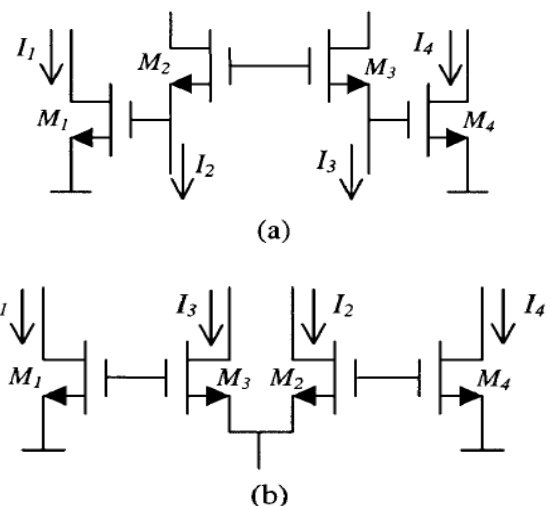

Fig 1. Voltage translinear-loop (a) Stacked Topology (b) Up-down topology

$$V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4} \qquad (1)$$

And replacing $V_{GS} = V_{th} + \sqrt{\frac{2I}{\mu C_{ox}\frac{W}{L}}}$ and assuming equal MOS transconductance factors and threshold voltages, the following expression is obtained:

$$\sqrt{I_1} + \sqrt{I_2} = \sqrt{I_3} + \sqrt{I_4} \qquad (2)$$

Hence, several nonlinear current-mode functions can be implemented by properly injecting such currents. For instance, if we force

$$I_3 = I_4 = \frac{I_1 + I_2 + 2I_5}{4} \qquad (3)$$

Being I_5 a certain current, after squaring both sides in (3) and rearranging, currents I_1, I_2 and I_5 become related by

$$I_5 = \sqrt{I_1 I_2} \qquad (4)$$

Therefore, a geometric-mean circuit is obtained if I_1 and I_2 are the input currents and the output current is a copy of I_5 .Alternatively, a squarer/divider is obtained if the output is a copy of I_2 and the inputs are I_1 and I_5 . The simplest way to force (4) is to use the well-known structure of Fig. 2. However, the diode-connected MOSFET of the current mirror precludes very low voltage operation due to the stacking of two diode-connected transistors.
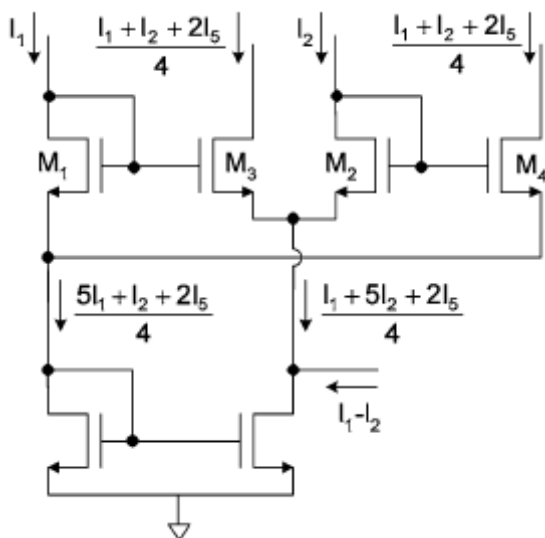

Fig 2. The square/Divider using stack loop

III.   THE NEW LOW-VOLTAGE SQUARER CIRCUIT

Equation (4) can be alternatively implemented using the novel topology of Fig. 3. Now a FVF, formed by transistors M_1 and M_{F1}, sets the proper reference dc voltage at the loop nodes. An advantage of this structure is that the source of M_1 is a very low impedance node, so that voltage at this node is

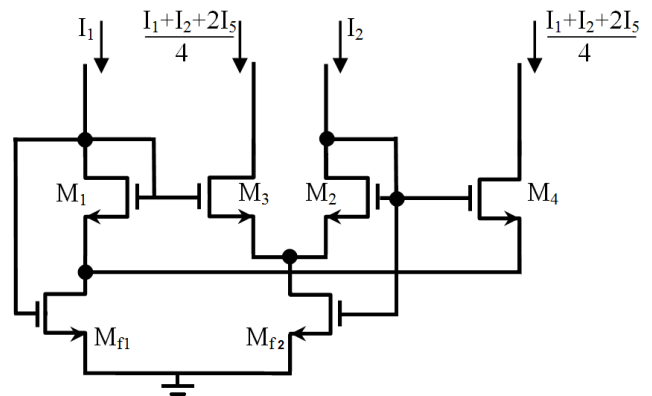kept essentially constant regardless of the input and output current

Fig 3. The proposed low-voltage squarer circuit

The minimum supply voltage is limited by the path formed by I_b, M_1 and M_{F1} so the minimum supply voltage is

$$V_{DD}^{min} = V_{GSF} + 2V_{DSbsat} \qquad (5)$$

where V_{GSF} is gate-source voltage of M_{F2} , V_{DSbsat} is the minimum voltage drop in current source I_b and can be as small as 0.1V in 0.18μm CMOS technology, V_{th} =0.55 V for NMOS so,

$$V_{DD}^{min} = V_{th} + 3V_{DSbsat} = 0.55 + 3 * 0.1 = 0.85V$$

We have selected V_{DD}=1V in order to have an appreciable voltage swing.

IV.   THE NEW LOW-VOLTAGE DIVIDER/MULTIPLIER CIRCUIT

Following will described the principal of operation of the proposed Divider/Multiplier.
Consider the following expression:

$$I_{OUT} = \frac{I_1 I_2}{I_3} \qquad (6)$$

I_1,I_2 ,I_3 and being current signals. Equation (6) can be equivalently written as

$$I_{OUT} = \frac{\left(\sqrt{I_1 I_2}\right)^2}{I_3} \qquad (7)$$

It becomes apparent that if we were able to calculate the geometric mean of two currents and then to introduce the output current into a squarer circuit having the following input-output characteristic:

$$I_{OUT} = \frac{I_1 I_2}{I_3} \qquad (8)$$

Then, according to (8), a current-mode multiplier/divider implementing could be obtained. This idea is shown schematically in Fig. 4, where the geometric-mean and squarer/divider outputs have been assumed to be flowing out.
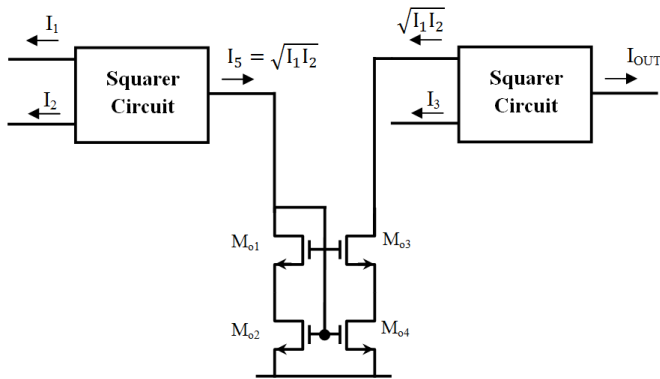

Fig 4. Principle of the multiplier/divider circuit

Fig.5 shows the proposed low-voltage current-mode divider/multiplier circuit. In this topology, I_a is a constant bias current so the output current I_{OUT} will be the multiplication of current I_1 by current I_3.
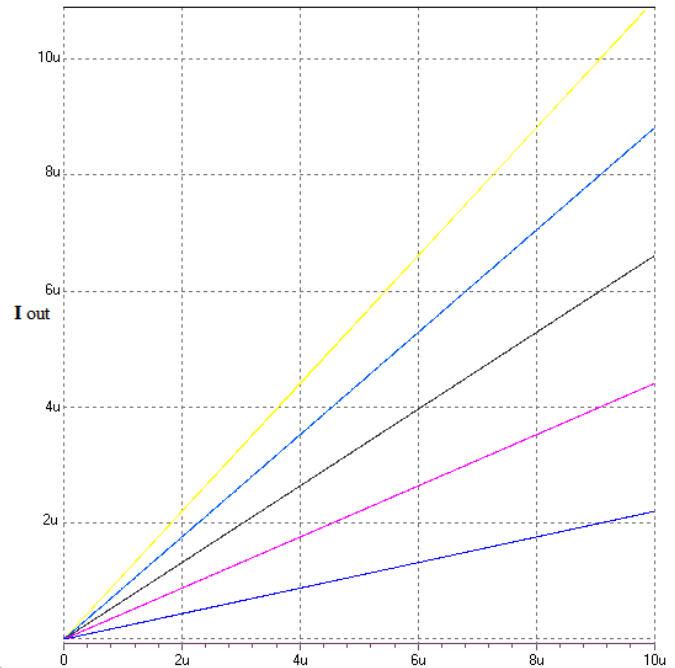
V. SIMULATION RESULT

The squarer circuit depicted in Fig.3 and the current multiplier in Fig.5 was laid out in standard 0.18μm CMOS technology. Post layout simulations from extracted circuit were performed for a 1 V single power supply voltage using HSPICE and level 49 parameters (BSIM3V3).

Fig.6 shows SPICE simulation of the squarer circuit where a constant DC current is applied as I_1 and a triangular current for I_2. The result is showed by I_{OUT} .

The DC characteristic of proposed current multiplier is presented in Fig.7 where a constant bias current is applied to the circuit as I_3 .
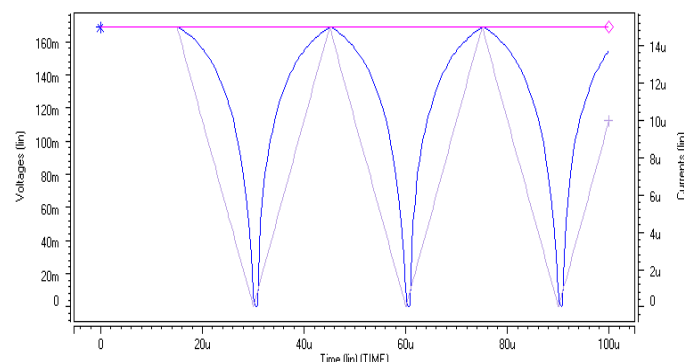

Fig 6. Simulation result of proposed squarer

Fig 7. Simulated DC transfer characteristic of the multiplier (I_{out} as a function of I_1 with I_3=10u and I_2 ranging from 2uA to 10uA in 2uA step)

VI. CONCLUSIONS

A new, Low-voltage current Defuzzifier circuit based on devider circuit is described. The proposed circuit works with a single 1V power supply which makes it suitable for designing low-voltage fuzzy controller circuit.
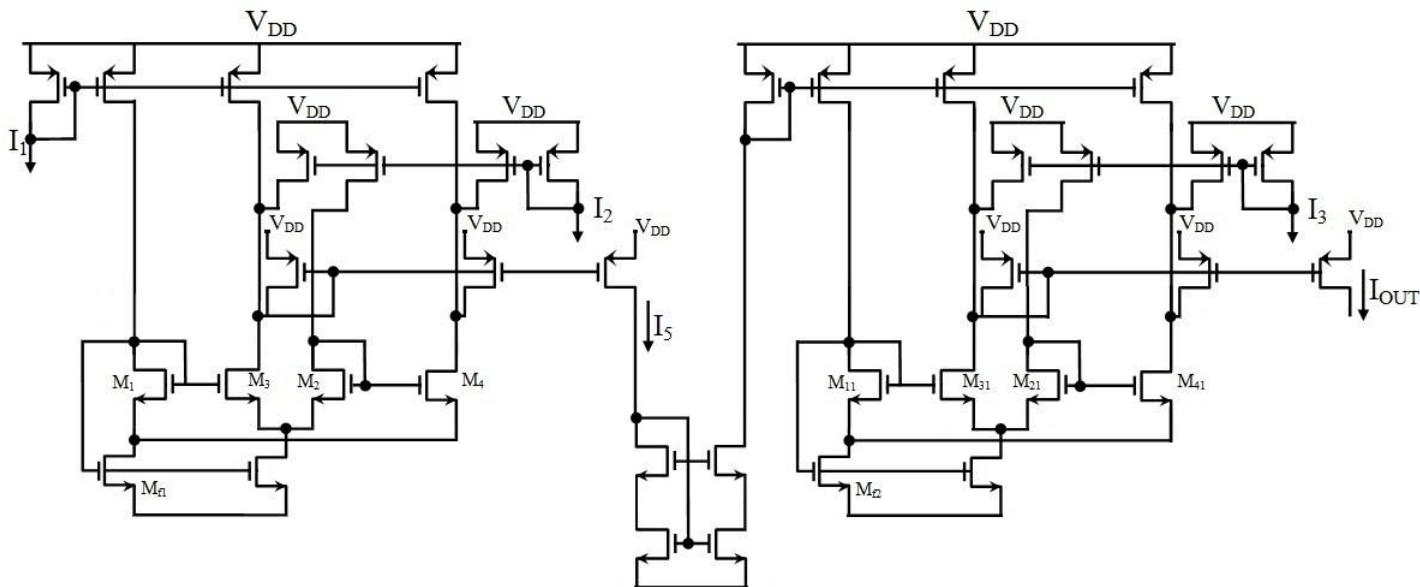
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Fig 5. The low-voltage current defuzzifier

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