Leakage power analysis Techniques for Nano CMOS Digital Circuits

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***Abstract*—**Due to the growing impact of subthreshold and gate leakage, static leakage is contributing more and more towards the power dissipation in deep submicron Nano CMOS technology. The high leakage current in the nano Cmos is becoming a significant proportion of power dissipation in digital circuits. In deep-submicron processes a significant portion of the power budget is lost in standby power due to increasing leakage. The identification and calculation of different leakage currents are very important in designing low power Nano Cmos Digital circuits.There have been many works on subthreshold leakage and techniques to reduce it, such as controlling the input vector to the circuit in standby mode, forcing stack and body bias control. In this tutorial paper we review the leakage current power loss, various transistor intrinsic leakage phenomenon, with contention current and reduction techniques of standby power, further analyzes the different components of standby power dissipation and highlights the significance of the same.
Finally, the paper describes different circuit techniques to reduce the leakage power consumption.

Keywords - Leakage Current, Subthreshold Leakage Current, Gate Tunneling Leakage Current, Contention Current, Low power design, Digital CMOS Circuit.

I. Introduction

With the continuous scaling of CMOS devices, leakage current is becoming a major contribution to the total power consumption. In current deep-submicrometer devices with threshold voltages, subthreshold and gate leakage have become dominant sources of leakage [1, 2]. One of the most challenging aspects of today's CMOS VLSI circuits is standby power dissipation. Feature size reduction has made the effects of leakage currents more pronounced. This becomes more complicated in sub 100nm technologies with not only subthreshold leakage but also with the gate oxide [3, 6].

Device dimensions are scaled down with each technology generation to increase the density and performance. With scaling of device dimensions, the supply voltage must be scaled down to keep power consumption low[7]. The speed of the circuit decreases if the ratio V_{dd}/V_{th} is less than five because the current driving capability decreases. Hence the transistor threshold voltage (V_{th}) has to be commensurately scaled to maintain a high drive current and achieve performance improvement. The scaling of threshold voltages results in an exponential increase in subthreshold current. However, threshold voltage scaling results in a significant amount of leakage power dissipation due to an exponential increase in the subthreshold leakage current conduction [8]. Borkar in [9] predicts a 7.5-fold increase in the leakage current and a five-fold increase in total energy dissipation for every new microprocessor chip generation. In order to maintain reasonable short channel effects (SCE), the gate oxide thickness (T_{ox}) has to be scaled. However the gate tunneling current increases with scaling of T_{ox} [10], [11].

For a CMOS circuit the total power dissipation includes dynamic and static components during active mode of operation. It is given by [5]

$$P = C_L.V_{DD}^2.f + t_{sc}.V_{DD}.I_{peak}.f + V_{DD}.I_{leakage} \quad (1)$$

In standby mode, the power dissipation is due to standby leakage current ($V_{DD}.I_{leakage}$) and contention current in ratioed circuit. In nanometre technologies, nearly one-third of the power is leakage.For dynamic power dissipation of a CMOS circuit in active mode, there are two components .One is the switching power ($C_L.V_{DD}.f$) which is dissipated every time switching occurs due to charging and discharging of load capacitance. The other component is the short circuit power ($t_{sc}.\ V_{DD}.\ I_{peak}$) due to nonzero rise and fall time of input waveforms. The static power ($V_{DD}.I_{leakage}$) of a CMOS circuit in active mode is the power dissipation due to flow of leakage current when there is no switching activity in the circuit.

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Dynamic switching power accounts for majority of total power dissipation. Dynamic short circuit power accounts for a small portion of total power and is decreasing absolutely. Whereas leakage power accounts for a very small portion of total power dissipation and is increasing exponentially with scaling. The impact of standby power is increasing as dimensions are shrinking due to increase in leakage current.

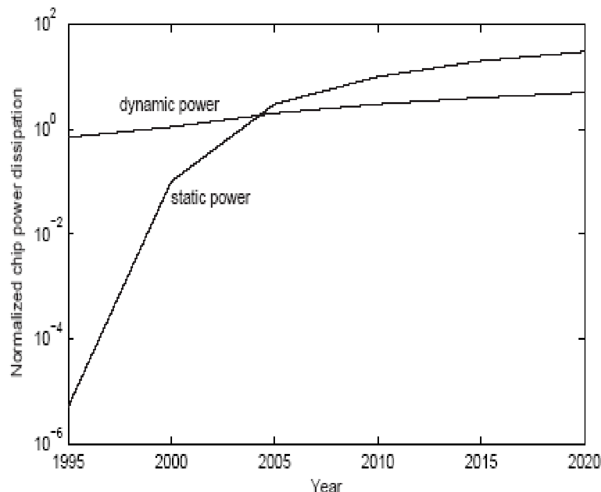

Fig.1 Leakage and active power trends according to ITRS roadmap.

As shown in Fig. 1, this impact is of more importance particularly for portable, low voltage systems and for systems that have long idle times punctuated by burst of activity.

This paper is organized as follows. In Section II, different leakage current components and mechanisms in nano cmos transistors are described, which is essential to model solutions for reducing standby power and static leakage. Section III explores different circuit techniques for leakage power control in nano-scale CMOS circuit. Finally the conclusion of the paper given in Section IV.

II. LEAKAGE CURRENT ANALYSIS

We describe six short-channel leakage mechanisms [4] as shown in Fig. 2 and contention current.

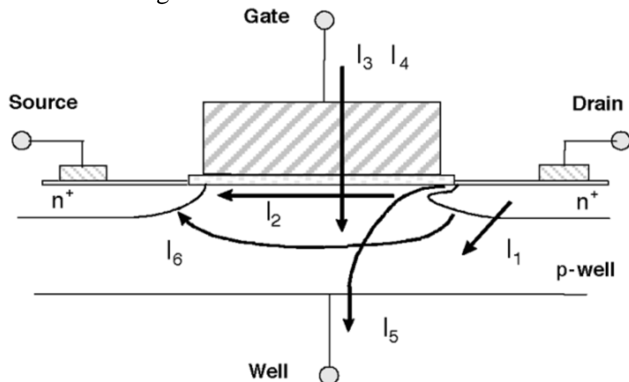

Fig.2 Leakage Current mechanism of nano transistors.

I_1 is the pn junction reverse-bias current; I_2 is the subthres -hold leakage; I_3 is the gate tunneling leakage; I_4 is the hot-carrier injection gate current; I_5 is the gate induced drain leakage (GIDL); and I_6 is the channel punchthrough current. Currents I_2, I_5 and I_6 are off-state leakage current, while I_2 and I_3 occur in both ON and OFF states.

A. *Pn Junction Reverse Bias Current*

P-n junction reverse bias leakage current flows across the reverse biased drain and source to well junctions. It consists of two main components: one is the minority carrier diffusion/drift near the junction and the other is due to electron-hole pair generation in the depletion region of the reverse biased p-n junction. As scaling of technology is done the doping is increased which increase the electric field across the depletion region of the reverse biased junction. When electric field is very high (>10^6 V/cm), the electrons from the valence band of the p region tunnel to conduction band of the n region and this leads to band to band tunneling. As shown in Fig.3 ,this current adds to leakage power. The tunneling occurs when the voltage drop across the channel is more than the band gap.

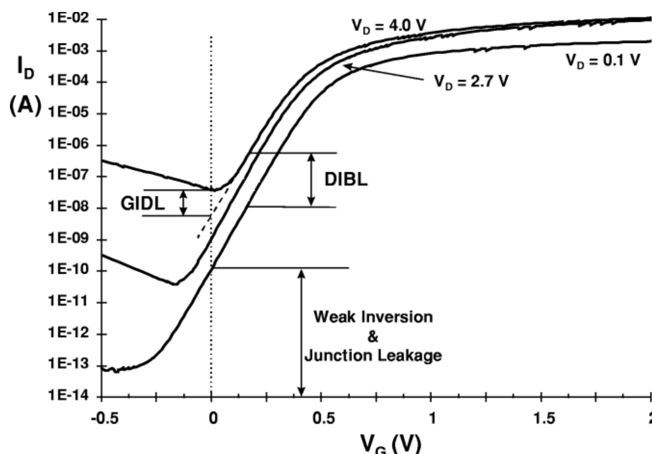

Fig.3 I_D vs. V_G for 3 values of V_D shows GIDL, DIBL, weak inversion and junction leakage.

B. *Subthreshold lekage*

The subthreshold current is the drain-source current of an OFF transistor when gate voltage Vg < Vth. This is due to the diffusion current of the minority carriers in the channel, for a MOS device operating in the weak inversion mode (i.e. the subthreshold region.) For instance, in the case of an inverter with a low input voltage, the NMOS is turned OFF and the output voltage is high. Even when V_{GS} is 0V, there is still a current flowing in the channel of the OFF NMOS transistor due to the V_{DD} potential of the V_{DS}. The magnitude of the subthreshold current is a function of the temperature, supply voltage, device size, and the process parameters, out of which, the threshold voltage V_{th} plays a dominant role.

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1) *Drain Induced Barrier Lowering:* In submicron technologies as device dimensions are scaled to achieve higher performance and density, the drain and source are moving closer to each other which affect threshold voltage. In a short-channel device, the source and drain depletion width in the vertical direction and the source and drain potential have a strong effect on the band bending over a significant portion of the device. Therefore the threshold voltage and hence the Subthreshold current of short channel devices vary with drain bias. DIBL occurs when the source barrier potential decreases due to the interaction of drain and source depletion regions with each other near the channel surface. When a drain voltage is applied to a short channel device, it lowers the source potential barrier height, resulting in further decrease of the threshold voltage and increases subthreshold leakage current.

2). *Body Effect:* The reverse biased source to well/substrate junction enhances the bulk depletion region and hence increases the threshold voltage required to make the channel

Inverted. The effect of body bias can be considered in the threshold voltage equation

$$V_{th} = V_{fb} + 2\varphi_B + \frac{\sqrt{2\varepsilon_{si} q_{Na}(2\varphi_B + V_{bs})}}{C_{ox}} \quad (2)$$

3). *Vth Rolloff:* With decrease in channel length, the drain and source depletion regions surrounding the drain and source is comparable to the distance between them. The depletion regions spread into the channel is comparable to the channel length itself hence channel is already depleted.

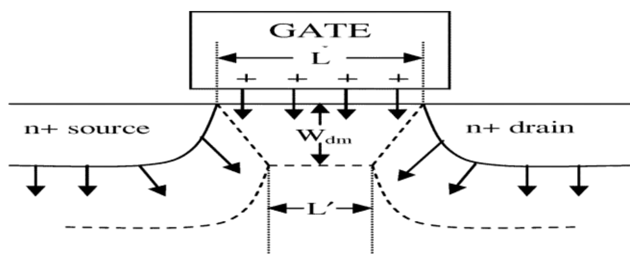

Fig. 4 Spreading of source/drain depletion regions

The gate voltage required to invert the bulk charge is lesser and hence the threshold voltage is reduced. Higher drain bias results in more spreading of depletion region and hence lesser threshold voltage and higher subthreshold current.

$$V_t = V_{fb} + \emptyset_{st} + \frac{Charge\ in\ Trapezoid}{C_{ox}} \quad (3)$$

Where V_{fb} is flatband voltage; $\emptyset_s$ is surface potential; c_{ox} is oxide capacitance.

C. Gate tunneling Leakage: The gate direct tunneling leakage flows from the gate through the "leaky" oxide insulation to the substrate. As scaling is done in submicron technologies, to counteract various short channel effects oxide thickness is reduces this results in development of a high electric field across the oxide, which increases gate tunneling leakage. In the very thin gate oxides (less than 3-4 nm),electrons from the inverted silicon surface tunnel directly through the forbidden energy gap of the oxide layer instead of tunneling through the conduction band of the oxide layer. Hence direct tunneling occurs when $V_{ox} < \Phi_{ox}$ where V_{ox} is the voltage drop across the oxide layer and Φ_{ox} is the Si-SiO2 interface barrier height for electrons.

Its magnitude increases exponentially with the decrease in gate oxide thickness t_{ox} and $V_{ox.}$ According to the 2001International Technology Roadmap for Semiconductors, high-K gate dielectric, is required to control this component of the leakage current for low standby power devices.

D. Hot Carrier Leakage: The mobile carriers in short channel devices acquire enough energy to cross interface potential and enter the oxide layer. The injection of electrons from Si to SiO_2 is more likely than holes, as the effective mass of holes is lesser than that of electrons and the barrier height of holes(4.5 eV) is more than that of electrons(3.1 eV).

E. Gate Induced Drain Leakage: When gate is biased in accumulation region, the silicon surface under the gate has the same potential as the substrate. The surface behaves like it is more heavily doped than the substrate region. This causes the depletion at the surface to be narrower and hence electric field develops mostly near the surface. When the negative bias at the gate is large (with drain at V_{DD}), it causes the n+ drain region under the gate to be depleted or even inverted. The possibility of tunneling via near surface taps also increases. This causes more field crowding and peak field increase resulting in high field effects such as avalanche multiplication. As a result of all these effects, minority carriers are emitted in the drain under the gate. As substrate is at lower bias the minority carriers in n+ drain depletion region below the gate are swept laterally into the substrate. Thinner oxide thickness and higher V_{DD} enhance the electric field and therefore increase GIDL.

F. Punchthrough: In short channel devices as the drain and source are closer to each other, the depletion regions at the drain–substrate and source-substrate junctions spread into a considerable length of the channel. If the drain bias in these short channel devices is increased further then it can lead to a point when the increase in drain bias lead to merging of the drain junction and source junction depletion regions. Punchthrough decreases the source substrate potential barrier and hence the majority carriers in the source flow to the substrate and some of them are reach the drain. This results in a subthreshold current and also increases the subthreshold slope.

G. Contention Current: Static CMOS circuits have no contention current. CMOS logic eventually replaced

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nMOS logic, however ratioed circuit are still useful in special application draw current even while quiescent. For example, pseudo-nMOS gates having contention between the nMOS pull downs and the always-on pMOS pullups when the output is 0. Current-mode logic and many analog circuits also draw static current. Such circuits should be turned OFF in sleep mode by disabling the pullups or current source.

III. LEAKAGE POWER REDUCTION TECHNIQUE

3.1 Leakage Reductions at Process Level

The substrate doping concentration should increase to decrease the depletion width proportionally. The principle of constant field scaling lies in scaling the device voltages and the device dimensions by the same factor, In addition to gate oxide thickness and junction scaling, another technique to improve short-channel characteristics is well engineering. By changing the doping profile in the channel region, the distribution of the electric field and potential contours can be changed. The goal is to optimize the channel profile to minimize the OFF-state leakage while maximizing the linear and saturated drive currents.

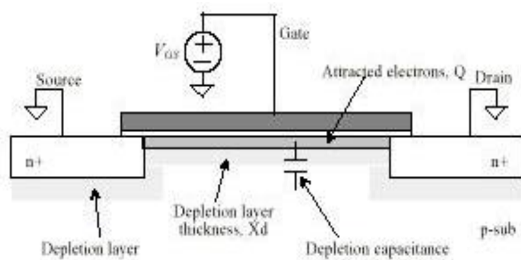

Fig-5 MOSFETs Graphical Representation

3.2 Leakage Reductions at Circuit Level

A. Power Gating: The most natural way of lowering the leakage power dissipation in the standby state is to turn off supply voltage to the sleeping transistors. This can be done by using one PMOS transistor and one NMOS transistor in series with the transistors of each logic block to create a virtual ground and a virtual power supply . In practice only one transistor is necessary. Because of their lower on-resistance, NMOS transistors are usually used.

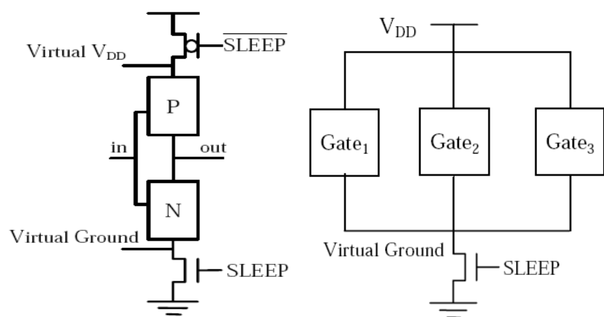

Fig-6 Power Gating Circuit

In the active state, the sleep transistor is on, the circuit functions as usual. In the standby state, the transistor is turned off, which disconnects the gate from the ground. To lower the leakage, the threshold voltage of the sleep transistor must be large and the width of the sleep transistor is smaller than the combined width of the transistors in the pull-down network.

B. Self reverse biasing

The body effect in CMOS transistors, a smaller width of the depletion layer leads to lower V_T. The reverse biasing of CMOS transistor increases V_T while on forward biasing of the CMOS transistor V_T decreases. Also in CMOS, threshold voltage increases with increased doping of the channel but decreases with applied bias. Therefore the current in the sub threshold region can be partially decreased by reverse biasing CMOS transistors in standby mode. Equation (6) quantifies the back-gate bias parameter as function of the oxide capacitance and substrate doping level [7].

$$\gamma = \frac{t_{ox} \cdot \sqrt{2 N_{SUB} q \epsilon_{Si}}}{\epsilon_{ox}} \quad (4)$$

Where t_{ox} is gate oxide thickness, N_{SUB} is substrate doping level q is unity electron charge ϵ_{ox} is gate oxide permittivity and ϵ_{Si} is Silicon permittivity.

C. Multiple V_{th} designs

Multiple-threshold CMOS is most popular technique for leakage power reduction which put high V_T and low V_T transistors on a same chip. The high-threshold transistors can partially decreased sub threshold leakage current, while the low-threshold transistors are used for high performance and Stability.

In MTCMOS circuit high threshold voltage sleep transistors are used to cut off the power supply and ground connection to an idle low threshold voltage circuit block as shown in fig . 6. In standby mode upper and lower transistors are cut off to lower the subthreshold leakage current in an idle circuit block, whereas in active mode these are activated to get normal circuit operation with high performance.

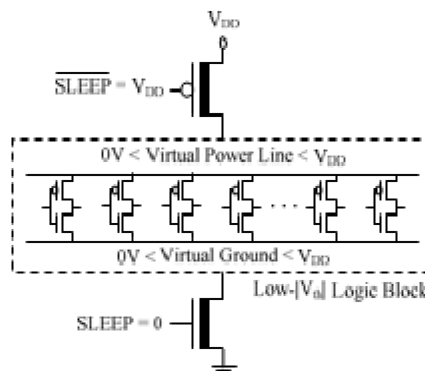

Fig-7 Power and ground gated MTCMOS circuit

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IV. STACK EFFECT

Subthreshold current depends exponentially on V_T, V_{DS} and V_{GS} [1]. Therefore it is a function of the terminal voltages, V_D,V_B,V_S and V_G. This means that to know subthreshold leakage of a device the biasing condition should be known or by controlling the terminal voltages the subthreshold leakage can be controlled.

From (1) for tunneling current it can be observed that tunneling current increases exponentially with a decrease in oxide thickness as well as V_{ox}. The latter depends on the biasing condition which is related to gate topology and input signal.

Therefore input pattern of each gate affects the subthreshold as well as gate leakage current. The leakage of transistors in a stack is a function of no. of transistors and input pattern.

Source biasing is the general term for several techniques that change the voltage at the source of a transistor. The goal is to reduce V_{GS}, which has the effect of exponentially reducing the subthreshold current. Another result of raising the source is that it also reduces V_{BS}, resulting in a slightly higher threshold voltage due to the body effect. Circuits that directly manipulate the source voltage are rare, and those that exist usually use switched source impedance or a self-reversed biasing technique

Probably the simplest example of source biasing occurs when “off” transistors are stacked in series. Conceptually, the source voltage of the upper transistor will be a little higher than the source voltage of the lower transistors in the stack. Hence V_{GS} of upper transistor is negative, V_{BS} is negative resulting in increase in threshold

2nm in the new generation technologies, both the leakages, gate leakage and subthreshold leakage have to be addressed together. The leakage currents are therefore analyzed considering their effects on the two leakage mechanisms.

Circuit level techniques incorporated requiring support from technology and process level techniques can be more effective in reducing leakage. There cannot be a single technique that will guarantee the best leakage power reduction. There are delay and area overheads and also the cost of minimum leakage vector application depends on the previous state of the circuit and time for which it will remain in standby mode. Hence the future work can be collaborating the circuit level techniques with technology dependent circuit level techniques and process level techniques.

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