Performance variations in Digital CMOS circuit technologies due to temperature

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***Abstract*— This paper identifies the device parameters that characterize the variation of MOSFET current due to temperature fluctuations on 180nm CMOS technology. Further, the effect of temperature variation on performance of CMOS digital circuits and optimization of device parameters for temperature variation insensitive performance of the circuit is also presented.**

***Keywords*— Zero temperature coefficient point (ZTC), crossover point, threshold voltage.**

I. INTRODUCTION

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Temperature fluctuations often vary system speed, power, and reliability by altering the threshold voltage and mobility in each device. The resulting changes in current can lead to self-heating and increased leakage current which in turn has a detrimental effect on performance and reliability of the system. Figure 1 shows the simulated transconductance characteristics of n-channel MOSFET, at the temperatures of 25 and 125 degrees, simulated on HSPICE version A-2008.03 in 180nm CMOS technology. It can be seen that the characteristics have a common intercept point known as zero-temperature coefficient (ZTC) point [6]. If transistor is biased to this point by a current source, then the gate-source voltage will not depend on temperature. It occurs when the transistor has mutual compensation of mobility and threshold voltage temperature effects.

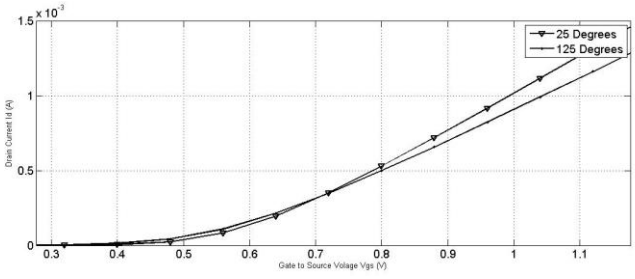

Figure 1 Drain current vs gate to Source Voltage of n-channel MOSFET with L=0.18u and W=5u

Section II identifies the various temperature dependent parameters of MOSFET. Section III details the effect of change in temperature on performance of digital CMOS circuits. Section IV concludes the entire paper.

II. TEMPERATURE DEPENDENT PARAMETERS OF MOSFET

A. Mobility

Phonon, Surface and coulomb are the three major scattering mechanisms that govern the characteristics of carrier mobility in the inversion layer of MOSFET with phonon scattering being the dominant at higher temperature. To describe the effect of mobility on temperature, a second order polynomial is used with U_a,U_b,U_c being linearly dependant on temperature [2][3].

$$\mu_{eff}(T)=U_0\left(\frac{T}{T_0}\right)^{U_{te}}\left[\begin{matrix}1+\left\{\frac{V_{gsteff}+2V_t(T)}{T_{ox}}\right\}^2.U_b(T)+(U_c(T).V_{bseff})+\\ U_a(T).\frac{V_{gsteff}+2V_t(T)}{T_{ox}}\end{matrix}\right]^{-2} \quad (1)$$

Here,

$$U_a(T)=U_a(T_0)+U_{a1}\left[\frac{T}{T_0}-1\right]$$

$$U_b(T)=U_b(T_0)+U_{b1}\left[\frac{T}{T_0}-1\right]$$

and

$$Uc(T)=U_c(T_0)+U_{c1}\left[\frac{T}{T_0}-1\right]$$

The values of U_o, U_a, U_{a1}, U_b, U_{b1}, U_c, U_{c1}, U_{te} can be extracted from measured I-V data. T is the device temperature in Kelvin, and T_{norm} is the temperature at which the parameters such as U_a, U_b, U_c are extracted. Figure 2 plots the effect of change in electron mobility as the function of gate to source voltage V_{gs}. It can be seen from the plot as the temperature is

increased, the mobility decreases.

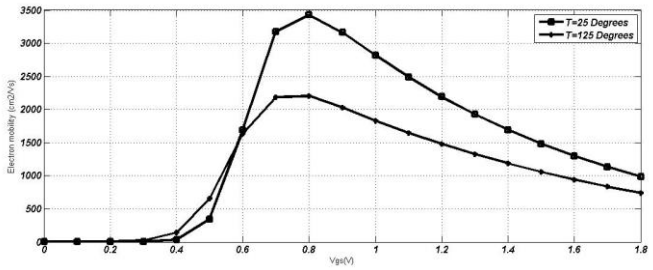

Figure 2 Electron Mobility Vs gate to source Voltage plot of n-channel MOSFET with L=0.18u and w=5u at 25 and 125 degrees

B. Threshold Voltage

Threshold Voltage is another important parameter that increases as temperature decreases due to the shift in Fermi level and bandgap energy. For long channel devices, threshold voltage depends linearly on temperature. BSIM3v3 uses following temperature model [2][3]:

$$\text{NMOS: } V_t(T)=V_t(T_0)+\left[KTI+\frac{KTIL}{L_{eff}}+V_{bseff}KT2\right]\left[\frac{T}{T_0}-1\right] \quad (2)$$

$$\text{PMOS: } V_t(T)=V_t(T_0)-\left[KTI+\frac{KTIL}{L_{eff}}+V_{bseff}KT2\right]\left[\frac{T}{T_0}-1\right] \quad (3)$$

Where $V_t(T_0)$ is the threshold voltage at room temperature. The parameters K_{T1}, K_{T1L} and K_{T2} are extracted from experiments. K_{TIL}/L is the minor term introduced to improve the fitting accuracy further. Figure 3 shows the plot of variation of threshold voltage with respect to temperature for n-channel MOSFET with l=0.18u and w=5u. It can be seen from the plot that the threshold voltage decreases almost linearly with increase in temperature.

As per equation (2) and (3), threshold voltage of MOSFET also depends on channel length, varying the channel length shifts the ZTC point of the MOSFET. Figure 4 shows the plot of variation of ZTC point voltage with respect to change in channel length. It can be seen from the plot that as the channel length is increased, the zero temperature coefficient point voltage decreases.

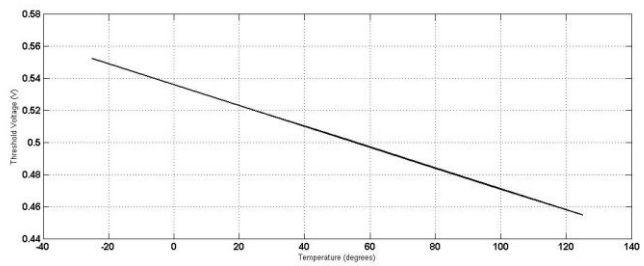

Figure 3 Threshold Voltage Vs Temperature plot of n-channel MOSFET with L=0.18u and W=5u

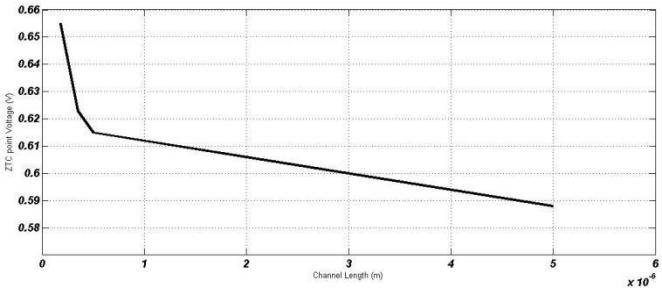

Figure 4 ZTC point Voltage Vs Channel Length variation of n-channel MOSFET with L=0.18u and W=5u

C. Saturation Velocity

Saturation Velocity V_{sat} is the weak function of temperature. BSIM3v3 uses following temperature model for temperature dependence of saturation velocity [2][3]:

$$V_{sat}(T)=V_{sat}(T_0)-AT\left[\frac{T}{T_0}-1\right] \quad (4)$$

Where A_T is the parameter extracted from data.

D. Parasitic Drain/Source Resistance

As the supply voltage reduces and MOSFET current becomes larger, drain/source series resistance becomes one of the most important parameter to describe the I-V characteristics accurately. The component of R_{ds} includes contact resistance, drain and source diffusion sheet resistance and the spreading resistance at the edge of the inversion layer due to current crowding. R_{ds} increases almost linearly with increasing temperature. The effect of temperature on R_{ds} is expressed as [2][3]:

$$R_{ds}(T)=\{R_{dsw}(T)[1+P_{rwg}V_{gsteff}+P_{rwb}(\sqrt{\phi_s-V_{bs}}-\sqrt{\phi_s})]\}\left[(10^6W_{eff})^{W_r}\right]^{-1} \quad (5)$$

and

$$R_{dsw}(T)=\{R_{dsw}(T_{norm})+P_{rt}\left[\frac{T}{T_{norm}}-1\right] \quad (6)$$

Where $R_{dsw}(T_{norm})$ is the resistance per unit width, $P_{rwg}V_{gsteff}$ is the dependence of gate bias on resistance $P_{rwb}(\sqrt{\phi_s-V_{bs}}-\sqrt{\phi_s})$ is the term that describes the effect of body bias on resistance. W_r is the fitting parameter to improve the accuracy. $P_{rt}\left[\frac{T}{T_{norm}}-1\right]$ describes the temperature dependence of resistance.

II. EFFECT OF TEMPERATURE DEPENDENCE ON CMOS CIRCUIT PERFORMANCE

The high-to-low and low-to-high propagation time for CMOS INVERTER gate can be expressed as[4][5]:

$$t_{phl} = \frac{2C_L V_{tn}}{k_n (V_{dd} - V_{tn})^2} + \frac{C_L}{k_n (V_{dd} - V_{tn})} \ln\left(\frac{1.5V_{dd} - 2V_{tn}}{0.5V_{dd}}\right) \quad (7)$$

$$t_{phl} = \frac{-2C_L V_{tp}}{k_n (V_{dd} + V_{tp})^2} + \frac{C_L}{k_n (V_{dd} + V_{tp})} \ln\left(\frac{1.5V_{dd} + 2V_{tp}}{0.5V_{dd}}\right) \quad (8)$$

Where

$$K_n = \mu_n C_{ox} \left(\frac{W}{L}\right)_n, K_p = \mu_p C_{ox} \left(\frac{W}{L}\right)_p$$

Are the transconductance parameters for NMOS and PMOS respectively and C_L is the effective load capacitance of the CMOS inverter circuit. The propagation delay of the NOT gate is therefore defined as:

$$T = \frac{t_{phl} + t_{plh}}{2} \quad (9)$$

Equation (7), (8) and (9) contains the temperature dependent MOSFET parameters threshold voltage V_t and mobility μ. As temperature increases, both mobility and the threshold voltage will decrease. In the case of supply voltage Vdd much larger than threshold voltage V_t, the thermal effect on the propagation delay will be dominated by the mobility [7][8].
Ring oscillator provides an efficient and highly accurate temperature measurement by exhibiting a linear dependence of oscillation frequency on junction temperature. As mentioned above, the delay of any CMOS circuit depends on the temperature and hence it is expected that the delay of a ring oscillator and hence its frequency will change as we vary the temperature. Therefore, at any specific temperature, the oscillator will exhibit a fixed frequency of oscillation [9].

III. CONCLUSIONS

Propagation delay variation with respect to temperature has been investigated in this paper. MOSFET device parameters that cause variation in drain current are also identified. Following points are concluded:

- As the temperature is increased, the drain current of n-channel MOSFET decreases at a fixed gate to source bias applied. There is a zero temperature coefficient point where the drain current becomes independent of gate to source voltage. Before the ZTC point, the drain current exhibits opposite behaviour i.e. it increases as the temperature is increased at a fixed gate to source bias applied.
- As the length of the channel is increased, the value of the ZTC point voltage decreases i.e. the value of the gate to source voltage for which the drain current becomes independent of temperature decreases as the length of the channel is increased.
- The mobility of the electrons and the threshold voltage of n-channel MOSFET decrease as the temperature increases.
- The frequency of the CMOS digital circuit decreases as the temperature is increased at a fixed supply voltage V_{dd}. There is a crossover point where the frequency becomes independent of temperature i.e. there is a supply voltage at which the frequency of the circuit or the speed becomes temperature independent. Before the crossover point, the frequency exhibits opposite behaviour i.e. it increases as the temperature is increased.

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