Priority based FIFO Network on-Chip Design

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***Abstract*-- The growing complexity in consumer products are designed with Multi-Processor Systems-On-Chip (MPSoCs), consist of complex integrated components communicating with each other at very high-speed rates. communication necessities of MPSoCs made of hundreds of cores will not be feasible using a single shared bus or a hierarchy of buses due to their poor scalability with system size, their shared bandwidth information between all the connected cores and the energy efficiency requirements of final products. To resolve these problem of scalability and complexity, Adaptive Priority based Networks-On-Chip (NoCs) have been proposed as a promising replacement to eliminate many of the overheads of buses and MPSoCs connected by means of general-purpose communication architectures. Network On-Chip (NoC) is the communication centric solution for integrating numerous on-chip components and the performance of NoC depending on context switching, CPU efficiency, and response time. The adaptive priority scheduler designed based on input FIFO usage and previous history information and this approach improves the throughput performance, reduce the data loss and low latency. This model is simulated on network simulator (NS2) and the throughput performance measured and compared with the round robin scheduling and priority based scheduling techniques.**

***Keywords*--** Network On-Chip (NoC); Adaptive Priority based scheduling; Multi-Processor Systems-On-Chip (MPSoCs); context switching.

I. INTRODUCTION

Design space exploration place a major problem in the System-on-Chip (SOCs), however, different functionality of the multiple SOC cannot be implemented in the single chip. As number of components on a system-on-chip increases the performance and the throughput decreases. NOC architecture plays a major role in the performance and energy consumption of the overall system. NOC integrating the various on-chip components. NOC bring a networking method to on-chip communications. Improve the QOS performance for the hard real time environment. A network switch is a Computer networking device that is used to connect many devices together on a computer network. Switch will send message to the device that needs or requests it. It has ability to route a packet.

(A) NOC Switch

NOC switch perform the circuit switching with lossless data transmission. The challenging task of network-on-chip to design an on-chip switch/router to dynamically support (hard) guaranteed throughput under very tight on-chip constraints of power, timing, area, and time-to-market. The existing model uses circuit-switched switch for NOC design. The circuit-switched switch, [1] based on a backtracking scheme, operates with a source-synchronous wave-pipeline approach. The switch will support a dynamic path-setup scheme and can achieve high bandwidth and high area and energy efficiency.

(B) Round Robin scheduling

It uses the round robin scheduling [3] for transmission control of each port. Maximum control overhead due to repeatedly searching the same path. Average waiting time increases when number of port increases. Lesser data transmission, higher amount of data cannot be set at a time it is used in short message data transfer. NOC switch such as circuit switching [2] cannot be performed well in the Multiprocessor switching mechanism. To improve the reliability and throughput performance the adaptive priority based algorithm is implemented in the NOC. Multi-processor system on-chip cannot work will in NOC [4], it causes errors, delay during the transmission. The performance of NOC on high through multimedia applications is influenced by context switching, CPU efficiency, and response time. Two or more sources ports are requested for the same destination port at that time performance and throughput is reduced in the round robin scheduling. To overcome this problems of scalable and

complexity Adaptive Priority based algorithm on Networks-On-Chip (NOCs) have been proposed.

(C) Adaptive priority based scheme

The adaptive priority scheduler designed based on input FIFO usage and previous history information, improves the throughput performance, reduce the data loss and low latency. NOC reduces context switching time, response time. The CPU efficiency increases. Average waiting time decreases when number of port is increases. It performs high speed in multimedia applications.

II. NETWORK ON CHIP

Network on chip is the switching network to interconnect the various IP modules in SOC's. NOC implemented different routing and arbitration strategies as well as the different organization communication infrastructure. Network on chip approach emerged recently as a promising alterna-tive to classical bus-based and point-to-point communication architectures.

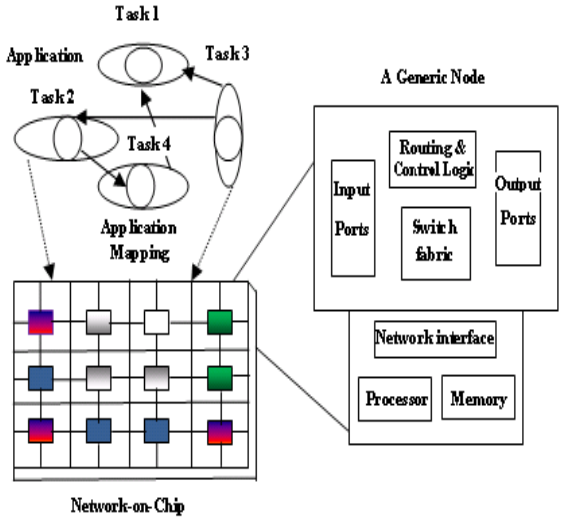


Figure 1: NOC Architecture

As shown in figure1 NoC enables communication between various processing elements (PEs)such as gen-eral or special purpose processors, embedded memories, application specific components, mixed-signal I/O cores, to happen via exchanging messages over the network. The actual traffic through the NoC depends on how applications are partitioned and mapped onto the PEs. The various features of NOC is (1) It is operating at a high speed (2) It has less hardware overhead (3) Best effort and guaranteed services (4) Effective use of network resources.

III. SYSTEM ARCHITECTURE

Network-on-Chip (NOC) switch is a general purpose on-chip communication concept that offers high performance to deal with complexity of modern systems. The three major components of network on chip architecture are switch, network interface.

(A) Architecture of NOC switch

Switch is used in NOC when number of input port is request for same output port. When all input port are request for same output port. The adaptive priority based arbiter is assigning priority based on the previous history information and buffer filling. It sends the higher priority port to execute the service. Fig 5.1 shows the NOC switch architecture. The Output signal generated by arbiter is reading external clock, three bit select lines for crossbar switch to select output channel. External clock signals which are indication for next connecting router that data is now available on output port of source router. The signal is high means data is now available on output port of that router. Read signal considering the current status of signal of that port only. Read signal is high only when FIFO empty. The Signal is low means buffer is not empty , some data is store in Arbiter generates three bit select lines to select output channel for outputting data out of router. Steps follow to generate three bit select lines to properly route in coming packet out of router given as below.

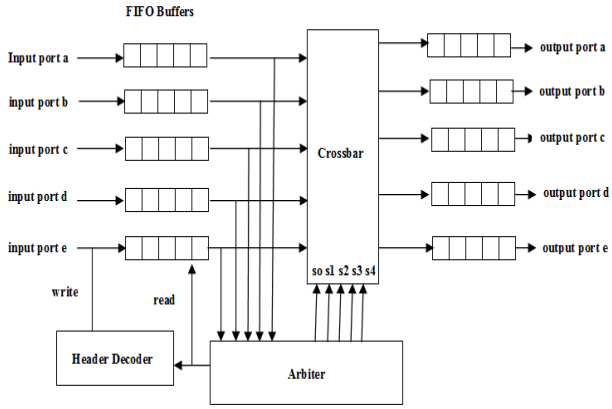


Figure 2: Architecture of NOC switch

First compare three bit destination address to select output channel for dataflow out of router. Next three bit are source address indicate the input channel from where packet is transmitted. As the area and speed on a single chip now faces the big challenge on a single chip, more and more processing elements now are placed on System on chip. Network-on-chip (NOC) is on a chip becomes a primary factor which limits the performance and power consumption. As the switch speed of crossbar switch increases rapidly, on faces the big problem, proposed a new method for on chip communication to solve the problem that challenges the system on chip. The physical interconnection resolve is to implement a fast and fairness arbiter to maximize the switch throughput and timing performance for Network-on-chips.

NOC has advantages on architecture, performance, reusability and scalability than traditional bus-based system-on-chip. The arbitration should guarantee the fairness in scheduling, avoid starvation, packet congestion and provide high throughput. The NOCs switches should provide high speed and cost-effective contention resolution scheme when multiple packets from different input ports compete for the same output port. An arbiter provide high performance NOC switches. For the above reasons, the analyses of the performance of the arbiters are significantly meaningfulness in the design of Network-on-chips.

IV. ADAPTIVE PRIORITY BASED ALGORITHM

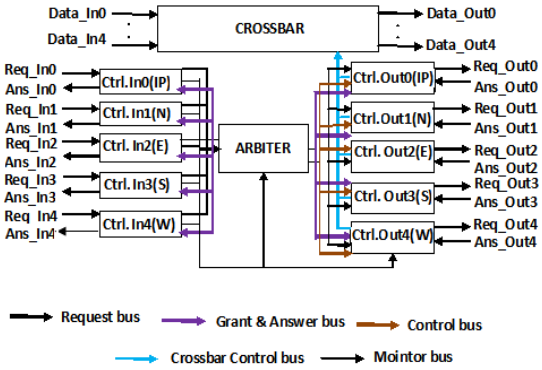
The Arbiter schedules the transmission priority using adaptive priority scheduling method. The adaptive priority scheduling works based on FIFO usage, previous transmission history, and last two sec transmission status of the ports. This method checks the FIFO usage is higher than ¼th input FIFO size then it consider the previous transmission history and last two seconds transmission status then assign the priority for transmission otherwise this check FIFO usage and last two seconds transmission status to assign the priority for transmission order.

Algorithm

Read FIFO usage
Read Port usage history
Check FIFO usage for all port
If all port FIFO usage more than ¼th of
FIFO size
Sort port usage throughput for last 30 sec
Assign priority on sorting order
If check last two second usage status of port
Swap the priority ascending to the best way of port
End
Else Swap FIFO usage based on previous priority
Sort port usage throughput for last 30 sec
Assign Priority based on sort
For each port
FIFO usage more than 1\4 of FIFO &&
Not used before
Swap priority
End
End

V. NOC IMPLEMENTATION MODEL

NOC modules are implemented in the FPGA via VHDL code and simulated in the model sim. With the help of Ethernet controller transfer the data from one port to another. NoC Switch is implemented in FPGA and Serial-to-Ethernet (S2E) (serial to parallel converter). An FPGA is a reconfigurable gate array logic circuitry the internal circuitry is connected in a way that creates a hardware implementation of the software application. SPARTAN III family is implemented in FPGA to design the NOC switch module. Ethernet controller is based on the TEXAS microcontroller, a highly integrated ARM® Cortex TM –M3, 10/100 Ethernet MAC and PHY, 50-MHz performance, and ample single cycle on chip Flash and SRAM memory for efficient network traffic handling. The S2E modules such as one 10/100 Ethernet port, two serial ports and 10-bit,3-channel ADC with flexibility that includes both RS-232 and CMOS/TTL level signaling, flow control, and hardware support for both synchronous and asynchronous serial communication. The most common application for the S2E module is for augmenting legacy products that contain a serial port for a configuration or control interface. Simply installing a S2E module into the legacy serial device provides instant networking capability with no major board redesign or software changes, a tiny form-factor for unobtrusive implementation, and cable lengths much longer than what is available for simple serial connections.



CONTROL INPUT

The Ctrl Ins is processing the incoming probe headers from upstream switches. When an incoming probe header arrives at an input, the corresponding Ctrl In monitors the output status through Monitor bus and requests ARBITER to grant it access to the desired Ctrl Out through the internal Request bus. Based on output status or the feedback from ARBITER placed in Grant & Answer bus, the Ctrl In operates appropriately and replies to the upstream switch through its Ans In.

CONTROL OUTPUT

The Ctrl Outs based on the command from the ARBITER placed in the Control bus, make requests to the downstream switches and control the CROSSBAR. The Ctrl Out handles the CROSSBAR to establish a direct connection from the Data In to the target Data out.

CROSS BAR

Data Path includes crossbar with internal transceivers to support direct-forwarding (wave-pipelining) of the source-synchronous data. The crossbar has two functions, providing connection for probe headers in the setup phase and with internal transceivers as direct-forwarding

pipelined data in the transmission phase, under the control of Ctrl Outs.

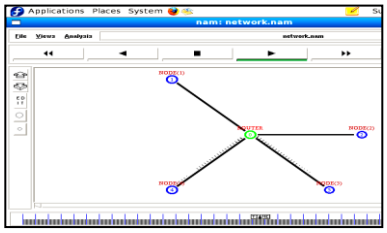
ARBITER

The arbiter traps the source and destination address from the output buffer and generate the control signal so that input data from source side sending to the output port. Arbiter controls the arbitration of the ports and resolve contention problem. It maintains the status of all the ports and knows which ports are free and which ports are communicating with each other. Packets with the equal priority and destined for the same output port are scheduled based on algorithm. The arbiter will release the output port which is connected to the crossbar once the last packet has finished transmission.

VI. SIMULATION

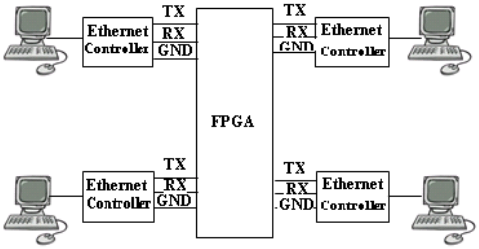
The Network on chip is implemented in the NS2 (Network simulator) ,the behavior of a network either by calculating the interaction between the different network entities (hosts/packets) using mathematical formulas.

The NoC switch module such as adaptive priority algorithm, FIFO, UART is simulated in the Ns2.



VI. REAL TIME IMPLEMENTATION

Real time network on chip is used for the implementation of the T-CREAT NOC. It is based on the MANGO and A Ethereal NOC's. The T-CREST aims is to developing a multi-processor
platform for real-time systems where all components (processors, interconnection network, compiler etc.) are designed with a focus on time-predictability. NOC is implemented in circuit switching to perform a telephone to voice over IP gateway and mail transfer application via internet. It gives higher bandwidth, latency when used in a hard real time system with scheduling of the traffic.



VII. CONCLUSION

The concept of Network on Chip switch is proposed, which is reducing the data loss and low latency. The adaptively priority scheduler designed based on input FIFO usage and previous history information to avoid congestion problem and improve the throughput performance. Study of throughput performance measured and compared with the round robin scheduling and priority based scheduling is simulated on network simulator (NS2).

IX. FUTURE WORK

Future work proposes the FPGA implementation and NOC switch design and NOC is implemented in the global interconnecting network for solving complex problem in the networking. Future work implementing the other modules such as algorithm, crossbar in hardware part. Comparing the round robin scheduling and priority based scheduling to measure the throughput performance.

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