

## PLL-AIDED FAULT DETECTION AND FAULT CURRENT LIMITERS FOR FAST PROTECTION OF POWER SYSTEMS

Yepuru Swathi<sup>1</sup>, ch.rajeshkumar<sup>2</sup>

<sup>1</sup>Department of electrical and electronics engineering, Narayana Engineering College, Nellore,Ap,India.

<sup>2</sup>Asst.proffesor Department of electrical and electronics engineering, Narayana Engineering College, Nellore,Ap,India.

<sup>1</sup>[swathiyepuru@gmail.com](mailto:swathiyepuru@gmail.com)

**Abstract-** In this paper, a new method is proposed that can be used to discriminate faults from switching transients. The method is primarily intended for use in systems where fast fault detection and fast fault clearing before the first peak of the fault current are required. An industrial system, in which high short-circuit power is desired but in which high short-circuit currents cannot be tolerated is an example of such a system. A phase-locked loop (PLL) is used to perform the discrimination. Computer simulations have been performed and it has been demonstrated that the output of the PLL is completely different for a fault compared to a switching transient. This difference can be used for discrimination between a fault and a switching transient.

**Keywords-** PV system, Wind power generation, Energy management, MPPT, DFIG, Grid control and its operation, Hybrid micro grid and power electronic converters.

### I.INTRODUCTION

High short-circuit power is often desired in an industrial system in order to connect and disconnect loads without causing disturbances to sensitive equipment or processes. With the high short-circuit power; a high fault current develops in case there are faults in the system. This high fault current has to be considered when designing the switchgear and other components that build up the power system. This is easily done in new installations but can be problematic when there is a need for higher short-circuit power in an existing system. In these cases, the installation of a fault current limiter could be an alternative to rebuilding the switchgear.

The installation of a fault current limiter can also provide the opportunity to make connections in the power system that otherwise would not be possible due to fault currents that exceed the rating of the switchgear. One of these examples is the paralleling of two transformers. If a fault current

limiter is installed as a sectionalizer between the two transformers, the system will experience the benefit of higher short-circuit power and in case of a fault in the system, the fault current limiter is operated and the system is sectionalized, thus reducing the fault current to levels which the system can handle. In, a trend toward increased short-circuit power is reported, which is also illustrated by an experience of more than 2800 installations of fault-current limiters throughout the world.

In this paper, the need for fast and reliable protection is discussed. Fault-current limiters are an essential building block in many systems as well as the need for fast and reliable fault detection. It is demonstrated that a phase-locked loop (PLL) can be used for power system protection purposes as an alternative to other methods. An investigation on how to use a PLL for the purpose of discriminating between a fault and a switching transient has been performed. Furthermore, the combination of protection relays and PLLs is discussed. It is proposed that the protection relay will detect the current transient and that the PLL will determine whether the current transient is caused by a fault or a switching transient. The protection relay and the PLL can consist of software implementations on a suitable hardware platform.

This paper is structured in the following way: First, a background on fault-current limiters and fault protection is given. This is followed by a description of the PLL and how the PLL can be used in a method to detect faults and discriminate between faults and switching transients. Then, a section with a case study is provided including computer simulations of the proposed method. Finally, there is a section with concluding remarks and proposal for future work. Furthermore, a short appendix describing some methods of estimating power system signals is added for convenience.

## II. MODELING OF CASE STUDY FAULT-CURRENT LIMITERS AND FAULT- CURRENT DIVERTERS

An apparent contradiction regarding the short-circuit power of a supply network is that whereas there are obvious advantages with a stronger network (less voltage dips, more and larger loads can be connected, less switching transients), there are also obvious disadvantages (high-fault currents in case of short-circuit faults in the system).

### A. Fault-Current Limiters:

One way of solving this contradiction is to use a fault-current limiter. A fault-current limiter is a device that during normal operating conditions allows a strong network but when a fault occurs, introduces enough impedance in the circuit so that the fault current is limited.

The purpose of a fault-current limiter is to limit the fault current so that its prospective peak value never is reached. The current limiting functionality can be achieved in several ways (e.g., current limiting reactors; fuses; triggered fuse; superconductive fault-current limiters; and fuses and power-electronic-based current limiters).

### B. Fault-Current Diverters:

Fault-current diverters can be used as an alternative to fault current limiters. A current diverter consists of a switch that is in open position under normal operating conditions. When a fault is detected, the switch closes and short circuits the phases of the power system to earth at a predetermined location. This predetermined location is preferably chosen as close to the source as possible. The fault current will still flow from the source through the current diverter to earth and will continue to do so until the main circuit breaker (CB) clears the fault current. The benefit of a fault-current diverter is that the load that is connected to the system does not see the full short-circuit current once the switch has been closed. Thus, for the load, the fault-current diverter provides a limitation of the fault current. A current diverter is an easy solution to provide fault-current limiting functionality in a power network. The network downstream the current diverter experiences only a small residual current once the fault current has been commutated to the earth path.

## III POWER SYSTEM PROTECTION

As concluded in the previous section, power system protection is another important issue. It is essential for safe operation of the power system that faults are detected and cleared automatically in a fast and reliable manner so that the operation of the power system is not disturbed. A typical fault protection

system is built from circuit breakers (CBs), protection relays, and primary transducers, such as voltage and current transformers and auxiliary equipment.

There are many methods and algorithms available to detect short-circuit current in a power system. One simple (but yet efficient) method is to estimate the current from measured current samples. If the magnitude of the estimated current is larger than a predetermined threshold it is assumed that a fault has occurred (magnitude relay). The estimation of the current can be performed using several different techniques, such as, for example, by calculating the root mean square (RMS) value by a fast Fourier transform (FFT) method or by a least-square (LSQ) method. The accuracy of the estimation and the amount of information that is available for the estimation are correlated. In general, if more information is available, the estimation will become more accurate. On the other hand, if faster fault detection is required, the estimation becomes less accurate since less information is available. In an earlier paper, fast fault detection has been defined to be in the range of 1–2 ms after fault inception.

This short detection time is needed for the fault-current limiters as mentioned in the previous section. Some methods that have been suggested for use in transmission systems have the potential of being fast. These methods could be based on traveling waves, neural networks, wavelet transforms, and fault-generated noise.

Although it is sometimes possible to adapt the mentioned techniques for fast fault detection in power distribution systems, new techniques have been explored. In the latter reference, a method for fast fault detection is described, which detects that a fault has occurred when five consecutive current samples are above a predefined threshold (i.e., the measured current samples are not fitted to a signal model). With proper signal processing (filtering), it was further demonstrated that it was possible to discriminate between a fault and common switching transients. In this paper, an alternative method to perform the discrimination is proposed.

Even though the detection of faults is the primary concern for fault protection devices (dependability), the ability to distinguish between a fault and a switching transient (security) is also important. Switching transients can, under certain circumstances, give rise to high currents, which are much larger in magnitude than normal load currents. In existing relay protection, capacitor energization and transformer energization have been detected by analyzing the measured current to find certain characteristics of the two types of current transients as described. A current transient caused by a

transformer energization typically contains a superimposed dc component and a superimposed second harmonic component. A current transient caused by a capacitor energization typically contains higher frequency harmonic components. The harmonic components in the measured current can be identified with Fourier-based methods, but that typically requires more time. For fast fault detection purposes, other methods have to be investigated. The method that is proposed in this paper uses a PLL for that purpose.

**IV PROPOSED METHOD**

In this section, the proposed method of using a PLL for discrimination between faults and switching transients will be described. First, a short description of the basics of a PLL is given.

Second, a well-known implementation of a PLL suitable for simulation purposes is described and the relevant signals that are used for the actual discrimination between a fault and a switching transient are identified. Third, the tuning of the parameters of the PLL implementation is discussed and suggestions for a first selection of parameters is given.

**A. Basics of a PLL:**

The PLL has been an important device in electronics and power system applications ever since the first implementation in the 1930s by de Bellescize, as mentioned. The first PLLs were analog devices but following the development in solid-state electronics and computer technology, the PLL has developed from an analog device via digital implementations to pure software implementations.

A PLL is a circuit that is used to synchronize an input signal with a reference signal (an output signal that is generated by the PLL) with respect to phase and frequency. The function of the PLL can be explained from the block diagram of a simple PLL, as shown in Fig. 1.

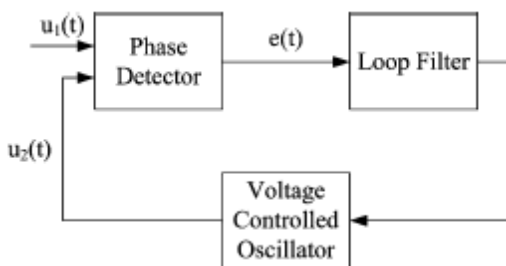


Fig.1. Block diagram of a PLL.

The input signal  $u_1(t)$  is compared with the reference signal  $u_2(t)$  in the phase detector (PD). The output of the phase detector is zero as long as the input signal and the output signal is equal in phase and frequency. If the phase or frequency of the input

signal changes, the output of the phase detector will deviate from zero. The error signal is passed through a low-pass filter (LF) and then to a voltage-controlled oscillator (VCO), which generates a reference signal (the output signal). If the error signal deviates from zero, the VCO will adjust the frequency of the reference signal so that the phase error becomes zero and the two signals are in phase. When the input signal is in phase with the reference signal, the PLL is in its locked state; hence the name phase locked. Recent research related to PLLs has been from several research fields: general descriptions of PLLs, distributed generation applications, active power-line conditioner applications, servo controllers, as well as protection and control.

**B. Description of a PLL that is Suitable for the Discrimination between a Fault and Switching Transient a:**

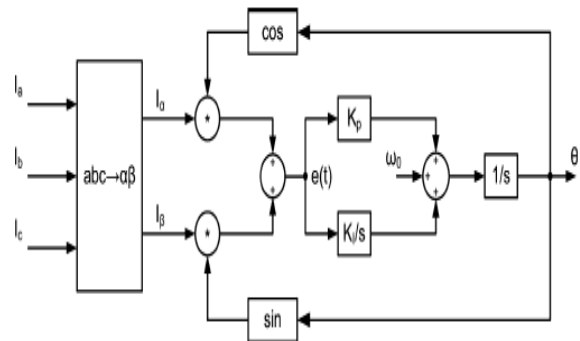


Fig.2. PLL implementation

A vector implementation, as shown in Fig. 2, of a PLL is described in this paragraph. Compared to the block diagram of Fig. 1, the error signal  $e(t)$  corresponds to the output of the PD, whereas the proportional-integral (PI) regulator and the integrator corresponds to the loop filter and the voltage-controlled oscillator (VCO). The inputs to the PLL are the three phase-currents ( $I_a, I_b, \text{ and } I_c$ ), which are first transformed to  $\alpha\beta$  quantities ( $I_\alpha, I_\beta$ ) using Clarke's transformation. Then, the  $\alpha\beta$  quantities are projected onto a reference frame. Depending on the proximity of the  $\alpha\beta$  quantities to the reference frame, an error signal is formed. This error signal is fed through a PI regulator so that the error is controlled to zero. Once the error is zero, the input signals are in phase with the reference frame. If it is assumed that the system is in steady state and that the power system is completely balanced, the phase currents can be written as

$$\begin{aligned}
 I_a &= I \cdot \sin(\omega t) \\
 I_b &= I \cdot \sin\left(\omega t - 2 * \frac{\pi}{3}\right) \\
 I_c &= I \cdot \sin\left(\omega t + 2 * \frac{\pi}{3}\right)
 \end{aligned}
 \tag{1}$$

Then, the Clarke's components  $I_\alpha$  and  $I_\beta$  equate to

$$\begin{aligned}
 I_\alpha &= \frac{(2 \cdot I_a - (I_b + I_c))}{3} = I \sin(\omega t) \\
 I_\beta &= \frac{(I_b - I_c)}{\sqrt{3}} = -I \cos(\omega t).
 \end{aligned}
 \tag{2}$$

Now, with reference to Fig. 2, the error signal is given by

$$e(t) = I_\alpha \cdot \cos(\theta) + I_\beta \cdot \sin(\theta) = I \sin(\omega t - \theta)
 \tag{3}$$

Thus, the error is zero exactly when the output angle of the PLL is in phase with the current of phase a. When a transient occurs in the system, the error signal will deviate from zero. Depending on the characteristics of the transient, the deviation will have different magnitude and frequency. Since a fault is typically an ac fundamental power frequency character, the deviation will be different than for a switching transient that contains non fundamental power frequency components. The behavior of the error signal of the PLL will also depend on the tuning of the PLL.

**C. Tuning of the PLL:**

The PLL will be tuned to the power system frequency. PLLs have been used for many years in HVDC transmission in order to synchronize the firing of the thyristors to the phase angle of the connected ac system. It is thus a well-known procedure and it is advisable to use parameters from such an installation as a starting point for the tuning. Fine-tuning of the parameters can then be made by, for example, computer simulations or any other standard tuning method.

**D. Fault Detection and Discrimination Using a PLL:**

The method that is used to detect a fault and discriminate the fault from a switching transient is described here. Two algorithms are executed in parallel. The first algorithm is based on the estimation of the magnitude of the current. If the estimated magnitude is higher than a preselected threshold, a flag is set.

The second algorithm is as previously mentioned, monitoring the error signal of a PLL. If this error

signal exceeds a preselected threshold, a second flag is set. If both flags are set, it is determined that a fault has occurred.

**V SIMULATION AND RESULT**

In order to test the proposed method, a simple test system has been developed and implemented in an Electromagnetic Transients Program(MATLAB/SIMULINK)

**Fault\_Pll case 1:**

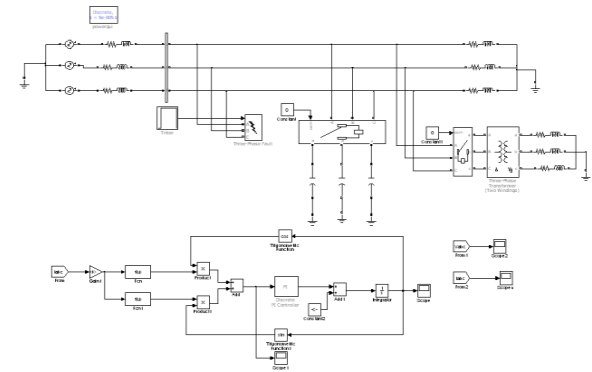


Fig.2. PLL implementation, MATLAB/SIMULINK test system.

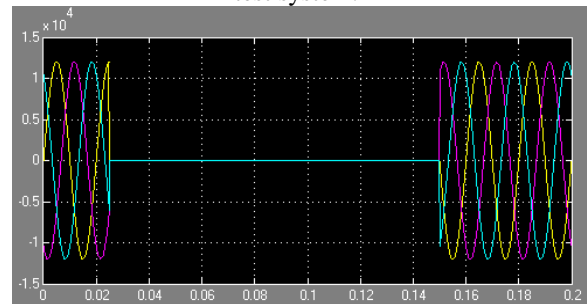


Fig.3. Three phase voltages  $V_{abc}$

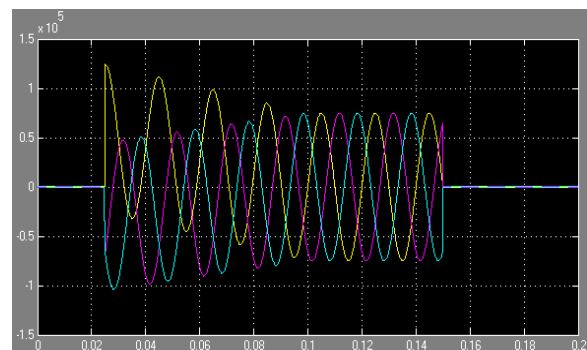


Fig.4. Three phase current  $I_{abc}$

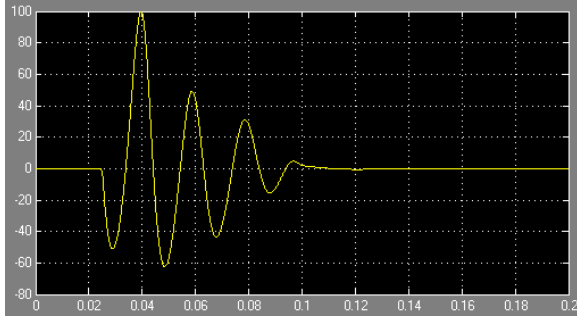


Fig.5. Error signal due to three phase fault

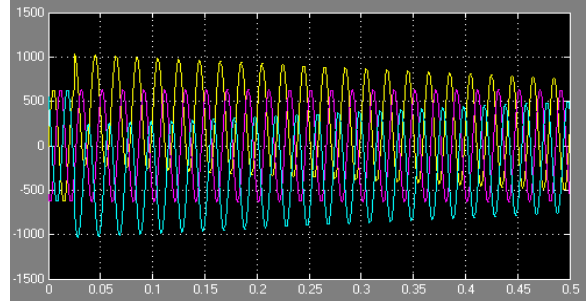


Fig.7. Phase currents due to transformer energization.

**Fault\_PII case 2:**

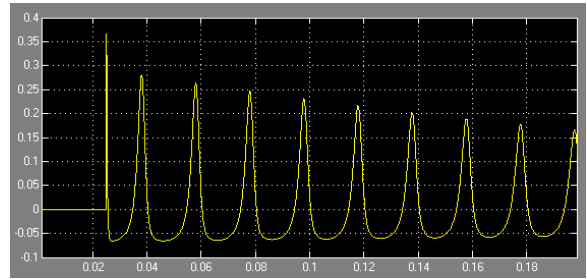
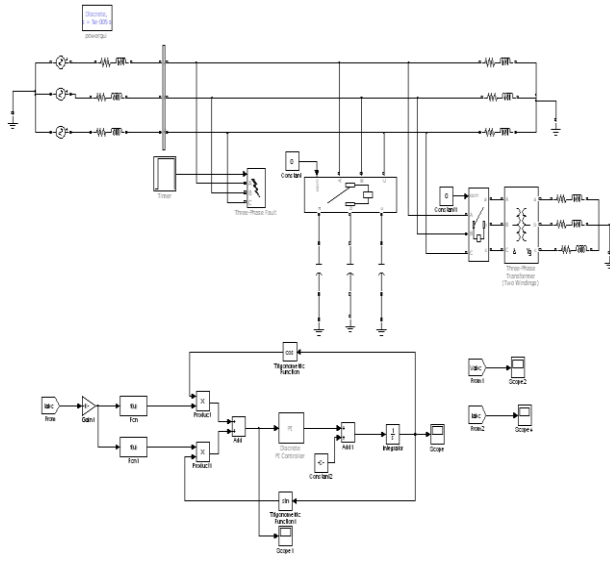


Fig.8. Error signal due to transformer energization

**Fault PII Case 1 Double Phase Fault**

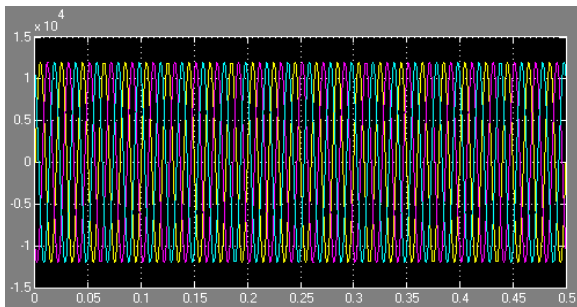
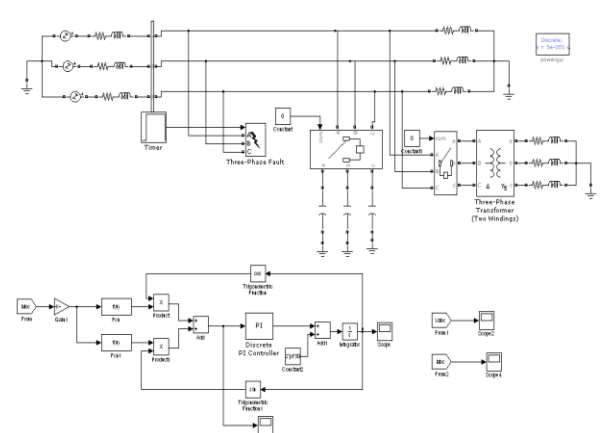


Fig.6. Phase voltages due to transformer energization

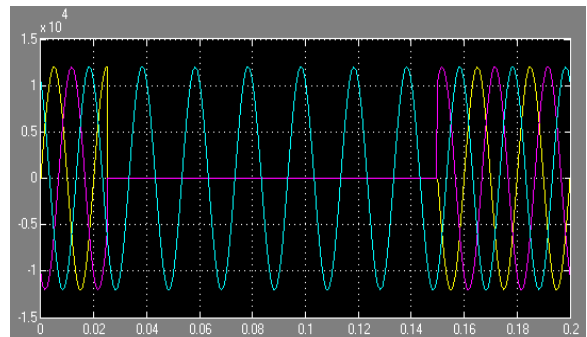


Fig.9.Phase voltages due to the phase to phase fault

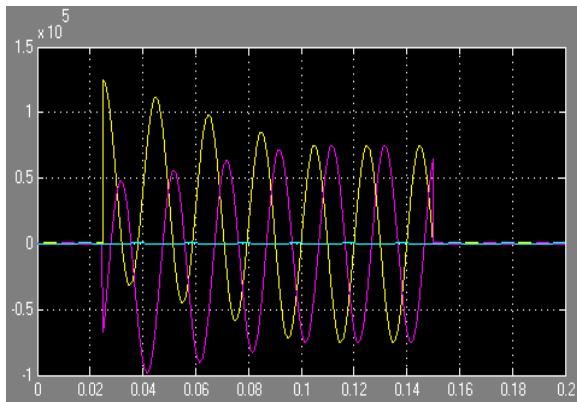


Fig.10.Phase currents due to the phase to phase fault

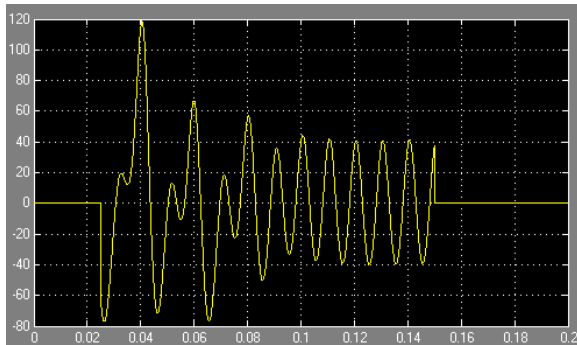


Fig.11. Error signal due to a phase to phase fault

**Fault PII Case3:**

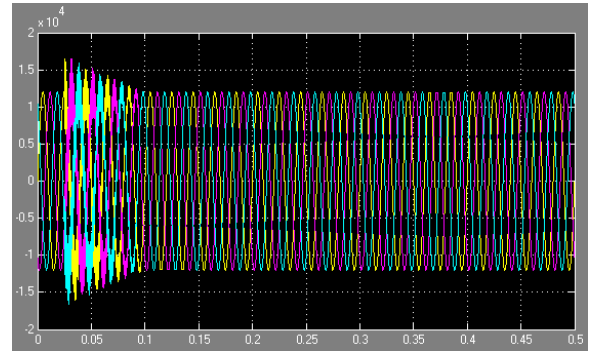
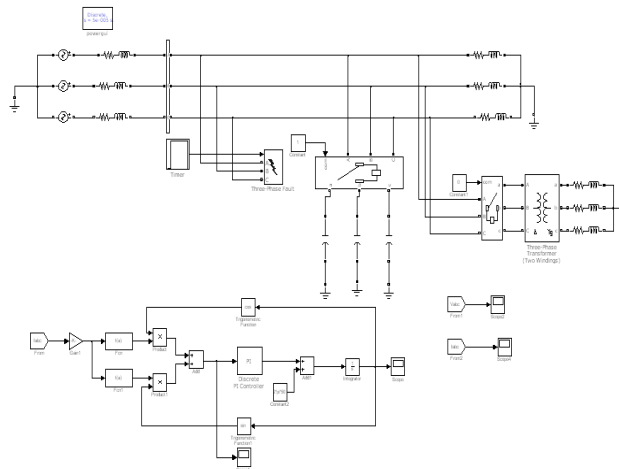


Fig.12.Phase voltages due to capacitor energization

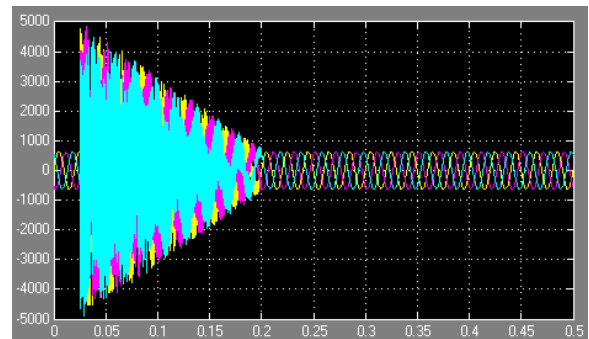


Fig.13.Phase currents due to capacitor energization

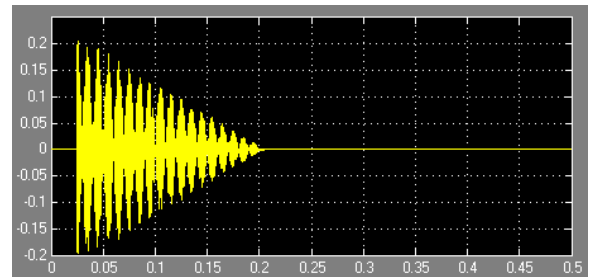


Fig. 14.Error signal due to capacitor energization

**VI.CONCLUSION**

In this paper, it has been demonstrated that a PLL can be used to determine whether a current transient is due to a fault in the system or due to a switching transient. Transformer and capacitor switching have been specifically studied due to the large occurrence of these switching transients in the power system. Simulations have been performed using a test system where faults and switching transients have been simulated. For all of these events, a large difference was observed in the error signal of the PLL when a fault or a switching transient was applied. This difference can be used to discriminate faults from switching transients.

The work presented in this paper is based on simulations and theoretical investigations. The focus has been on discrimination between switching transients and low impedance faults. For future work, high impedance faults must also be considered. Furthermore, the method could be tested in a real-time digital simulator with actual recordings of faults and switching transients and eventually implemented in a real protection system.

## REFERENCES

- [1] K.-H. Hartung and V. Schmidt, "Limitation of short circuit current by an is-limiter," in Proc. 10th Int. Conf. Electrical Power Quality and Utilisation, Sep. 2009, pp. 1–4.
- [2] CIGRE Working Group A3.10, Fault current limiters in electrical medium and high voltage systems, 2003.
- [3] A. Wright and P. Newbery, Electric Fuses, 3rd ed. London, U.K.: Inst. Elect. Eng., 2004.
- [4] M. Stemmler, C. Neumann, F. Merschel, U. Schwing, K.-H. Weck, M. Noe, F. Breuer, and S. Elschner, "Analysis of unsymmetrical faults in high voltage power systems with superconducting fault current limiters," IEEE Trans. Appl. Super conduct., vol. 17, no. 2, pp. 2347–2350, Jun. 2007.
- [5] K. Yasuda, A. Ichinose, A. Kimura, K. Inoue, H. Moiré, Y. Tokunaga, S. Torii, T. Yazawa, S. Hahakura, K. Shimohata, and H. Kubota, "Research and development of superconducting fault current limiter in Japan," IEEE Trans. Appl. Super conduct., vol. 15, no. 2, pp. 1978–1981, Jun. 2005.
- [6] H.-S. Choi, S.-H. Lim, and D.-C. Chung, "Discharge and current limiting characteristics of a superconducting fuse," IEEE Trans. Appl. Super conduct., vol. 15, no. 2, pp. 2360–2363, Jun. 2005.
- [7] W. Fei, Y. Zhang, and Q. Wang, in A Novel Bridge Type FCL Based on Single Controllable Switch, Bangkok, Thailand, 2007, pp. 113–16.
- [8] M. Komatsu, N. Ide, and S. Yanabu, in Proc. solid-State Current Limiting Switch for Application of Large-Scale Space Power Systems Conf., Orlando, FL, 2007, pp. 1471–6.
- [9] F. Huang and F. Flett, in Proc. IGBT Fault Protection Based on di/dt Feedback Control, Orlando, FL, 2007, pp. 1478–1484.
- [10] W. Fei, Y. Zhang, and Z. Meng, in Proc. Novel Single Self-Turn-off-Device Based FCL for Three-Phase Power Systems Conf., Taipei, Taiwan, 2007, pp. 1369–73.
- [11] Arceliminator, Rapid elimination of Internal Arcing. ABB, 1999. [Online]. Available: <http://www.abb.com>

- [12] R. Garzon, in Arc Terminator an Alternative to Arc-Proofing, Toronto, ON, Canada, 2001, pp. 185–9.

## AUTHOR DETAILS



Yepuru Swathi received the B.Tech degree from Audisankara College of Engg & Tech, Gudur, Nellore(dt). Present she is perceive M.Tech from Narayana Engineering College, Nellore.



Tirupathi.

ch.rajeshkumar received the Master degree in electrical power engineering from Anna university Chennai, B.Tech degree from sri vidyanikethan engineering college Affiliated to Jntu ananthapur .Rangampet