A New Structure for 0.18µm CMOS Squarer And Transresistance Analog Multiplier

Milad Kaboli
Islamic Azad University, Omidiyeh Branch, Omidiyeh, iran
kaboli.m@iauo.ac.ir

ABSTRACT

A new CMOS low-voltage current-mode four-quadrant analog multiplier was presented based on a squarer circuit with voltage output. The proposed circuit was composed of a pair of current subtractors, a pair of differential-input V-I converters and a pair of voltage squarer. The circuit was simulated using an HSPICE simulator at standard 0.18 µm CMOS level 49 MOSIS (BSIM3 V3.2 SPICE-based) and L-EDIT software. Simulation results showed performance of the proposed circuit and experimental results were given to confirm the operation. This topology of multiplier resulted in high frequency capability with low power consumption.
The multiplier operated at power supply of ±1.2V. The simulation results of analog multiplier demonstrated THD of 0.068% at 10 MHz, a −3 dB bandwidth of 2 GHz and maximum power consumption of 6.1 mW.

INTRODUCTION

At present, battery-power systems require circuits which operate on low voltage supply and low power consumption. Thus, there are very high demands for analog circuits that can operate at low voltage supply. The analog multiplier circuit is one of the important building blocks in VLSI communication systems, which can be applied to frequency mixers, variable gain amplifiers, adaptive filters, phase-locked loops and many other signal processing circuits. Several low-voltage CMOS multipliers have been presented using CMOS transistors operated in the triode region [1-2] and saturation region [3]. Saturation region design has batter frequency response; so, this paper proposed the saturation region design.
The four-quadrant multiplier is a very important building block of analog signal processing system. It has many applications in automatic gain controlling, phase-locked loops, modulation, detection, frequency translation, square rooting of signals and neural networks. To implement the multipliers in IC technologies, the Gilbert cell is a popular structure in bipolar IC technologies due to its wide dynamic range and high frequency performance [4].
However, characteristics of MOS devices and bipolar devices are different; thus, MOS version of Gilbert cell [5-7] requires extra linearization circuits which degrade circuit performance. They have either high voltage (and/or power) supply requirements [6], poor linearity or low output (current) signal levels [7]. Recently, some four-quadrant multipliers suitable for low voltage operation have been developed in [8-9], but other features such as dynamic range and frequency performance are limited. In this paper, a new CMOS four-quadrant analog multiplier was proposed based on the squarer-algebraic identity in MOS saturation region. The multiplier resulted in the product of two continuous signals x and y, yielding an output z = Kxy, where K is a constant with a suitable dimension. In this paper, a low-power, high-speed four-quadrant analog multiplier circuit was presented in the current mode.

CIRCUIT DESCRIPTION

The principle of the proposed multiplier was based on the square-algebraic identity:

$$(I1 + I2)^2 - (I1 - I2)^2 = K\,V1\,V2 \qquad (1)$$

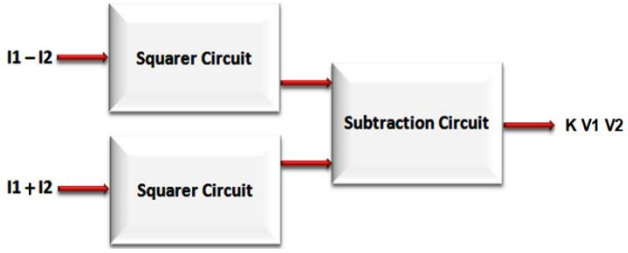


Fig. 1: Symbol of the proposed circuit

Therefore, the circuit needs two adder-subtractor circuits and two Squarer Circuits.

CURRENT ADDER-SUBTRACTOR CIRCUIT

The current adder-subtractor circuit is illustrated in Fig. 2, which consists of transistors M1 to M8. Current of the terminal-out followed the difference of currents of terminal-I1 and terminal-I2. Hence, terminal-out was named current output. The current of the terminal-out could be expressed as follows:

$$Id(m2) = I1 + Ibias \qquad (2)$$

$$Id(m3) = I2 + Ibias \quad (3)$$
$$Id(m2) = Id(m6) \quad (4)$$
$$Iout = Id(m8) - Id(m3) \quad (5)$$
$$Iout = (I1 + Ibias) - (I2 + Ibias) = I1 - I2 \quad (6)$$

By changing the direction of current I2, the circuit converted into a current adder in terminal-out.
The current source, Ibias forces equal currents of 56 µA in the transistors (M1–M4). Thus, the gate to source voltages of these transistors was equal, which made voltages of the two input terminals to be zero.

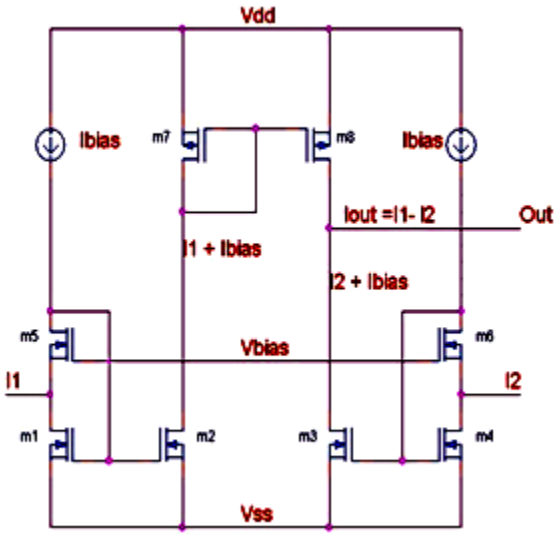


Fig. 2: Current subtractor circuit

SQUARER CIRCUIT

Considering the circuit in Fig. 3, while M1 and M2 worked in the saturation region:

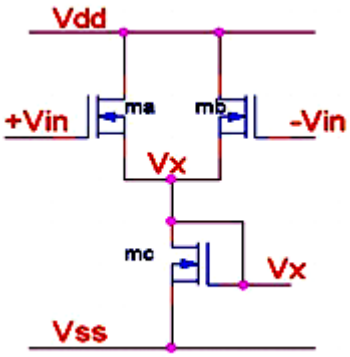


Fig. 3: Squarer

the currents through the transistors could be expressed as :

$$IDa = 0.5\,\mu n\,Cox\,W/L\,(VGS1 - VTn)^2 \quad (7)$$

$$IDb = 0.5\,\mu n\,Cox\,W/L\,(VGS2 - VTn)^2 \quad (8)$$

$$K = \mu n\,Cox\,W/L \quad (9)$$

$$VGS > VTn, VDS \geq VGS + VTn \quad (10)$$

where K is parameter of transistor, µn is electron mobility, Cox is gate oxide capacitance per unit area, W/L is transistor aspect ratio, VGS is gate-to-source voltage, VDS is drain-to-source voltage and VTn is threshold voltage of the MOS transistor. Supposing all the transistors as identical, then K1=K2=K and VTn1=VTn2=VTn and:

$$IDc = IDa + IDb \quad (11)$$

where IDc, IDb and IDa are drain currents of Mc, Mb and Ma, respectively.

$$IDc = \frac{K}{2}[(Vin - Vx - VTn)^2 + (-Vin - Vx - VTn)^2] \quad (12)$$

$$IDc = \frac{K[(Vin)^4 + 2(Vin)^2(Vss + 2VTn)^2 + (Vss + 2VTn)^4]}{4(Vss + 2VTn)^2} \quad (13)$$

For small signal of Vin, $Vin^4 \approx 0$ can be assumed.
Then, the output current can be expressed as the simple input signal squarer as follows:

$$IDc = \frac{K}{2}(Vin)^2 + \frac{K}{4}(Vss + 2VTn)^2 \quad (14)$$

The voltage at Vx can be derived from using a small signal model as :

$$VX = \frac{K}{2}gm(Vin)^2 + \frac{K}{4}gm(Vss + 2VTn)^2 \quad (15)$$

I to V Conventer

Fig. 4 is an I to V converter consisting of two MOSs with the same aspect ratio which operate in the saturation region.

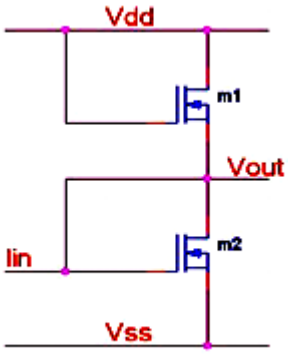


Fig. 4: I to V converter

$$ID1 = 0.5\,K\,(VDD - Vout - VTn)^2 \quad (16)$$

$$ID2 = 0.5\,K\,(Vout - VSS - VTn)^2 \quad (17)$$

$$(VDD - VTn) = -(VSS + VTn) \quad (18)$$

$$Iin = ID2 - ID1 \quad (19)$$

$$Iin = 2\,K\,Vout\,(VDD - VTn) \quad (20)$$

$$Vout = \frac{Iin}{2\,K\,(VDD - VTn)} \quad (21)$$

The Proposed Circuit

The proposed square circuit (shown in Fig. 5) included 14 NMOS transistors.

$$VG9 = \frac{-(Ix+Iy)}{2\,K\,(VDD - VTn)} \quad (22)$$

$$VG10 = \frac{(Ix+Iy)}{2\,K\,(VDD - VTn)} \quad (23)$$

$$VG12 = \frac{(Ix-Iy)}{2\,K\,(VDD - VTn)} \quad (24)$$

$$VG13 = \frac{-(Ix-Iy)}{2\,K\,(VDD - VTn)} \quad (25)$$

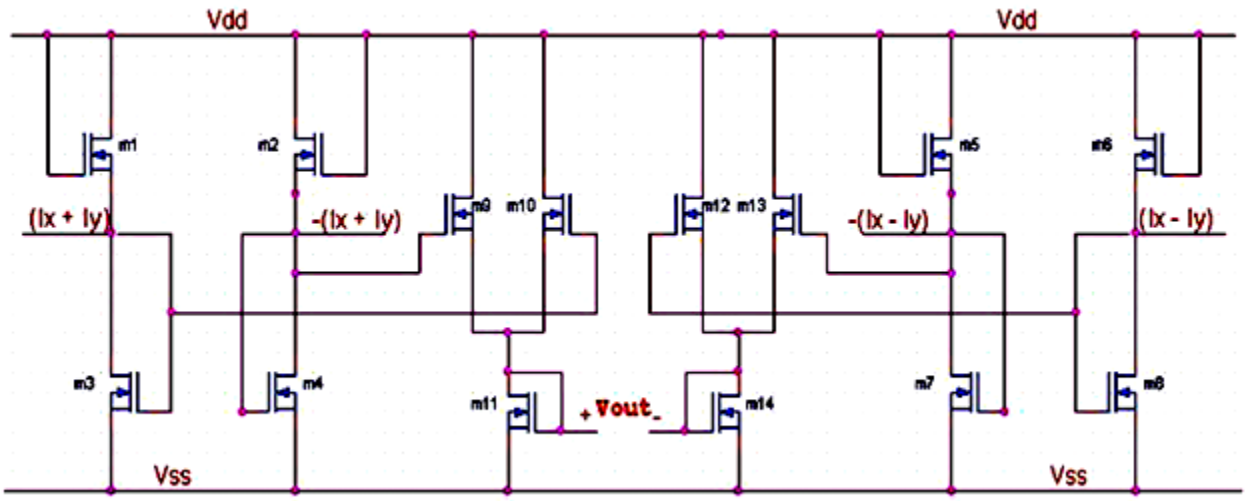
$$Vout+ = \frac{K}{2} gm\,(VG9 - VG10)^2 + Vc \quad (26)$$

$$Vout- = \frac{K}{2} gm\,(VG12 - VG13)^2 + Vc \quad (27)$$

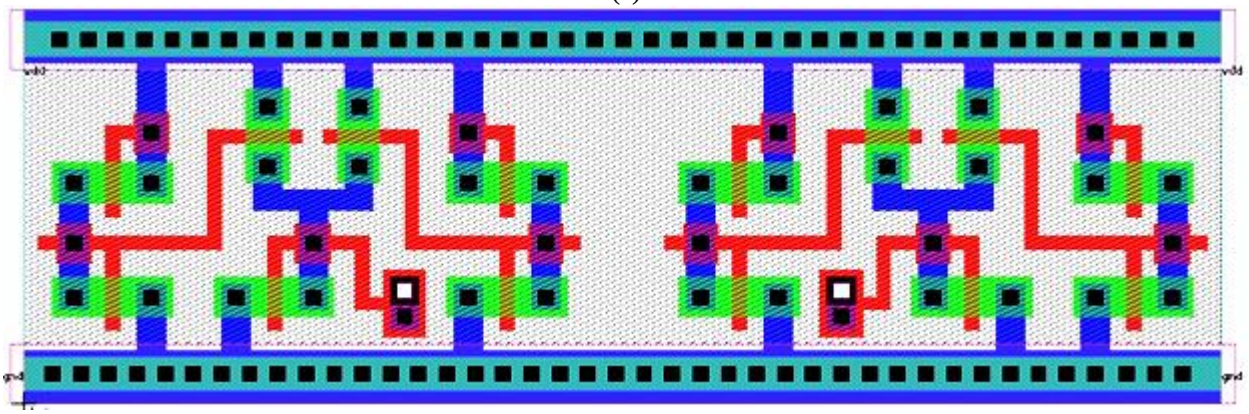
$$Vc = \frac{K}{4} gm\,(Vss + 2VTn)^2 \quad (28)$$

$$Vout = (Vout+) - (Vout-) \quad (29)$$

$$Vout = \frac{2\,gm}{K(VDD - VTn)^2}\,Ix\,Iy \quad (30)$$



(a)



(b)

Fig. 5: a. The proposed multiplier circuit, b. Layout of the proposed multiplier circuit

SIMULATION RESULTS

The complete circuit of the current multiplier can be seen in Fig. 5 and the simulation use 0.18µm CMOS and simulate with HSPICE level 49 MOS aspect ratio shown in Table 1.

Table 1. Aspect ratio of MOS transistor

MOS Transistor	W/L
M9-M14	10u/0.5u
M1-M8	0.5u/0.5u

Simulation result of the DC characteristic can be seen in Fig. 6. Input of Ix and Iy currents were -100µA to +100µA by Ix increase from -100µA to +100µA and Iy sweep from -100µA to +100µA in 5 (five) steps (as can be seen in Fig. 6).

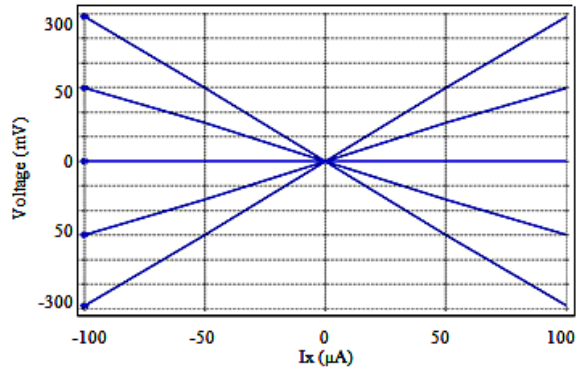


Fig. 6: Transfer characteristic curve of the multiplier

Fig. 7 shows the frequency response. Frequency increased from 100 kHz to 100 GHz. The simulation result demonstrated that -3dB of the frequency was about 2 GHz and offset of current sweep was from 5µA to 25µA in five steps.

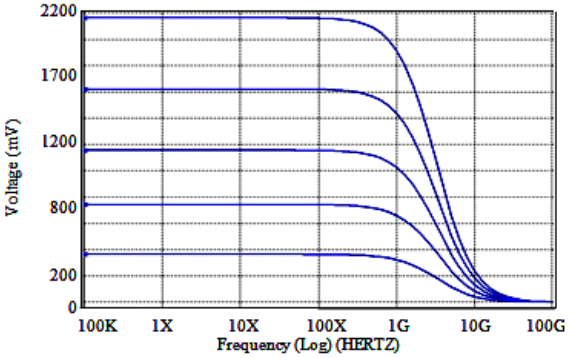


Fig. 7: AC transfer characteristics of the multiplier

Fig. 8 shows total harmonic distortion (THD). Iy current was fed by 1 value as +10 µA. Ix was sine wave by amplitude of 10µA and frequency of 1 kHz to 1GHz.

As seen in the THD graph, when Iy was +10µA, THD was approximately 0.068% until the frequency increase to 10 MHz, in which THD started to increase. The maximum THD was 5.46% at 1 GHz.

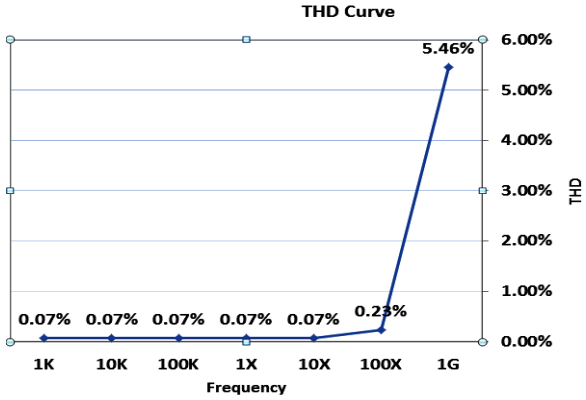


Fig. 8: Relationship between THD and frequency

The next point was about the multiplier circuit applied in the modulator. I_x was 50µA and had frequency of 100 MHz while Iy was a carrier signal with frequency of 1 GHz and amplitude of 50µA, as can be observed in Figs. 9 and 10. The modulated frequency is also shown in Fig. 11.

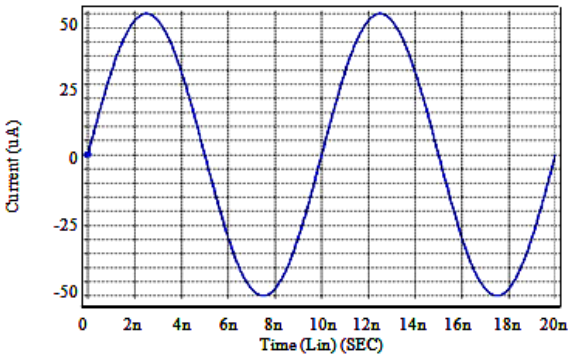


Fig. 9: Sinusoidal input signal

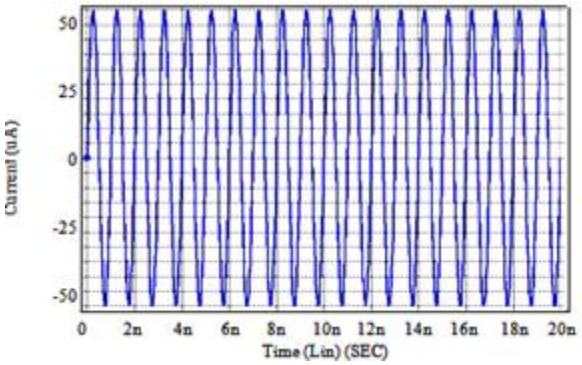


Fig. 10: Sinusoidal input signal

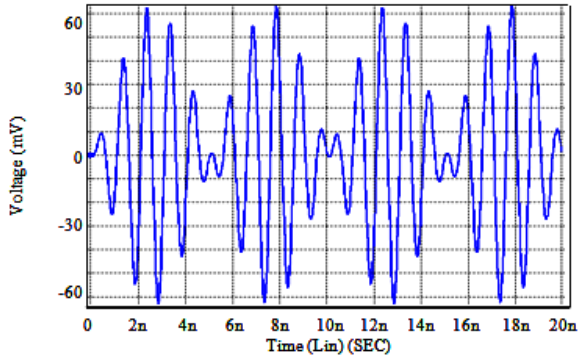


Fig. 11: Amplitude modulation of the two sinusoidal input signal

CONCLUSION & COMPARISION

A current multiplier circuit using ±1.2V voltage supply was proposed in this article. Frequency response of the circuit was 2GHz. Other simulation values and Comparisons are shown in Table 2.

Table 2. Other values of simulation and simulation results

Parameter	Value
Technology	0.18 µm CMOS
Supply voltage	±1.2
CMOS amount	14
Bandwidth	2GHz
Power dissipation	6.1mW
THD(%)	0.068%

Table 3. Compared with the reference [10]

	proposed circuit	Reference [10]
type	current-voltage	voltage-voltage
CMOS amount	14	16
Supply voltage	±1.2	±5
Bandwidth	2Ghz	20Mhz
THD(%)	0.068%	1%

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