Design and Simulation of A New Low Power Consumption High Speed Adder For Analog-Digital Circuits

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Abstract: Full-adders are the core elements of the complex arithmetic circuits like addition, multiplication, division and exponentiation. Regarding to this importance, new ideas and investigations for constructing full-adders are required.Besides, another fully symmetric full-adder has been presented.In this paper a new high speed and low power adder is presented. The circuit uses a hybrid concept of analog and digital circuit design to propagate the carriage and so achieve a Full Adder with 108 ps delay and 10.12µw of power consumption. Results and simulations demonstrate that the proposed design leads to an efficient full-adder in terms of power consumption. The supply voltage of circuit is 0.65-1.5V and circuit is based on 350 nm CMOS technology (with) using HSPICE.

Index Terms: Full Adder, Low Power consumption, Low Voltage, Analog-digital circuit design, Hybrid circuit.

I. INTRODUCTION

Adders are heart of computational circuits and many complex arithmetic circuits are based on the addition. The vast use of this operation in arithmetic functions attracts a lot of researchers` attentions to adder efficient designs [1, 2]. Nowadays, circuits with low power and high speed have a great importance. Specially regarding to development of mobile systems such as portable computers and cell phones, many researches are dedicated to high speed, low power circuits [3, 4, 6]. Consequently, as a critical part of digital processors, adders are largely studied [3, 6].

??power and have a high speed [7], for some problems such as a long time design procedure [8] they were not developed as processors, in contrast with digital counterparts. However, recently, designers used both concepts of analog and digital circuit design to achieve hybrid processors with positive properties of both analog and digital circuits [9- 13]. In this paper also we've used hybrid analog-digital circuits to make an adder with better properties (i.e. with reduced power consumption).

Fig. 1. demonstrates general structure of a full adder; consisting of two half adders and an OR gate. Regardless of implementation details of half adders, they've?? to include at least one gate. With a supposed minimum delay time of *t* for the gates, simply critical path (the path with maximum delay which determines the overall delay of full adder) can be recognized. it's "carry out" path with *3t* delay (shown in Fig.1).

It is also obvious that the minimum of supposed unit time, *t*, might be the transition delay of a transistor for changing the operation mode. Therefore digital full adders will have a valid output at least after three transistor delay time. It is exactly the point where this paper will focus on. It is tried to decrease this delay which in turn will decrease the overall delay time of the Full Adder. To figure out mentioned discussions, a conventional transistor level realization of a CMOS full adder has been inserted in Fig. 2.

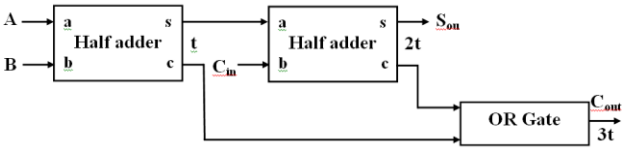

Fig. 1. General Structure of a Full Adder and Delay Propagation.

It is noteworthy that also in an *n*-bit adder consisting of *n* full adders, again the carry propagation path is the critical one and determines the overall delay (Note Fig. 3) . Names of different adders (Carry Save Adder, Carry Look ahead and so forth) in the literature [1, 14] witnesses the importance of carry propagation and the amount of works dedicated to.

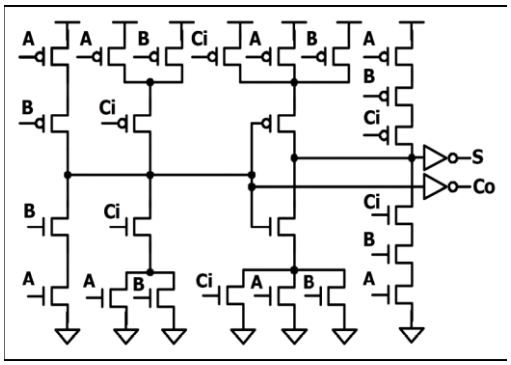

Fig. 2. Conventional CMOS Full Adder

This paper is organized as follow; In the next section the new proposed hybrid analog-digital adder will be presented.

The third section is dedicated to simulation, while the fourth one includes discussions and comparisons. Finally, the fifth section concludes the paper.

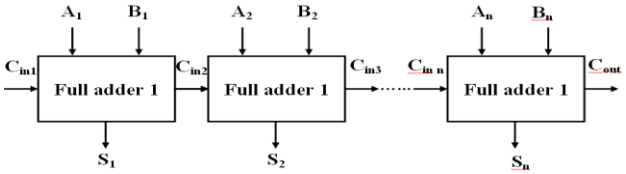

Fig. 3. Critical Path Delay; Carry Propagation is very deterministic

II. CIRCUIT DESCRIPTION

1. Effective Factors in Power Consumption:

In CMOS digital circuits, average power consumption Pav, in general, as the following expression :

$$P_{AV} = \alpha.c.f.V_{dd}^2 + P_{SC} + I_{Leakage} . V_{dd} \quad (1)$$

In this relation Vdd is supply voltage, α is Statistical rate signal changes, C is capacitance equivalent and f is Work-frequency circuit. Also Ileakage is leakage current and Psc is short circuit power. Last component in the right relationship (1) is power related to leakage currents. Leakage currents to three components flow below threshold leakage, gate leakage current and leakage current of bayas reverse source–drain junctions, are divisible. Source-drain current of transistor in model BSIM, is expressed as follows:

$$I_{DS} = I_0 e^{\frac{V_{GS} - V_{th0} + \gamma V_{BS} + \eta}{n V_T}} (1 - e^{-V_{DS} / V_T}) \quad (2)$$

In this Relation, V_T is the thermal voltage and V_{GS}, V_{DS} and V_{BS} are respectively gate-source voltages, drain-source voltage and Body-source voltage. Parameters γ and η are respectively, body effect coefficient and DIBL effect coefficient and n coefficient is slope of the below the threshold. I_0 value is also defined as follows:

$$I_0 = \mu_0 C_{OX} W_{eff} / L_{eff} V_T^2 e^{1.8} \quad (3)$$

In this relation, μ_0 is the electron mobility coefficient, C_{OX} is Capacitance per unit area gate oxide layer, W_{eff} and L_{eff} are the Effective channel length and width of the transistor and V_T is the thermal voltage. Relation (2) shows that in the turn off transistors (V_{GS}=0), drain-source current value is greater than zero. This current, leakage current below threshold is called??. In transistors with a channel length 130 nm and more, leakage currents are small and can be venial. In transistors with smaller dimensions, which also reduced the working voltage to maintain the circuit speed,it is also necessary for threshold voltage to be reduced. Relation (2) shows that leakage current below the threshold with the threshold voltage reduces as exponential increases.In the dimension reduction process, the gate oxide thickness for more control channel, is reduced. Decrease of the oxide thickness , increase of probability of quantum tunneling electron and hole from potential barrier oxide layer are along. Effect of this possibility increase will be as leakage current that will be established between the gate and heads of drain, source, channel and body. Whatever the gate oxide thickness less ??and Gate potential differences with other areas is more, This measure of current is increased [22]. leakage current of reverse Bias source-drain junction is low range and venial. In circuits with high density, Power consumption due to leakage currents A large percentage of the total power consumption makes up and with smaller dimensions is expected amount and percentage increase in the future to be more. Therefore, in designing and modeling digital circuits, it is necessary to consider the effect of leakage currents as determines parameter.

2. Reduce Power Consumption With Control Leakage Current:

Several methodes for leakage current reduction have been proposed. Some methods are used only in passive circuit conditions and some other decrease leakage currents in all cases. Relation (2) shows that increase potential of source in off transistor causes the leakage current reduction. One of the ways to achieve this state, is using a series switched-off transistor. In Figure 4 leakage current and loss resulting thereform, increases source potential in the transistor MN2. So leakage current of two off series transistor is much less than leakage current of off transistor MN1 [23]. With Replacing a transistor with two series transistor , Leakage current will be low, but Against speed of circuit will be low or space consumption increases.

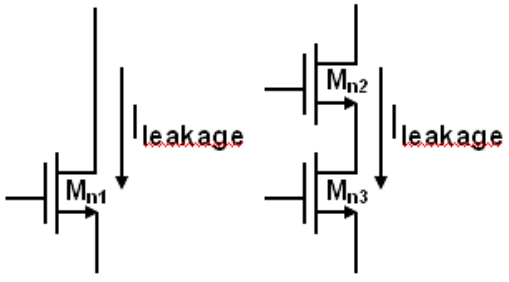

Fig. 4. Reducing leakage current in cut off transistors

Using transistors with different threshold voltage is another effective method in controlling leakage current. Transistors with low threshold voltage have low delay and high leakage current. Unlike High threshold voltage transistors which are with larger delay, Leakage current is less. The best place to use this type of transistor is known with Separation of different input and output ways of circuit to critical and uncritical. In the critical paths total

of path delay is equal with maximum allowable value or very close to it, but in uncritical paths total of path delay is smaller than the Maximum allowable Value.As regards, usually the number of critically paths in digital circuits is low, placing a low threshold voltage transistors in the critical paths and high threshold voltage transistors in the uncritical paths, speed of circuit is fixed, but current leakage can decrease power consumption. In MOS transistors the effective threshold voltage transistors are described using the following equation:

$$V_{th} = V_{th0} + \gamma V_{BS} - \eta V_{DS} \quad (4)$$

In this relation V_{TH0} is initial threshold voltage, V_{SB} is source-body voltage, V_{DS} is drain-source voltage and the parameters γ and η respectively are coefficients of body and DIBL effects. Based on the relation, there is a direct relationship between effective threshold voltage with coefficient γ and body voltage difference to the source. In another way, reduced power consumption that inverse-bias of body is called by change potential of body, increase effecting threshold voltage and leakage current is less???. Needed changes to control the affecting threshold voltage is in type n, the more negative is the body potential than the source and in the p type transistors, the more positive is body potential than the source.

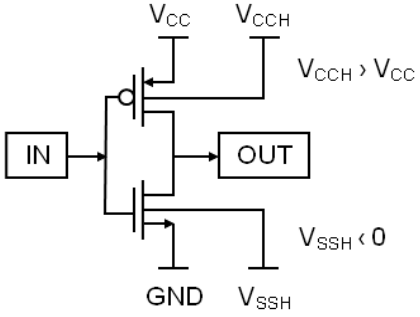

Fig. 5. Reverse body bias technique

Considering the reduced speed of circuit with increase threshold voltage, in another way it is considered connected to the transistor body in two different potentials. In the moments that higher speed is desirable, node of body Transistor respectively is connected to GND and V_{CC} which is less than threshold voltage. With this work, circuit delay is less but leakage current increases. In the Moments that higher speed is not required, body respectively is connected to V_{SSH} and V_{CCH} than??? increase threshold voltage and reduced leakage current. A problem existing in this method is production of needed reverse potential and possible availability of the node body transistors. Another method that is effective in reducing leakage current by adding the channel length (L_{eff})??. With Increased Channel length, the transistor Power Consumption reduces and the speed with the reduced linear track, but against the Leakage current decreases with exponentially rate.

3. Proposed Analog-Digital Circuit:

A. Carry propagation:

In this section we introduce a new design style, entitled "bridge". Bridge circuits are circuits that create a conditional conjunction between two circuit nodes. Using this kind of circuits the classical circuits can be implemented faster and smaller than the conventional. As mentioned before, conventional CMOS design style performs realizations by organizing some different branches. Each branch provides a path from supply lines to an output, whereas bridge design style focuses its attention on meshes, and connects each two adjacent mesh by a transistor, named "bridge transistor". Bridge transistors provide the possibility of sharing transistors of different paths to create a new path from supply lines to an output. These transistors must be arranged in such a way that not only validate the correctness of the circuit, but also preserve pull-up and pull-down networks mutually exclusive. In general, bridge style can lead to very structured designs. In this style control signals can be applied to the sides of meshes [15 ,20].

Figure 6 illustrates a bridge implementation of the three inputs majority function (or carry generator). The transistors in grey boxes (Figure 6) are bridge transistors. This structure uses 14 transistors to implement the relevant function. With respect to high flexibility of bridge methodology, variants of logic circuits can be easily realized. In this design it has been tried to have a symmetric structure in both pull up and pull down networks. In order to construct a full-adder, two different parts are required. Carry part implementation has been performed as Figure 6.

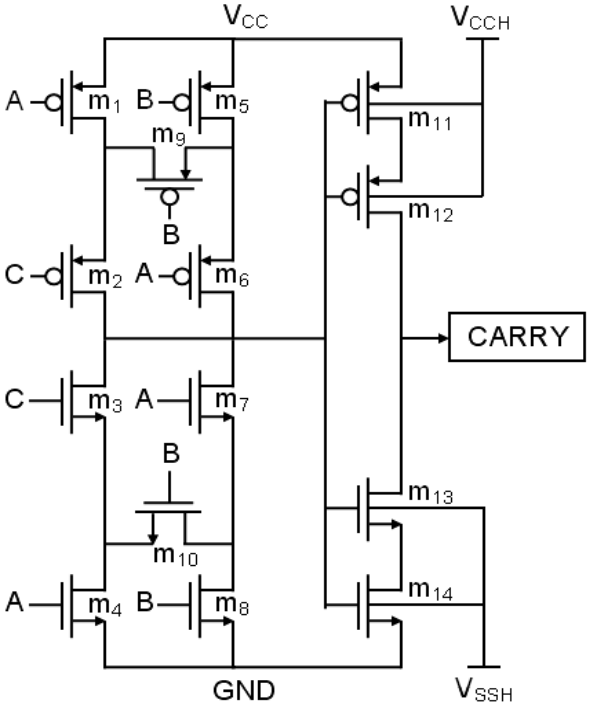

Fig. 6. A symmetric structure for carry generator

In this figure m_{12} and m_{13} are series transistors with m_{11} and m_{14} to decrease leakage current and power consumption. Also in transistors m_{11}, m_{12}, m_{13}, m_{14} body

nodes are connected to V_{CCH} and V_{SSH} to increase V_T and decrease leakage current and power consumption.

B. Sumation:

For summation a simple digital circuit consisting of two XNOR gates has been used to produce output summation as in Fig. 7-(a).

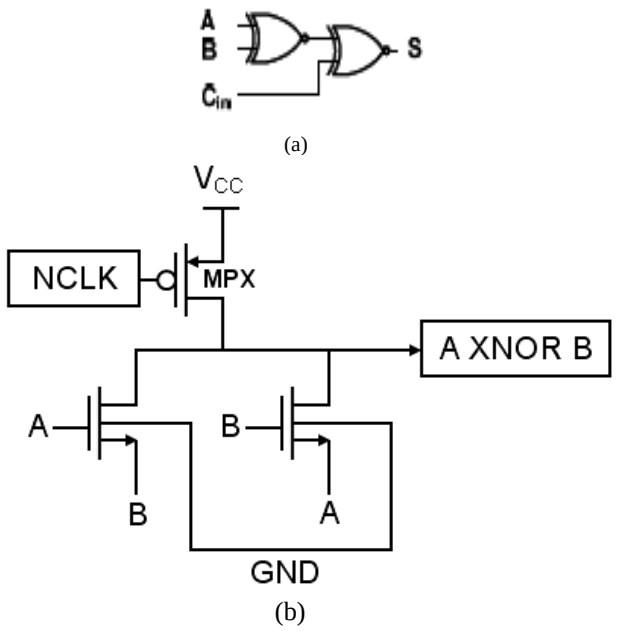

Fig. 7 (a) Digital Circuit for Summation, (b) XNOR circuits used in part (a).

XNORs of Fig. 7-(a) are implemented by circuit shown in Fig. 7-(b). When both inputs are high, or low, both transistors would be in cut-off and so the output remains at high level which was pre-charged to. If one of the inputs is high and the other is low, then one of the transistors (which has a gate node at high level and source at low level) will be in saturation and discharges the output node. Therefore the final circuit of summation was implemented as demonstrated in Fig.8.

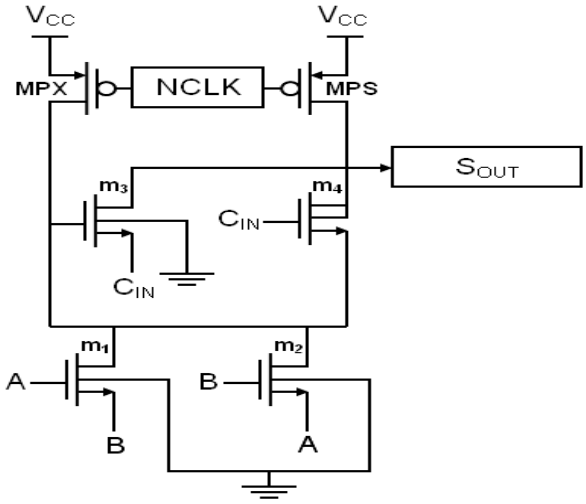

Fig. 8 Final Summation Circuit.

III. SIMULATION

To study performance of the proposed circuit, it was simulated on HPICE, with the 0.35μm TSMC at room temperature with supply voltage ranges from 0.65v to 1.5v. As one of the properties of used technology, the minimum width and length of transistor are respectively 0.60μm and 0.45μm,. Figure 9 shows input signals of A, B, C_{in} and output signals of S_{out} and C_{out}.

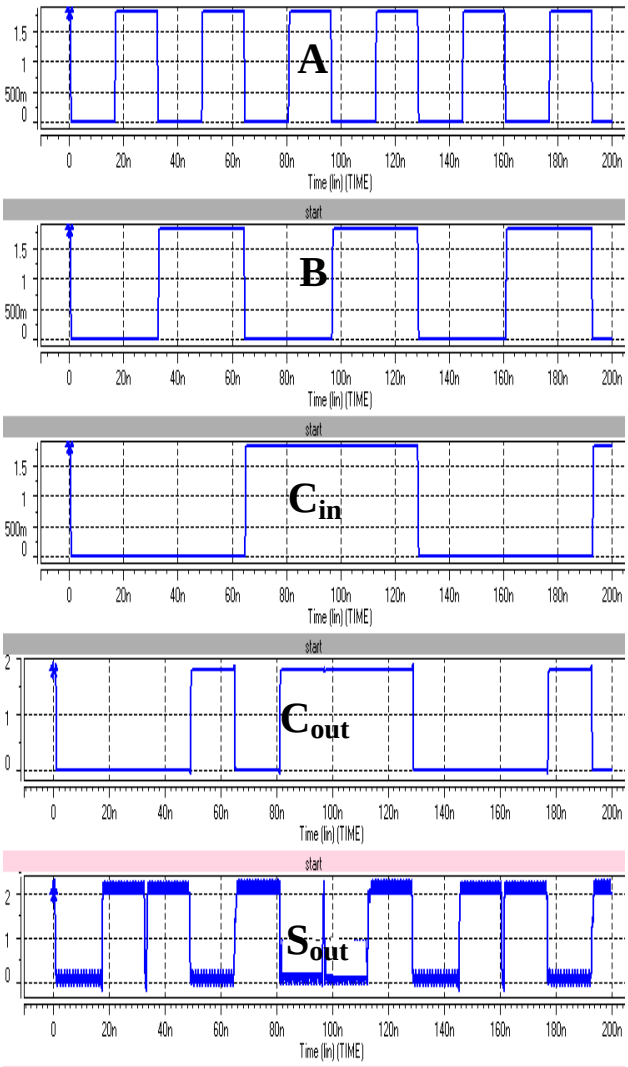

Fig.9. Simulation results for different inputs of the proposed Full Adder.

IV. CONCLUSION

The supply voltage of circuit is 0.65-1.5V and circuit is based on 350 nm CMOS technology (with) using HSPICE. Other simulation values are shown in Table 1.

Number of MOS	20
Supply	0.65-1.5V
power consumption	10.12 μw
Delay	108 ps

TABLE I
SPECIFICATION OF CIRCUIT

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