VHDL Implementation of Bit Processes for Bluetooth Bitstream Datapath

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Abstract **— In this paper VHDL implementation of HEC & CRC generation and data whitening for Bluetooth bitstream datapath is presented. Numerous bit manipulations are performed in the transmitter before the data is transmitted for reliability and security. The bitstream datapath is a part of the baseband module for processing the bit-intensive baseband protocol functions. An HEC is added to the packet header, the header bits are scrambled with a whitening word, and FEC coding is applied. In the receiver, the inverse processes are carried out. Bluetooth bitstream processing may be power-efficient if implemented in hardware. The results show that the propagation delay for the circuit implemented for HEC & CRC generation and data whitening using vertex 2p device is 4.64 ns, 2.922 ns and 4.609 ns respectively. Hence the above circuit may be used in implementation of bitstream datapath for baseband processor.**

Keywords - Bluetooth, Bitstream Datapath, HEC & CRC Generation, Data Whitening and VHDL Implementation.

I. INTRODUCTION

Recently, there is enormous increase in the applications using wireless connecting devices and wireless personal area networking (WPAN) has resulted in various standards, such as Home RF, IEEE 802.11 and Bluetooth. Bluetooth is a short-range radio link intended to replace the wires, connecting portable and/or fixed electronic devices. Bluetooth are built into cellular mobile phones, laptops, desktops etc will help to replace the wires used to connect the laptop to a mobile phones and peripherals to laptop and desktops. Printers, personal digital assistants (PDAs), desktops, fax machines, keyboards, joysticks, and virtually any other digital device can be part of the Bluetooth system [1]. In addition, Bluetooth provides a mechanism to form small private ad-hoc groupings of connected devices away from fixed network infrastructures. Bluetooth establishes ad-hoc voice and data connections and operates in the 2.4 GHz unlicensed ISM band. Its specification is open and royalty-free. The symbol rate is 1 Msps to exploit a maximum available channel bandwidth of 1 MHz. Fast frequency hopping is applied to combat interference and fading. A shaped, binary FM modulation is applied to minimize transceiver complexity. The basic protocols that all Bluetooth systems must have are a radio, a baseband, a link manager, and a logical link controller. The radio takes care of sending and receiving modulated bitstreams. The baseband takes care of the timing, and the framing, as well as packets, flow control, error detection, and correction. The link manager takes care of managing states and packets and of controlling flow on the link. The logical link controller takes care of multiplexing user protocols, as well as segmentation and reassembly of larger datagrams into packets, and management [1]. In this paper hardware architecture for the implementation of HEC & CRC generation and data whitening is presented. The design is simulated using Xilinx ISE synthesis tools and implemented using vertex 2p device. The paper is organized as follows. In section 2 the bitstream processing schemes is explained. Section 3 deals with the hardware architecture of the HEC & CRC generation and data whitening. Results and Conclusion are presented in section 4 and section 5 respectively.

II. BITSTREAM PROCESSING

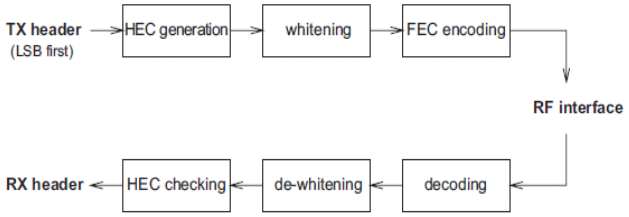

Figure 1. Header Bit Processes [2]

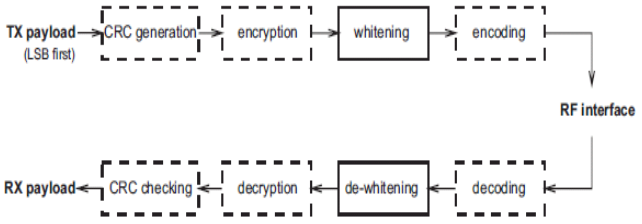

Figure 2. Payload Bit Processes [2]

Numerous bit manipulations are performed in the transmitter before the data is transmitted for reliability and security. The bitstream datapath is a part of the baseband module for processing the bit-intensive baseband protocol

functions. An HEC is added to the packet header, the header bits are scrambled with a whitening word, and FEC coding is applied. In the receiver, the inverse processes are carried out. Bluetooth bitstream processing may be power-efficient if implemented in hardware. All header bit processes are mandatory. In addition to the processes defined for the packet header, encryption can be applied on the payload. Only whitening and de-whitening are mandatory for every payload while all other processes are optional and depend on the packet type and whether encryption is enabled [2]. Figure 1 shows the processes carried out for the packet header at transmit and receive side. Figure 2 shows the processes that may be carried out on the payload. The packet can be checked for errors or wrong delivery using the channel access code, the HEC in the header, and the CRC in the payload. The HEC generator polynomial is given as

$$g(D) = (D + 1)(D^7 + D^4 + D^3 + D^2 + 1) \qquad (1)$$

Figure 3 shows the HEC generation and checking at transmit and receive. Initially this circuit shall be pre-loaded with the 8-bit UAP such that the LSB of the UAP goes to the left-most shift register element, and, MSB goes to the right-most element. Initial state of the HEC is shown in figure 4.

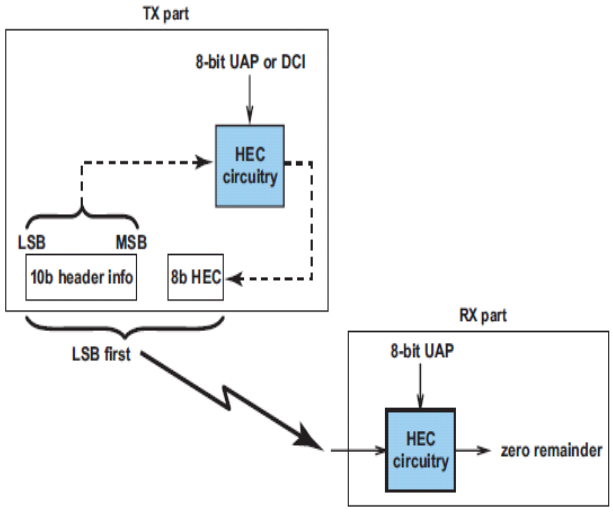

Figure 3. HEC Generation and Checking [2]

Position	0	1	2	3	4	5	6	7
Initial state	UAP_0	UAP_1	UAP_2	UAP_3	UAP_4	UAP_5	UAP_6	UAP_7

Figure 4. Initial State of the HEC [2]

Figure 5 shows the CRC generation and checking at transmit and receive. The 16 bit CRC is constructed similarly to the HEC generator polynomial that is given as

$$g(D) = D^{16} + D^{12} + D^5 + 1 \qquad (2)$$

For this case, the 8 leftmost bits shall be initially loaded with the 8-bit UAP while the 8 right-most bits shall be reset to zero [2]. Initial state of the CRC is shown in figure 6.

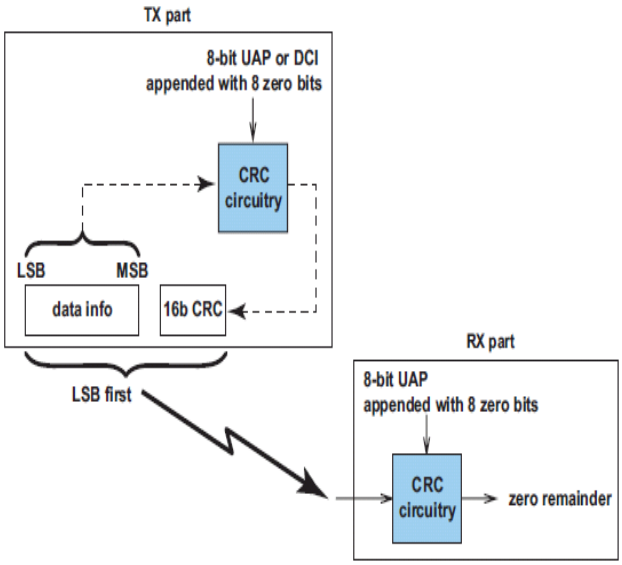

Figure 5. CRC Generation and Checking [2]

The header and the payload are scrambled with a data whitening word in order to randomize the data from highly redundant patterns and to minimize DC bias in the packet before transmission. The scrambling is performed prior to the FEC encoding. At the receiver, the received data is descrambled using the same whitening word generated in the recipient and is performed after FEC decoding. The whitening word is generated with the polynomial given in equation 3 [2].

$$g(D) = D^7 + D^4 + 1 \qquad (3)$$

Position	0	1	2	3	4	5	6	7
Initial state	UAP_0	UAP_1	UAP_2	UAP_3	UAP_4	UAP_5	UAP_6	UAP_7
Position	8	9	10	11	12	13	14	15
Initial state	0	0	0	0	0	0	0	0

Figure 6. Initial State of the CRC [2]

The whitening word $(10010001)_2$ in binary is XORed with the header and payload. Figure 7 shows the generation of whitening word using linear feedback shift registers (LFSR). The LFSR are initialized with the portion of the Bluetooth clock clk6 – 1 extended with MSB of value logic '1'. The initialization is done with the clk 1 at position 0, clk 2 at position 1 and so on, finally clk 6 at position 5 and MSB position 6 initialized to value logic '1' before transmission. After initialization, the packet header and the payload including the CRC are whitened. The payload whitening shall continue from the state the whitening LFSR had at the end of HEC. No re-initialization of the shift register is done between packet header and payload. The first bit of the data in sequence is the LSB of the packet header. For Enhanced Data Rate packets, whitening is not applied to the guard, synchronization and trailer portions of the Enhanced Data Rate packets. During the periods where whitening is not applied the LFSR is paused.

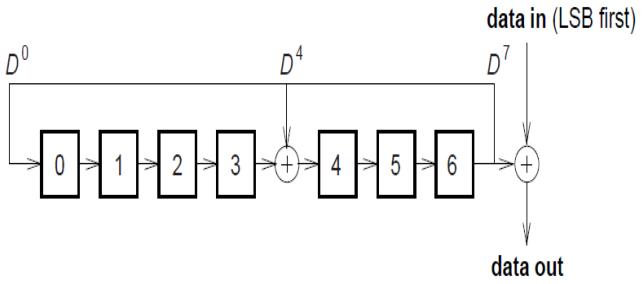

Figure 7. Data Whitening [2]

III. HARDWARE ARCHITECTURE FOR BIT PROCESSES

The hardware architecture for the implementation of HEC and CRC generator is shown in figure 8 and figure 9 respectively. The HEC generator polynomial is given in equation 1. Initially this circuit shall be pre-loaded with the 8-bit UAP such that the LSB of the UAP goes to the left-most shift register element, and, MSB goes to the right-most element. Then the data must be shifted in the register. Finally when the last data has been clocked into the register, the HEC can be read out. The register should be read out from right to left i.e. first transmitted bit will be in position 7 followed by the bit in position 6. The CRC generator polynomial is given in equation 2. For this case, the 8 leftmost bits shall be initially loaded with the 8-bit UAP while the 8 right-most bits shall be reset to zero. Similar to HEC generator the data must be shifted in the register and should be read out from right to left i.e. first transmitted bit will be in position 15 followed by the bit in position 14. The digital circuit implemented for both HEC and CRC generator uses only 8-bit and 16-bit shift registers respectively with polynomial generator and read / write logic. No buffers are used to store the partial results while writing and reading the registers. Thus it reduces the hardware of the circuit, power dissipation and propagation delay.

The hardware architecture entity for the implementation of data whitening is shown in figure 10. The whitening generation polynomial is given in equation 1. Initially this circuit is pre-loaded with Bluetooth clock clk6 – 1 extended with MSB of value logic '1'. The initialization is done with the clk 1 at position 0, clk 2 at position 1 and so on, finally clk 6 at position 5 and MSB position 6 initialized to value logic '1' before transmission. This is done by shifting the data from the clock counter in the LFSR. Finally when the last data has been clocked into the register, the scrambled word can be read out. The LFSR should be read out from right to left i.e. first scrambled bit is obtained by performing XOR operation of input data and position 6 of LFSR. The digital circuit implemented for data whitening word generation uses 7-bit shift register using positive edge triggered D flip flops. The bit D_6 is connected as input to the flip flop FF_0 and XOR operation is performed between the output of flip flop FF_3 and bit D_6. The read / write logic circuit is used to bypassed the XOR operation and feedback while initialization of the LFSR. No buffers are used to store the partial results while writing and reading the registers. Clock gating scheme is used to reduce power dissipation when circuit is idle.

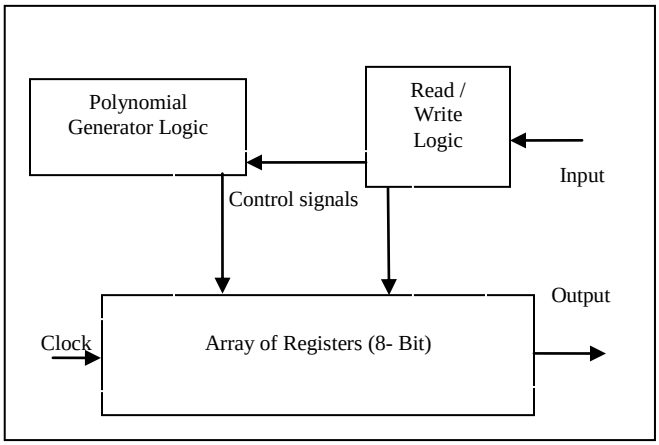

Figure 8. HEC Generator

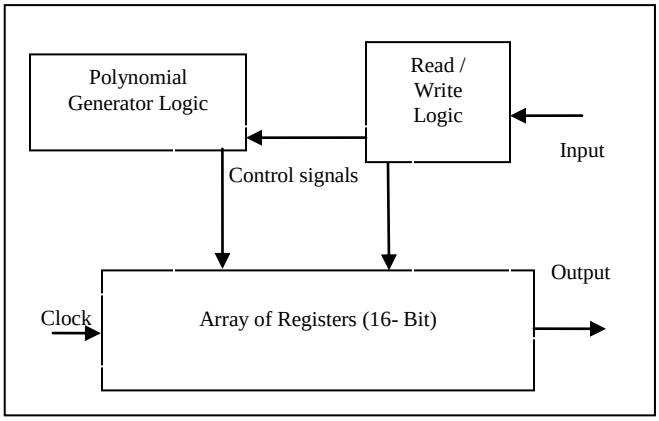

Figure 9. CRC Generator

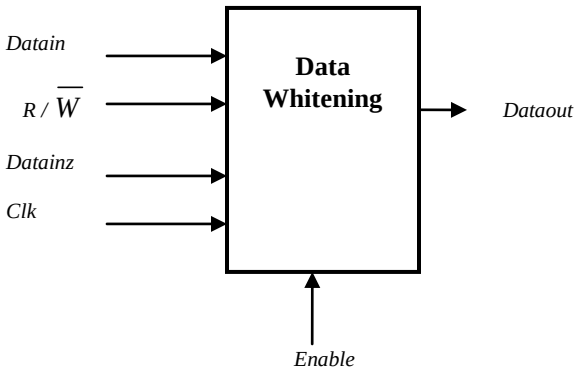

Figure 10. Hardware Entity for Data whitening

IV. RESULTS

The work presented in this paper was implemented using VHDL and logic simulation was done in Modelsim simulator and synthesis was done using ISE Xilinx synthesis tool. The design was synthesized for Vertex2P device [3]. The results obtained for logic delay, route delay and total delay are presented in table 1 and waveform for HEC & CRC generation and data whitening word is shown in figure 11, 12 and 13 respectively.

TABLE I. RESULTS FOR DATA WHITENING

Circuit	Logic Delay (ns)	Route Delay (ns)	Total Delay (ns)
HEC Generation	3.745	0.895	4.64
CRC Generation	2.59	0.332	2.922
Data Whitening	3.745	0.864	4.609

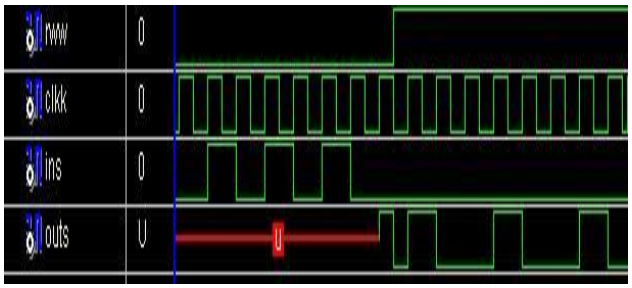

Figure 11. Waveforms for HEC Generation

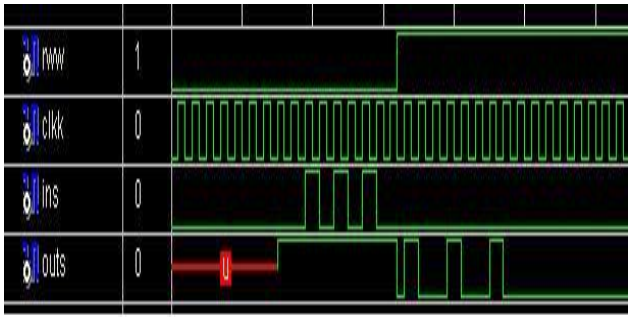

Figure 12. Waveforms for CRC Generation

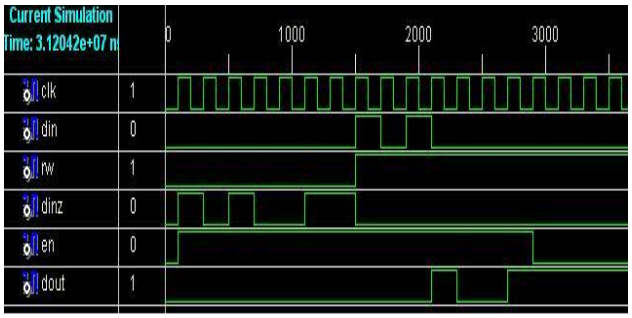

Figure 13. Waveforms for Data Whitening

V. CONCLUSION

VHDL implementation of HEC & CRC generation and data whitening for Bluetooth bitstream datapath is presented. The circuit was designed without buffers for low power consumption and low propagation delay. Clock gating scheme was used to reduce power dissipation when the circuit is idle. Bluetooth bitstream processing may be power-efficient if implemented in hardware. The results show that the propagation delay for the circuit implemented for HEC & CRC generation and data whitening using vertex 2p device are 4.64 ns, 2.922 ns and 4.609 ns respectively. Hence the above circuit may be used in implementation of bitstream datapath for baseband processor.

REFERENCES

[1] *Sunhee Kim, et al, "Design of Bluetooth Baseband Controller using FPGA", in Journal of Korean Physical Society, pp 200-205, vol 42, no. 2, Feb 2003..*

[2] *"Specification of the Bluetooth System Core Package version 4", in www.bluetooth.com, June 2010..*

[3] *"The Programmable Logic Data Book," Xilinx Publication.*

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