Design and Implementation of Queue Length based Dynamic Traffic Light Controller using SPARTAN 6

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***Abstract*— With increased road users, controlling and managing the traffic is always challenging. This paper deals with different way of handing the traffic, called Queue Length based Dynamic Traffic Light Controller (QLD-TLC). The purpose of this proposed paper is to flush out the fixed cycle TLC, which has fixed time counter for all possibilities. In this paper, the reduced waiting time during off-peak hours and smoothen traffic flow during peak hours are achieved by road selection with prioritization on the basis of traffic length. This system also considers an Emergency and/or VIP vehicles passing and safety of pedestrians. The QLD-TLC system offers security and identification of breaking rules by rash drivers. The efficient and low cost queue length based dynamic traffic light controller is developed using Verilog HDL and tested using Simulation. The proposed system is implemented using Wipro Mission10X UTLP Board, in which Xilinx SPARTAN 6 FPGA is mounted with additional interfaces.**

***Keywords*— Queue Length based Dynamic TLC (QLD-TLC), Emergency/VIP vehicles, Peak and Off-peak, Pedestrian Crossing, Verilog HDL , IR sensors, RF Modules and FPGA.**

I. INTRODUCTION

Traditional traffic light control system is based on Microcontrollers, which are fixed cycle controllers, difficult to adapt with various traffic conditions and it is not upgradable. The existing traffic light control systems are having equal time intervals for all conditions, i.e., peak and off-peak times. Due to this, road users may spend more time during off-peak hours also. During emergency vehicles are arrival, the existing system is inefficient to allow that vehicles. And people may not be safe at the intersection when they are crossing the junction. These drawbacks must be improved for increased road users in the modern cities. So the efficient traffic light controller system is needed to achieve traffic flow with different time slots. For this, different approach called Dynamic Traffic Light Controller (DTLC) is used in this paper. DTLC means the counter value should vary depending on the density of the traffic. Also the road with heavy traffic must be given priority over the others.

In this paper, Queue Length based Dynamic TLC (QLD-TLC) system is developed for four intersecting road junction and it is used to solve the traffic chaos and provides smoothen traffic flow. This system provides priority to Ambulances, Fire Engines and VIP vehicles by using Radio Frequency Modules (RF Transmitter & Receiver). Pedestrian's lights are activated for directing people according to shining of traffic lights on particular road and the system is useful for predicting rule breaker by rash driving using IR (Infra-Red) Sensors embedded on the road. The main goal of this paper is to enlarge the existing system with possible conditions for managing traffic flow by considering queue length of particular road with different time slots for both peak and off-peak hours. In this system, priority for the emergency vehicles is provided using RF Transmitter and Receiver. The major accidents can be avoided by directing publics with lights status on every road. The IR sensors are used to defend the junction and to predict the rash drives by triggered on the camera.

Many research works have been published on traffic light controller system using different controlling methods. M.Sabri and Husin have designed FPGA based TLC system to control traffic with various time for four intersecting roads, main roads are controlled with fixed-time controller system and smaller roads are controlled autonomously by sensor [2]. R.Selvakumar and Dr.S.Nirmala have designed and implemented Automated Day-Night Traffic Light Controller with FPGA for four road junction to achieve smoothen traffic flow during Peak and reduced waiting time during off-peak hours [1]. El-Medany and Hussain have implemented FPGA based 24-hour TLC that manage traffic movement of four roads and reached maximum utilization of the traffic during rush hours and normal times [3]. Liu Zhenggang and Xiong Jialong proposed FPGA-based Dual-mode Traffic Lights System that controls the junction with night module and emergency module [4]. Shwetank Singh and Shailendra C. Badwaik have designed FPGA-based Adaptive Dynamic Traffic light controller which manages traffic based on the density of the road and just gives different time based on density [5]. This system does not considered peak and off-peak time slots. Even though different time slots are assigned to the road based on the density, road user must wait for signal during off-peak hours with same time while in peak hour. But this proposed paper considers both peak and off-peak time slots by assigning different times for each slot. The proposed QLD-TLC system design aims to adapt FPGA Technology to

realize functionality to reduce traffic in genuineness. Field Programmable Gate Array (FPGA) is an Integrated Circuit with programmable by user, which contains an array of identical logic cells and extensively used for prototyping and verification of the design [1, 2, 3].

FPGA has many advantages over microcontroller in terms of speed, number of input and output ports and performance [3]. It develops the use of digital systems, can significantly shorten the design time, decrease the number of peripheral circuits, reduce development cost and improve system reliability [4]. FPGA is also cheaper solution compared to ASIC (Custom IC) design which is only cost effective for mass production [1,2]. The Verilog HDL is popular in Electronics Design Automation (EDA) Industries preferred for FPGA design because it offers many useful features for hardware design. Verilog HDL allows different levels of abstractions to be mixed in the same design. It supports most popular logic synthesis tools and all fabrication vendors provide Verilog HDL Libraries [6]. In this paper, Automated TLC system is designed and simulated using Xilinx ISE and also ModelSim simulator. The system actuality is observed by implementing with the hardware Wipro Mission10x UTLP (Unified Technology Learning Platform) Board, in which Xilinx SPARTAN 6 FPGA chip is attached along with OMAP 3530 Processor additionally with number of interfaces.

II. FOUR ROAD STRUCTURE AND SYSTEM SETUP

A. *Four Road Layout*

The road structure considered in this paper is shown in Fig.1. In this Road Structure, there are 12 traffic lights grouped by T1, T2, T3, and T4 for Vehicles passing, and there are 16 Pedestrians lights grouped by P1, P2, P3 and P4 for Pedestrians crossing. Four IR (Infra-Red) Sensors are placed every corner of square and Four RF receivers are placed approximately 500 meters from square on every road, represented by IR1, IR2, IR3, IR4, RF1, RF2, RF3 and RF4 respectively. RF transmitter is attached emergency vehicles. IR Sensors are used to detect unconditionally driving vehicles during red signal is active. RF Modules are used to identify the Emergency vehicles. Then the receiver outputs of all the sensors are fed to FPGA input port for further process. The arrow marks indicates the direction of traffic flow. Set of 16 IR sensors are mounted on median of road, each way has 4 sensors. These sensors are used to detect vehicles queue length.

B. *System Setup*

Traffic light controller system can sense and response to the traffic because of IR sensors and RF modules are embedded on the road. When vehicles cross the sensors it will generate pulses, which are taken as input to the system as shown in Fig.2. The design consists of three modules:

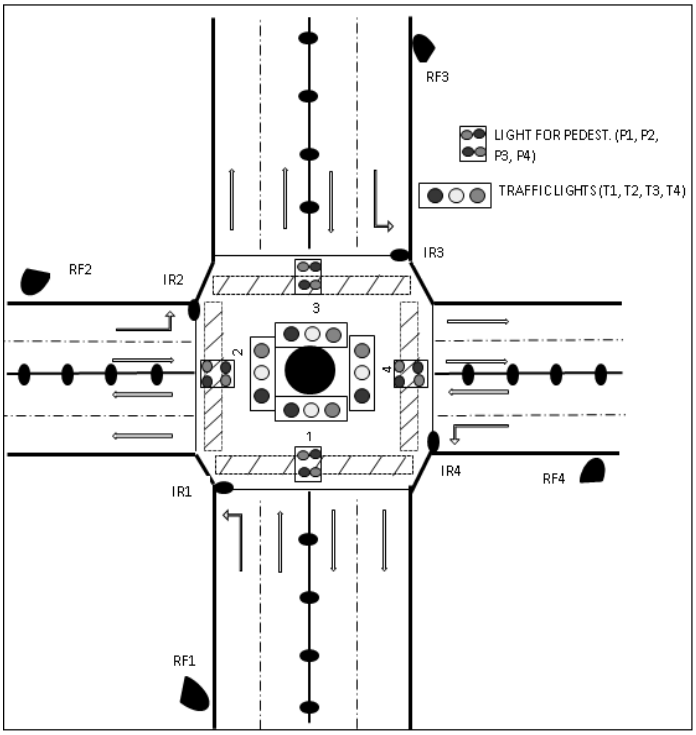

Fig.1.The Four Road Layout

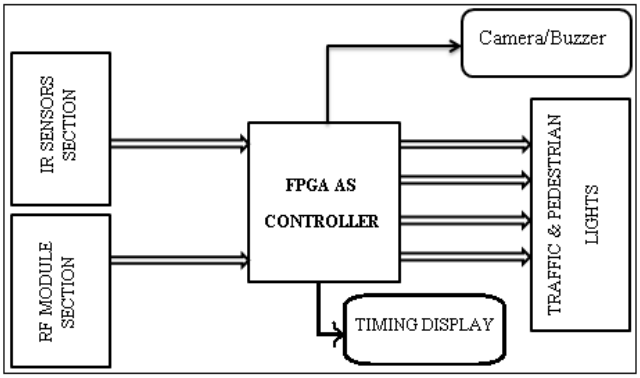

Fig.2.System Setup

Input module: IR sensors, RF modules and its interfaces.

Intermediate module: FPGA as a Controller

Output module: Traffic, Pedestrian Lights, Camera/Buzzer , Timing Display and its interfaces.

The required power supplies for the interfaces are used from FPGA board. The Receiver output is fed to the FPGA as input, FPGA output is derived to traffic lights and Camera/Buzzer signal is used to trigger on the camera or Buzzer.

C. *Verilog HDL Model*

Fig.3. shows the Verilog HDL model of the TLC system, which contains following inputs and output signals.

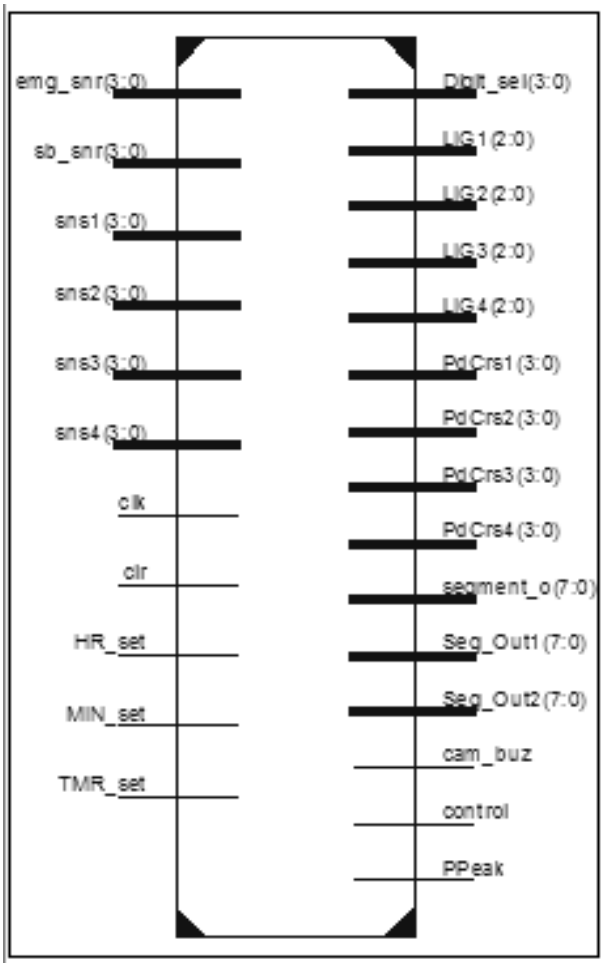

Fig.3.Verilog HDL Model

clk: is system clock.
clr: is system reset.
TMR_set: This is used to enable the assigning of timer inputs.
HR_set, MIN_set: These are used to assign time for system when TMR_set is high.
sb_snr: These are four sensors connected to the controller; it gets active when rash drivers cross the line.
emg_snr: These are four sensors connected to the system, when emergency vehicles are crossed.
sns1 to sns4: These are 16 sensors inputs mounted on the median of road.
LIG1 to LIG4: All are traffic lights for vehicles.
PdCrs1 to PdCrs4: All are signals for pedestrians.
Cam_buz: Control signal, high if any one of 'sb-snr' gets activated.
PPeak: shows the mode of hours.
Segment_o: Seven segment control signals for showing hours, and minutes.
Digit_sel: signal used for selecting digits.
Seg_out1 and Seg_out2: seven segment signals for showing seconds.

III. WORKING OF QLD-TLC SYSTEM

Functionality of the QLD-TLC system is mainly based on timing sequences of traffic lights, which are decided by counters. Counters are enabled based on the intermediate signals generated based on the input sensor values.

A. *Timing setting for traffic lights*

The output modules are awakes with respect to the counter display of traffic lights mounted at the particular square which are corresponding to the Queue Length of the traffic. Different Queue Lengths have various count values are tabulated in table I, II and III, all values are in seconds.

TABLE I

TIMING ALLOCATION FOR EMERGENCY CONDITION

Condition	**Counter**	**Time for Yellow**	**Time for Green**	**Time for Yellow**
Emergency mode	tm_60 (60)	5	52	3

TABLE II

TIMING ALLOCATION FOR OFF-PEAK CONDITION

Condition	**Sensor status**	**Counter**	**Light timing (sec)**	
			Green	**Yellow**
OFF-PEAK MODE	1st Level	tm1_7 (7sec)	4	3
	2nd Lvel	tm1_15 (15sec)	12	3
	3rd Level	tm1_22 (22sec)	19	3
	4th Level	tm1_30 (30sec)	27	3

TABLE III

TIMING ALLOCATION FOR PEAK CONDITION

Condition	**Sensor status**	**Counter**	**Light timing (sec)**	
			Green	**Yellow**

PEAK MODE	1st Level	tm_15 (15sec)	12	3
	2nd Lvel	tm_30 (30sec)	27	3
	3rd Level	tm_45 (45sec)	42	3
	4th Level	tm_60 (60sec)	57	3

IV. SIMULATION RESULTS AND FPGA IMPLEMENTATION

To verify result of the design, Timing Simulation is chosen. Wave forms show the behavioural functionality of the QLD-TLC. Fig.4-9 shows the simulation results of the designed QLD-TLC. In this paper, peak-hour periods are assumed between 7 – 10 AM and 5 – 9 PM. During this time 'peak_offpeak' signal will be high and it will be low for other times as shown in fig.4. Fig.5. shows the output of controller during off-peak hours, in which every road has 2 seconds for yellow signal and green signal timing is based on the Queue Length as discussed in section III. Fig.6. shows the output of QLD-TLC during peak hours, in which every road has 3 seconds for yellow signal and green signal timing is based on sensors strength during peak hour. When emergency vehicles are sensed, i.e. RF receiver receives RF signal from RF transmitter generated from Emergency vehicles, traffic lights can change their states according to receiver signal, which is demonstrated in Fig.7. The waveform shows timing sequence totally 60 seconds, first 5 seconds for warning all roads, 52 seconds for green signal and 3 seconds for yellow. After completing this module, it returns to stages where it is interrupted. This timing is common for both peak and off-peak hours. If reckless drivers are detected by IR sensor, which is mounted above on stop line, pulse will be reached the controller to trigger on the Camera to capture them, which is predicted in Fig.8. For pedestrian crossing, Fig.9 shows timing sequence, in which four roads are getting green and red signal according to the traffic light status. For example, if first lane is in green status pedestrian light will be red to block the people from crossing the junction.

A. *HDL Synthesis Report*

The Hardware Description Language report is tabulated in Table IV, which provides the number of RAM memory, Adders/Subtractors, Counter, Registers, Comparators, Multiplexers and FSMs that have been used while generating hardware out the Verilog HDL code for the design.

Table V entails that the selected device has been efficiently used. Maximum number of slices and LUTs has been utilized. The selected device is XC6SLX25T means SPARTAN 6 FPGA with maximum of 250 available users I/O pins.

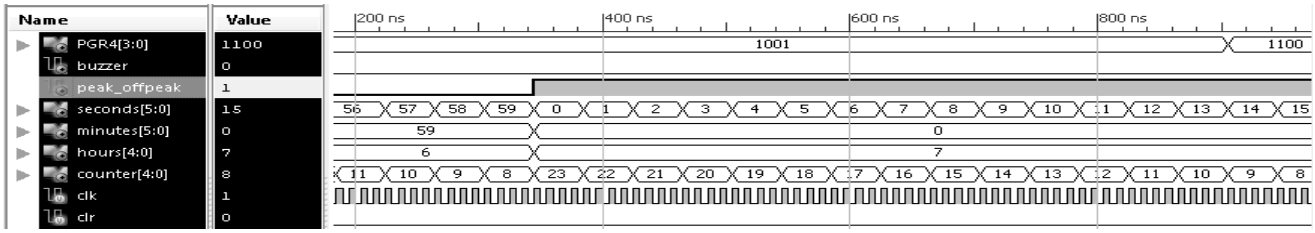

Fig.5. Simulation result of the controller for mode select (peak_offpeak)

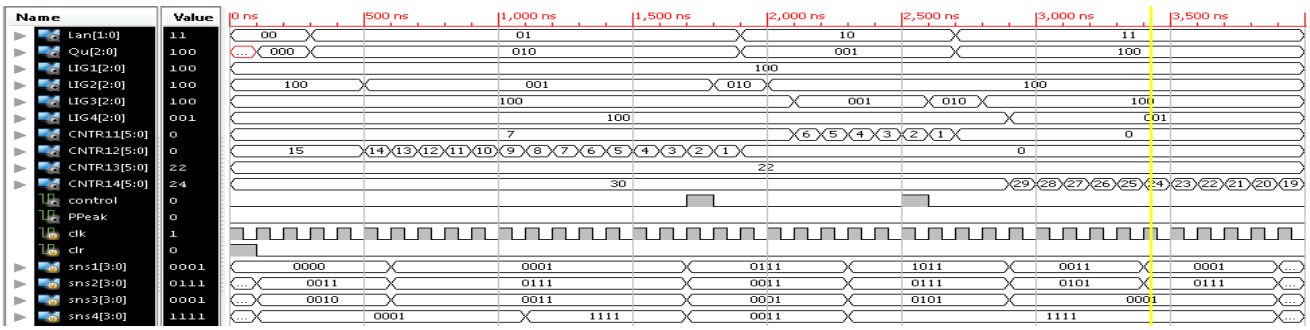

Fig.6. Simulation result of QLD-TLC during Off-Peak hours

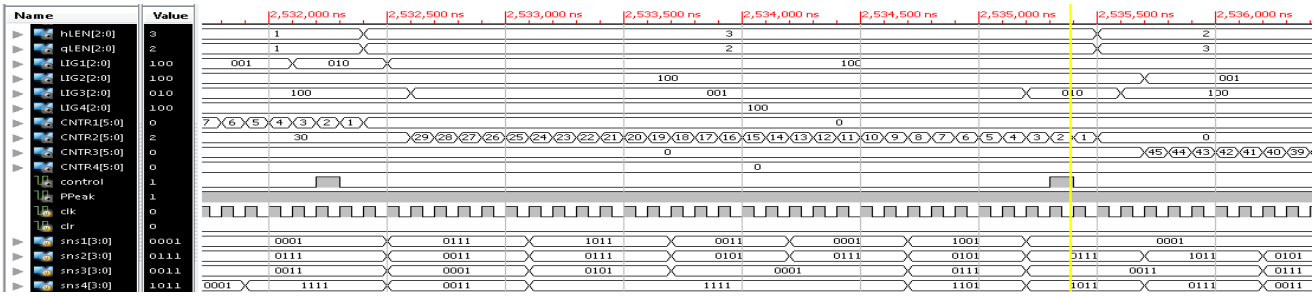

Fig.7. Simulation result of QLD-TLC during Peak hours

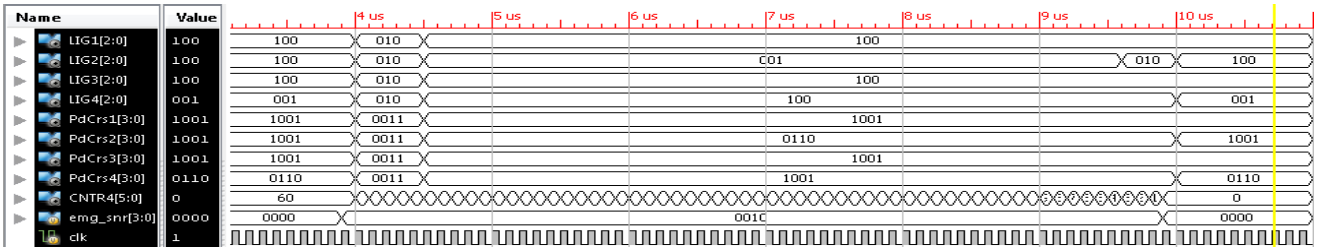

Fig.8. QLD-TLC output during RF sensor is active

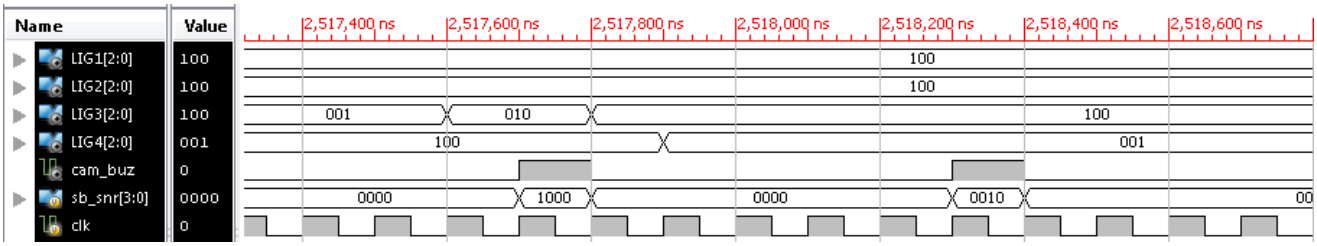

Fig.9. Simulation result of QLD-TLC during IR sensor active

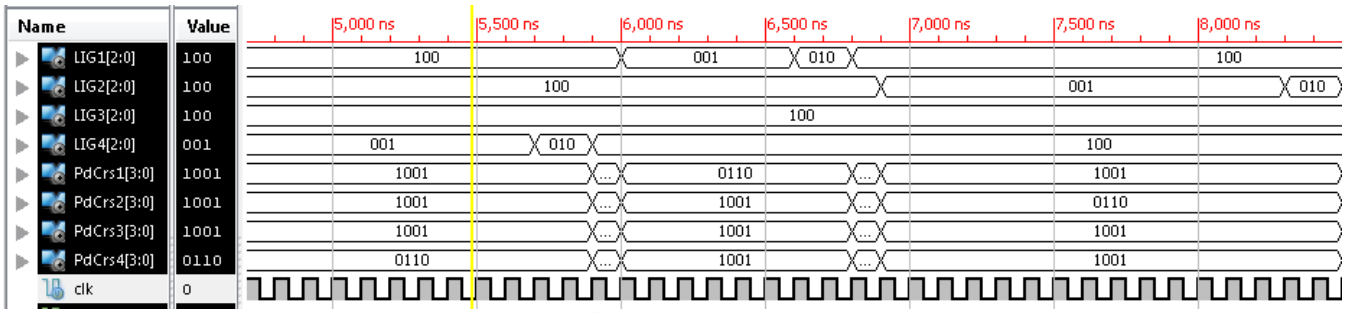

Fig.10. Simulation results of QLD-TLC, during pedestrian lights are active

TABLE IV
HDL SYNTHESIS REPORT

HDL Synthesis Report	
#RAMs	3
#Adders/Subtractors	19
#Registers	55
#Comparators	9
#Multiplexers	350
#FSMs	3

TABLE V
DEVICE UTILIZATION SUMMARY

Selected Device: XC6SLX25T			
Number of Slice Registers	218 out of	30064	0%
Number of Slice LUTs	763 out of	15032	5%
Number of fully used FF	215 out of	766	28%
Number of bonded IOBs	88 out of	250	35%

Number of BUFG/CTRLs	2 out of	16	12%

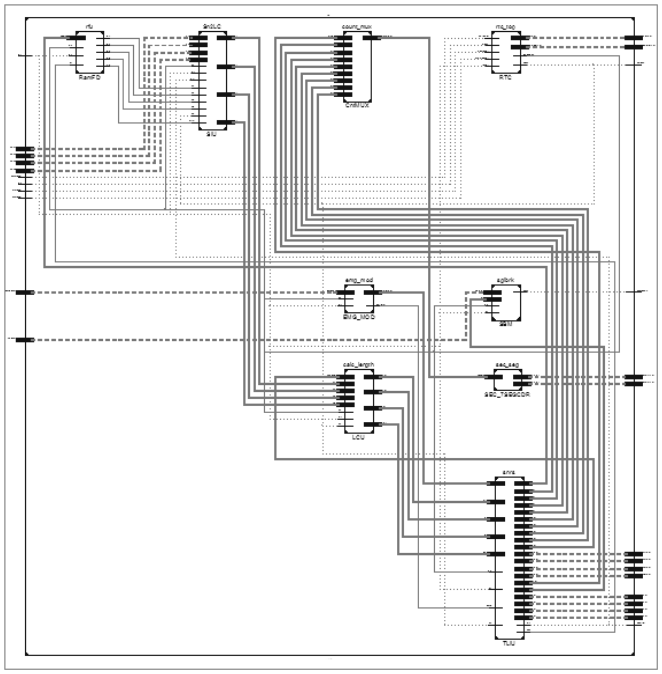

Fig.10. RTL Schematic of the Controller

B. *RTL Schematic*

The RTL Schematic has been generated using XILINX 12.1 ISE Version. The RTL Schematic is displayed in Fig.10, which actually shows the hardware generated inside the FPGA. The design is successfully implemented on SPARTAN 6 FPGA board, after testing the design by simulation.

C. Hardware Setup

Fig.11. shows the system hardware setup, in which the IR sensors are fixed on median of the road, it is then fed to the board via respective connectors, and white objects are represented as vehicles. For signalling purpose, LEDs are used to indicate Red, Yellow and Green signals, which are getting signal from UTLP Board. Seven segment displays are used to indicate timing sequence.

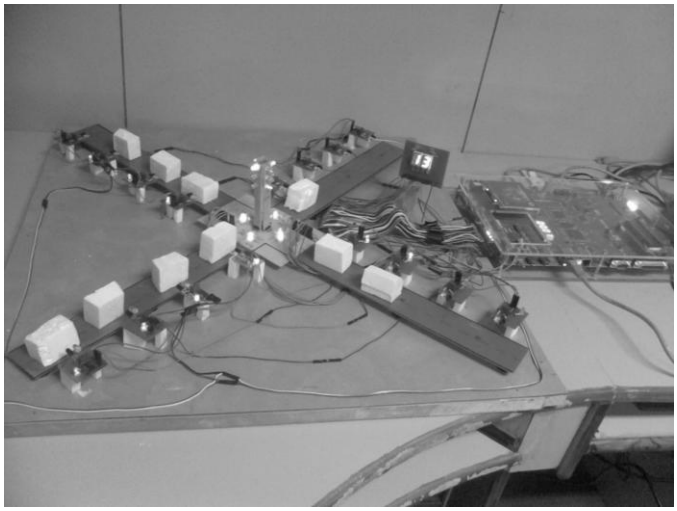

Fig.11. System Hardware Setup using IR sensors with UTLP Board

V. CONCLUSION AND FUTURE WORKS

In this paper, the Queue Length based Dynamic Traffic Lights Controller is designed, tested and implemented successfully to facilitate the traffic flow with different modes and different time slots accordance with Queue Length of road traffic. The system mainly considers the emergency vehicles passing through the intersections and Pedestrian crossing. Designed QLD-TLC is suitable for all conditions and grants full proof to Red signal breaking by rash drives. This efficient system is developed using Verilog HDL and implemented on SPARTAN 6 FPGA for reality. This system is focused on reduced waiting time and mainly for human life. This FPGA based QLD-TLC system costs minimum and reliable to the situations.

Further this system will be developed to consider more intersections and try to synchronize them using Green Corridor concept. Then a comprehensive and exceptional QLD-TLC design can be made into an embedded circuit board to control the actual traffic flow in the city's traffic intersections.

ACKNOWLEDGMENT

I would like to thank my Institution for providing lab facilities and also thank Dr.S.Nirmala (Project Guide) and Mr.T.R.Suresh Kumar (Coordinator) for their supports.

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