A DESIGN & DEVELOPMENT OF (N X N) MULTIPLIER USING REVERSIBLE LOGIC GATES USING VHDL SIMULATION

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Abstract- **There has always been a continuing need to improve the performance and functionality of arithmetic units for efficient computing. This is becoming exceedingly critical, with respect to low-power high speed arithmetic operation requirements, such as calculations based on logarithmic, exponential and trigonometric functions which required use of multipliers. The huge amount of operand associated with multiplier unit results in high power and high heat dissipation leading to increase in cooling costs. In the recent years, Reversible Logic (RL) has emerged as a promising technology for design of low power, low heat dissipation circuits and thus, finding its applications in CMOS, quantum computing, nanotechnology, and optical computing. The aim of this paper is to explore different techniques and implement new reversible logic based N×N multiplier circuit to reduce power consumption and heat dissipation without performance degradation. For proving this, a 4×4 reversible multiplier has been designed using TG gates in its partial product section and it has been found that the garbage output has been reduced to 28 from 52 as found in literature survey. Proposed architecture uses HNG gates as full adder and PG gates as half adder also. The total combinations of TG, PG and HNG gates provide a novel design architecture for the 8×8 or N×N reversible multiplier and have advantages in terms of lesser no of garbage outputs without affecting requirement reversible gates and circuit complexity.VHDL simulation of the 8×8 reversible multiplier is carried out to check the operation and result of the proposed reversible multiplier..**

Keywords- **Reversible Gates, Reversible Logic Adder, Reversible Multiplier Circuits (Rmc), Garbage Outputs, Partial Product**

I. INTRODUCTION

In the life of super computers which have speed of 1000 trillion calculations per second (33.86 peta flops), Most of the critical infrastructures are going to use high speed computing systems and continuously searching for ways to improve the economic and operational efficiencies, reliability and stability. These high speed computing systems are using processors which are faster, smaller and more complex then their predecessors. The high clock frequencies of today's processors along with high component density being used in computing systems lead to heat dissipation in the range of 60-80 watt

[2].So it needs high amount of thermal energy. To remove this huge amount of thermal energy from a processor requires highly sophisticated solutions. Core of heat removal solutions need to be attached with the processor. Once heat conducting connection to the processor is lost, the heat cannot be dissipated anymore and the processor overheats, which lead to disaster scenarios. The primary reasons leading to heat dissipation is:

A. Due to the increase in the clock frequency, Rise in power consumption.
B. Increased number of component density packed into a chip.

Computation of frequency domain filtering (FIR), frequency time transformation, etc required logarithmic, exponential, trigonometric and arrays etc. Implementation of above functions depends on the performance of the multiplier units of processor. Above referred constraints may be challenged by designing low power multiplier circuits, which is critical component of computing system. Thus, if a computation using high speed low power multiplier may be implemented without loss of information, the energy requirement could ideally be reduced to zero which is the best advantage of the system [1].

In this paper, design approach of 4×4 reversible multiplier has been proposed and comparison of various parameters with existing counterparts has been made. Results are also verified for 8×8 reversible multiplier using VHDL simulations.

II. WHY REVERSIBLE LOGIC TECHNOLGY REQUIRED?

On one side when Low power consumption and dissipation has become a crucial factor in the modern computing circuit design and its performance enhancement at that time On the other-hand, with a rapid revolution in silicon technology, the transistor sizes are decreasing at a faster rate as predicted by Moore's Law [4]. Due to this fact, power, component and power density (power per unit area) of VLSI circuits built with these transistors continues to generate serious amount of heat, consuming more power and finally reducing speed [3]. The reasons behind this is the use of conventional logic operations like NOT, AND, OR and XOR etc. These conventional logic gates which are called as "Irreversible Logic Operations" draws $C \times V^2$ Joules of energy, but energy stored in the capacitor is only $\frac{1}{2} \times C \times V^2$ Joules. Remaining half of the energy is dissipated in the form of heat when-ever a transition of signal from logic 0 to logic 1 or logic 1 to logic 0 takes place. Such operation will end the Moore's Law in the next decade [3], which has been the bench mark law for the growth of microelectronics semiconductor industry for more than five decades.

In 1960 R. Launder [6] had shown loss of single bit of information causes *KTln2* joules of energy dissipation in the form of heat where *K* is Boltzmann's Constant and *T* is absolute Temperature. Bennett [5]

In 1973 proved that heat dissipation of *KTln2*, for each bit loss, may be avoided by using Reversible Logic Gates (RLG).Any gate or circuit is said to be reversible if there is one to one mapping between input and output and by inversing the output, we must be able to reproduce exact input. Conditions of reversibility's are given in [7]–[11].

After 40 years of sporadic research through out the world on reversible logic technology, this idea is finally approaching the realm of practical implementation of reversible computing which is finding its applications in Low power CMOS, Quantum Computing, Nanotechnology, DNA Computing, Optical Computing, Bioinformatics and Cryptography and many more to come.

III. 8×8 MULTIPLICATION OPERATION

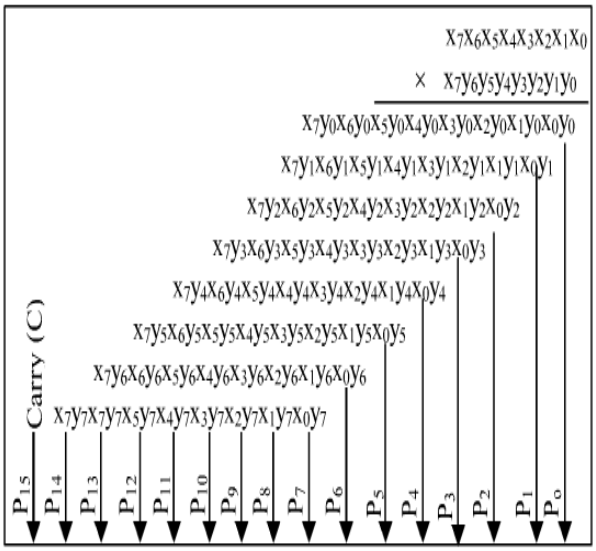

Fig. 1. Partial Product Generation

As shown in Fig. 1 multiplier operation consist of two parts. First part is generation of partial product of the form x_i, y_i, known as partial product generation in total 64 bits are generated for the partial product.

The second part is the addition of the all 64 bits partial product shown in Fig. 1 in the form P_i, i.e. P_0, P_1, P_2... It requires multiplication of the two bits first and then the addition on these bits. For this operation we have to decide the reversible gates best suited to the operation of the multiplication and addition, w.r.t. minimum garbage, gates and constant input values.

IV. PARTIAL PRODUCT GENERATION USING TOFFOLI GATE

During literature survey [12]-[16], it was found that Peres gate (PG) and Fredkin gate was being used for generation of partial product which resulted for a minimum number of 32 garbage outputs and 16 numbers of constant inputs for 4×4 reversible multiplier. In this paper it is proposed to use Toffoli Gate [18] gate instead of using the Fredkin gate or Peres gate [17] at partial product level. The constant input required at each TG gate is only one that is logic '0', so in total 16 constant inputs are required.

TG gate is shown in Fig. 2. If $A = y_0, B = x_0$ and $C = 0$, we get,

$$P = y_0$$
$$Q = x_0$$
$$R = x_0 \cdot y_0$$

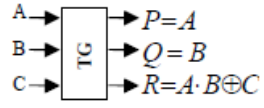

Fig. 2. Toffoli Gate (TG)

Here $P = y_0$ will be used as the input to the next stage of the partial product, $Q = x_0$ will act as an input to the next TG gate below the first one and $R = x_0 \cdot y_0$ is the required partial product term as shown in Fig.1and in similar manner partial product term for remaining can be generated.

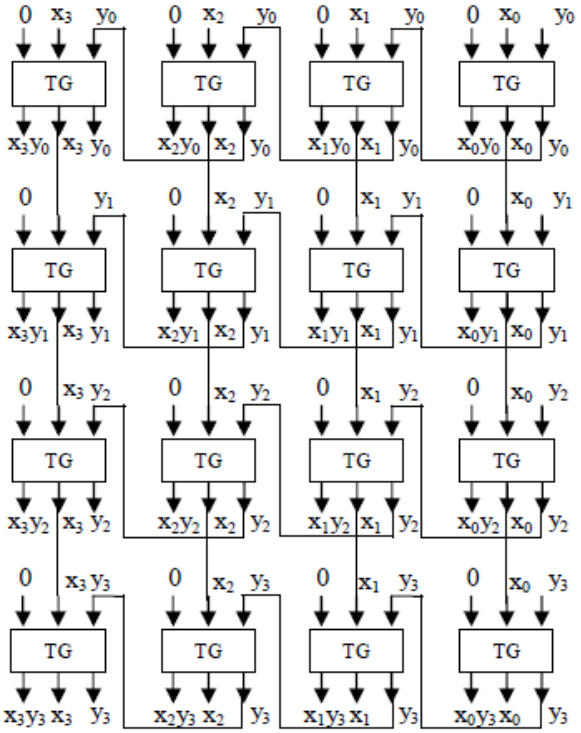

Fig. 3. Partial Product 4×4 using TG gate

During survey of literature [12]–[16] it was found that, in all the previously proposed multiplier architecture and comparisons are based on 4×4 reversible multiplier because of this reason, the detail architecture arrangement for the generation of the partial product for 4×4 reversible multiplier using TG gates is shown in fig.3. The same arrangement can be increased to form 8×8 or N×N reversible multiplier.

In this arrangement as shown in Fig. 3, it has been proved that the numbers of garbage bits generated are reduced with respect to their counter-parts because of using the outputs of the different stages of the TG gates as the input to the next stages as shown in Fig.3. Total numbers of constant inputs are 16 and number of garbage outputs are 8 at the partial product level which is much lower to their counter parts as proposed previously in different papers at the partial product level.

V. FINAL PRODUCT GENERATION

As shown in fig.1 the final product generation for 8×8 reversible multiplier is given as P_0, P_1, P_2 . . . P_{14}, P_{15}. This is the final part for getting the product term by adding the different terms generated at the partial product level. For example for,

$$P_0 = x_0 \cdot y_o$$
$$P_1 = x_1 \cdot y_0 + x_0 \cdot y_1 + c_{in}$$
$$\vdots$$
$$P_{14} = x_7 \cdot y_7 + c_{in}$$
$$P_{15} = c_{out}$$

Where $x_0 \cdot y_0, x_1 \cdot y_0 + x_0 \cdot y_1 + c_{in} \cdots$ are the partial product of the 8×8 reversible multiplier.

The same arrangement can be converted into a 4×4 reversible multiplier, with final product as,

$$P_0 = x_0 \cdot y_o$$
$$P_1 = x_1 \cdot y_0 + x_0 \cdot y_1 + c_{in}$$
$$\vdots$$
$$P_6 = x_3 \cdot y_3 + c_{in}$$
$$P_7 = c_{out}$$

So, half and full adder are required for final product.

VI. FINAL PRODUCT USING PG AND HNG GATE

For implementing half and full adder many reversible gates are available such as Peres Full Adder Gate (PFAG) [16], Thapliyal Srinivas Gate (TSG) [19], Peres Gate (PG), Haghparast Navi gate (HNG) [19]. In this paper PG gate is used as half adder and HNG is used as full adder for implementing final product [12]. PG gate is chosen [12] as a half adder because of its less hardware complexity and quantum cost as compared to the HNG gates. PG gate is a 3-input 3-output reversible gate as shown in Fig. 4 and its input and output vectors are given by,

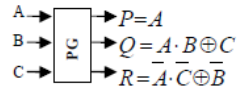

Fig. 4. Peres Gate (PG)

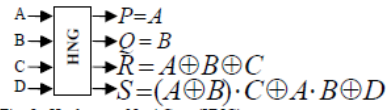

Fig. 5. Haghparast Navi Gate (HNG)

$$I_v = (A, B, C)$$
$$O_v = (P = A, Q = B, R = A \cdot B \oplus C)$$

Because PG gate is used as half adder, so making, $C = 0$, output will be,

$$P = A,$$
$$Q = A \cdot B$$
$$R = \bar{A} \oplus \bar{B} = A \oplus B$$

This will convert the Peres gate into half adder.

HNG gate is used for full adder, is a 4-input, 4-output reversible gate as shown in Fig. 5 and its input and output vector is given by,

$$I_v = (A, B, C, D)$$
$$O_v = (P = A, Q = B, R = A \oplus B \oplus C, S = (A \oplus B) \cdot C \oplus A \cdot B \oplus D)$$

By making $C = c_{in}$ and $D = 0$ the output vectors for HNG gate are,

$$P = A$$
$$Q = B,$$
$$R = A \oplus B \oplus c_{in}$$
$$S = (A \oplus B) \cdot c_{in} \oplus A \cdot B$$

The architecture [10] for the final product using PG and HNG gates are shown in Fig. 6 for 4×4 reversible multiplier.

VII. 4×4 REVERSIBLE MULTIPLIER

From the Table 1, it has been proved that, if TG gates are used for partial product generation, for 4×4 reversible multiplier, 8×8 reversible multiplier or N×N reversible Multiplier, then the reversible multiplier is better in terms of, minimum no of gates, garbage outputs and constant inputs used. In the coming section, by the use of the same architecture the, design of the 8×8 reversible multiplier has been shown along with the VHDL simulation.

VIII. N×N REVERSIBLE MULTIPLIER

After proving the advantages of using of TG gates for the partial product generation, the architecture has been extended for the N×N reversible multiplier as shown in Fig. 7.

IX. 8×8 REVERSIBLE MULTIPLIER

The operation of 8×8 reversible multiplier is similar to the 4×4 reversible multiplier. The 8×8 reversible multiplier consist of 64 partial product bit of the form x_i and y_i already shown in Fig. 1. As discussed earlier proposed reversible 8x8 bit multiplier circuit has two parts. First the partial products are generated in parallel using Toffoli gates similar to the 4×4 reversible multiplier as shown in Fig. 3. Partial product circuit uses 64 TG gates as one bit for 8×8 reversible multiplier. And in the second part addition is performed for final product generation given in the form of P_0, P_1…..$P_{15,}$ shown in Fig. 1.

The basic cell for product generation is full and half adder. HNG gates are used as reversible full adder and PG gates are used as reversible half adder. The proposed 8×8 reversible multiplier circuit uses 47 reversible HNG full adders and 15 reversible half adders. VHDL simulation has been carried out to check the basic arrangement, operation and result for different values of the x_i and y_i as shown in Table 2.

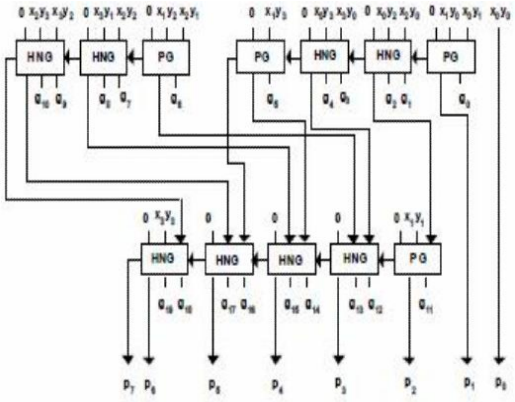

Fig. 6. Final Product of 4×4 Reversible Multiplier [10]

Table 1
Comparative table for Reversible multiplier

	No. of Gates	No. of Garbage output	No. of Constant input	VHDL Simulation
This Paper	28	28	28	YES
[12]	28	52	28	NO
[13]	40	56	31	NO
[14]	29	58	34	NO
[15]	28	56	32	NO
[16]	28	52	28	NO

Table 2
8×8 Reversible Multiplier Input

8-BIT x_i INPUT								8-BIT y_i INPUT							
x_7	x_6	x_5	x_4	x_3	x_2	x_1	x_0	y_7	y_6	y_5	y_4	y_3	y_2	y_1	y_0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	0	0	0	1	1	1	0	0	1	0	0	0
1	1	0	0	0	0	1	1	1	0	0	1	0	0	0	1
0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1

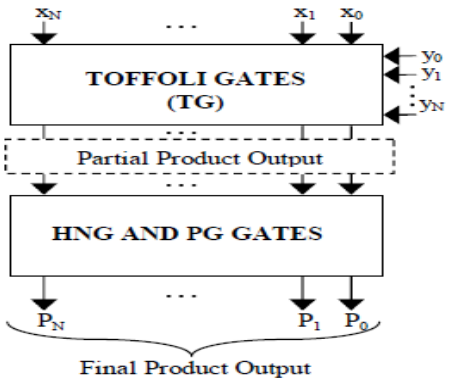

Fig.7. N×N Reversible Multiplier

X. CONCLUSION

In this paper, an approach has been proposed for design of reversible multiplier circuits with less numbers of garbage out put with respect to its previous counter parts. In the proposed design, partial products have been generated using Toffoli gate (TG). The comparison between the proposed multiplier and those of previous works at partial product level showed that no. of garbage output at the partial product level is about 75% less than that of the previous work for 4×4 reversible multiplier .

The prospect for further research include the reversible implementation of adder circuits for further reduction of garbage outputs with less depth of circuits. The approach multiplier may be further extended for N×N reversible multipliers.

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