An Efficient Architecture in Clock Gating Using Wide Spread Adapting Technique

[1]**R.Kiruthika,** *M.E-VLSI Design,NPRCET,*rkiruthika23@gmail.com
[2]**Dr.T.Kavitha,** *Professor /ECE,NPRCET,kavithaecephd@gmail.com*

Abstract: **The Clock gating reduces dynamic power dissipation in synchronous circuits. A clock gating cell (CGC) is inserted, which covers an internal latch that filters out potential glitches from a block called as the gating function. Clock gating logic uses strong and weak matching process,they are two kinds of factor form matching.The strong matching seeks for the matches which are externally present in the factored forms and the weak matching identifies matches that are implicit in the logic and they are hard to discover. The problem in existing system involves a flip-flop architecture with higher power consumption, gate count and circuit size . Hence a modified Boolean function technique known as Wide Spread Adapting (WSA) clock gating technique is implemented. The weak and strong matching are done by WSA technique since they do not require separate algorithms as in existing system's technique helps to reduce the clocking signal and the gate pattern. Thus the proposed method achieves reduced clock gating which also reduces delay, power, gate count and area.**

Keywords: **D flip-flops, flip-flop architecture, WSA technique, clock gating, strong matching, weak matching.**

I. INTRODUCTION

Clock gating helps to reduce clock power consumption. The 40% of power is drawn by network of clock distribution and registers. In synchronous circuit the Gating is a power-saving techniques, in other words it is a process of modifying selective signals. The clock gating is in a form of integrated clock cells.

Automatic gating function synthesis obtained from a gate level net list is another approach [1]-[3].From designer point of view it is a convenient approach. The RTL approach in a complement form is not specified by designers. The methods of using low power design in an automated design flow was explained, and the design time and performance trade-offs are examined [4].

A conventional positive-edge-triggered flip-flop (FF) senses and responds to the control input, at the time the clock input is changing from 0 to 1. All flip-flops in a circuit respond at single clock cycle but the efficiency gets reduced due to more clock cycles [5].

The power dissipation can be reduced automatically by synthesizing gated–clocks in synchronous static CMOS circuits. Flip–flops are grouped in and so called hold domains, and clocked by a gated–clock signal. The testability problem plays a vital role here [6].

Clock gating is the most popular among these techniques, and now has become a standard design practice. It involves the conversion of load-enable registers. Clock gating is usually applied within RTL design. During this process, a clock gating cell (CGC) is inserted, which contains an internal latch that filters out potential glitches from a block called as the gating function.

II. OVERVIEW OF THE APPROACH

Clock gating process saves significant die area as well as power, the multiplexers in a circuit are removed and the clock gating logic is implemented here in order to produce better results. A Wide Spread Adapting (WSA) clock gating technique is implemented here which is a modified Boolean function technique. It is an advanced technique used in clock gating logic. It uses a matching factor forms, which helps to find the same pulse gate signals and uses that signal and satisfy the same signal needed in tree structure.

The matching factor forms are done by strong and weak matching, they uses separate algorithms. The WSA wide spread adapting technique used here does the matching process hence they don't need any algorithms for matching process.

The WSA clock gating technique helps to reduce gating count. The word adapting tells that it has the ability to adapt themselves according to the circuit used in a process. The single clock is used to trigger all gates and flip-flops used in a circuit hence the power consumption is reduced in a process.

The significant die area also gets reduced, In other words the unused or wasted area gets reduced in a circuit.

The Boolean equation can also be modified in order to produce expected results. This method of clock gating technique uses matching factored forms. It helps to find the same gate signals in a circuit. If it finds the same signal in circuit, it then ON one signals to provide the all stages in the tree structure and at same time all other same signals is in OFF condition

The WSA technique is mainly used to reduce the clock gating function based on the gate tree connection and also optimizes the tree architecture. The clocking control modifies the internal gating functions and improves the clock controlling level. The clock formation improves the clocking speed and enhances the system functions.

The WSA technique helps to analyse the hierarchal tree formation and to reduce the clocking function. The matching process such as weak and strong match is done by the wide spread adapting algorithm. This technique helps to reduce delay, area, gate count and power in a circuit. This process deals with the modules such as clock, D flip-flop, gating function (WSA) and hierarchical formation.

III. MODULES & ITS DESCRIPTION

A.MODULES

The WSA technique is drawn by modules such as

- Clock
- D Flip-flop
- Gating function
- Hierarchical formation

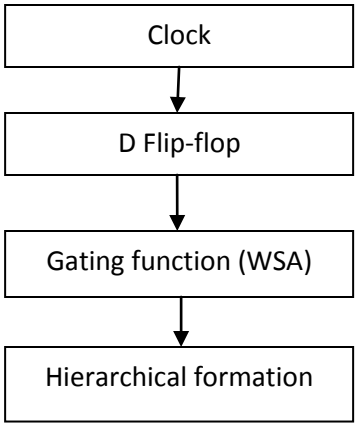

Fig: 1 Flow diagram

B. MODULE DESCRIPTION

From fig:1 the above structure reveals the modules involved in the process of clock gating using wide spread adapting technique. The input given to the system is a clock signal. The clock signal controls the process and the gating functions. It also controls the flip-flops and gates such as AND gate and the OR gate in architecture. The clocking signal improves the system performance and reduces the signal delay.

The D flip-flops are used to optimize the clocking and these flip-flops are assumed as the input to the gating function, the flip-flops are named by the variables here. The D Flip- Flop is by far the most important of the Clocked Flip-flops as it ensures that inputs S and R are never equal to one at the same time. But this problem occurs in SR flip-flop, if the value of S and R are 1 then the race condition occurs in a circuit.

The gating function helps to modify the circuit complexity based on the gate pattern count and the interconnection of the gate connection. The Wide Spread Adapting technique is done here in a gating function. The hierarchical formation helps to find the output results effectively and final clock gating architecture to be designed. The WSA technique uses a bottom up method for processing.

IV. EXISTING SYSTEM

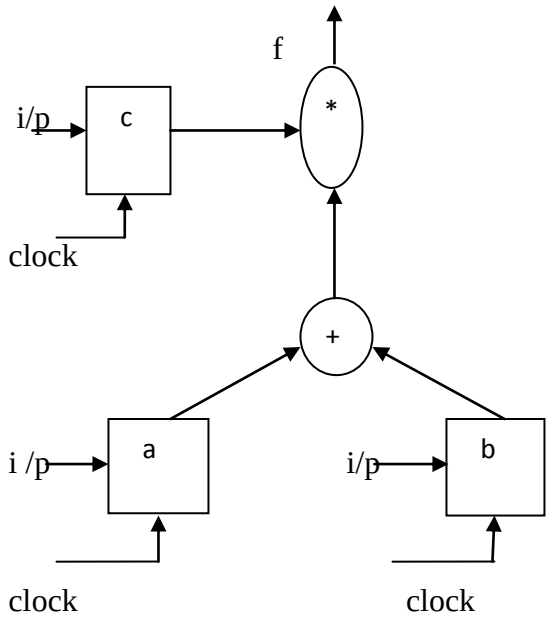

Fig:2: Existing system

From fig:2 the above architecture has two inputs a and b for OR gate. The variable a and b are considered as a D flip-flop. Consider that if a input of a and b are 1 and 0 then the output obtained at OR gate is 1.

The output of OR gate is given to the AND gate, the input c is also given to the AND gate, the c is also a D flip-flop which includes clock and input. The input variable a and b also has its separate clock. The input of c can be 1 or 0, if the value is 1 then the output obtained at AND gate is 1.if the input is 0 then the value obtained at AND gate is 0.The output of AND gate is the output of function. All these values are obtained at output only if the clock is given to the flip flops used here if the clock is not applied then the value do not obtained at the function**.**

V. PROPOSED SYSTEM

In proposed system the clocking is not given separately for each and every flip flop present in the process. This is achieved by implanting WSA technique.

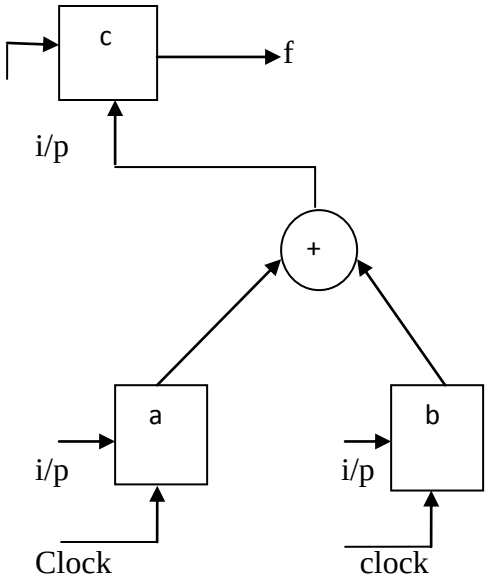

Fig:3 : Proposed system

From fig:3 The proposed system includes D-flip-flops, OR gate and clocking. Consider the input 1's and 0's, given for a and b block they should be ORed at the OR gate. These inputs a and b are D flip-flops containing inputs and separate clocking. If the inputs of a and b are is 1.

The output of OR gate is given as a clock to the c , instead of giving them to AND gate. The c has a separate input, the clocking depends upon the values of output of OR gate. If the value obtained at OR gate is 1, then the input given to the c is shifted and output is obtained as 1.In other case if the value obtained at OR gate is 0, then the clocking is not given hence the value is not obtained at the output. The output of c is the output of function. All these operations depends upon clocking only if the clocking is given the output obtains else not.

The WSA technique is applicable for the above architecture fig:3 :if the gates are interchanged ie if the OR gate is present in the place of AND gate and the AND gate is present in the place of OR gate then this method is not applicable because they do not satisfy all combinational inputs.

VI. SIMULATION AND RESULTS

Tabulation for delay, power and gate count for existing and proposed system

Architecture	Flip-flop	WSA
Delay	1.67ns	1.51ns
Power	1.024 W	0.095W
Gate count	18	16

From the table we observe that the existing system uses flip-flop architecture and the proposed system uses WSA architecture. Various parameters obtained for both existing and proposed values are also tabulated.

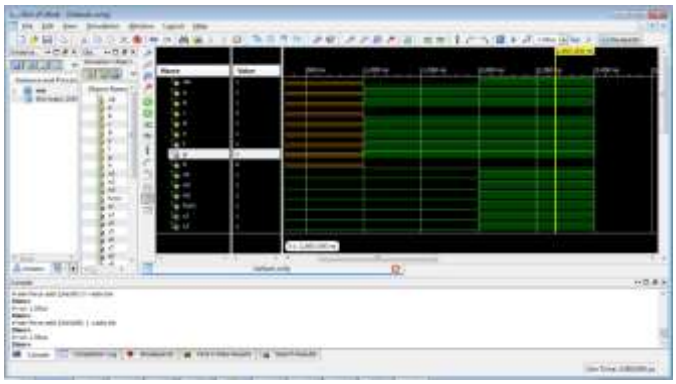

Fig :4 output waveform obtained

From fig:4 The simulation result is obtained by the WSA technique. The above waveform is obtained by giving various inputs for D flip-flops, which are represented as the variables such as a,b,c,d,e,f,g,h.The inputs are 1's and 0's.The output is drawn from the 'func'.

If the input values are assigned in the program then the undefined states do not occurs. Here the input values are not assigned in the program so the undefined state occurs initially those are represented in the redlines in the waveform shown above.

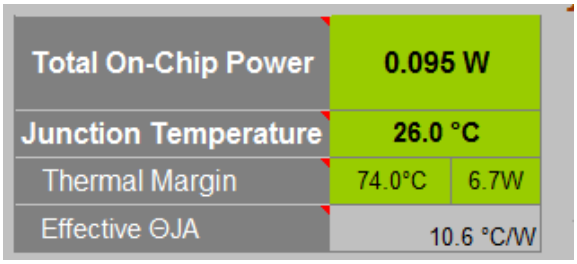

Fig: 5 Power report

From fig :5 The total power can be drawn automatically by including the values of LUTs and BRAM values in the power estimator. The power value is obtained as 0.095W by the WSA technique. The LUT value is 6 and BRAM value is 13, these values are observed from the design summary.

VII. CONCLUSION

The clock gating architecture is mainly used to control and generate any type of combinational architecture in real world application. The new technique called Wide spread adapting clock gating technique is proposed and implemented by using bench mark circuit. The proposed methodology produces better results than the existing methodology in power consumption level and delay time. The existing methodology uses flip-flop architecture; here the power consumption and delay time is larger. The proposed system reduces the number of logical block count using WSA method. The delay value have reduced from 1.67ns to 1.55ns.The gate count value reduces from 18 to 11.The power consumption value have improved as 0.095W from 1.024W.Thus it shows that the proposed methodology produces better results than existing method.

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