DESIGN of AREA OPTIMISED BCD MULTIPLIER USING VHDL

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Abstract: **Decimal multiplication is one of the most frequent operations used by many financial, business and user-oriented applications but current implementations in FPGAs are very inefficient in terms of both area and latency when compared to binary multipliers. In this paper we present a new method for implementing BCD multiplication more efficiently than previous proposals in current FPGA devices with 6-input LUTs. In particular, a combinational implementation maps quite well into the slice structure of the Xilinx Virtex-5/Virtex-6 families and it is highly pipeline-able. The synthesis results for a Virtex-6 device indicate that our proposal outperforms the area and latency figures of previous implementations in FPGAs.**

I-Introduction

A fundamental operation for any hardware implementation of decimal arithmetic is multiplication, which is integral to the Decimal computer arithmetic and is preferred in the environments of decimal data processing such as scientific, commercial, financial and Internet-based applications. The increasing needs for processing power, required by applications with intensive decimal arithmetic, cannot be met by conventional decimal arithmetic which has been, often until lately, implemented by three to four times slower software simulation on binary processors. However, hardware implementations as an integral part of recently commercialized general purpose processors have recently gained more popularity. Binary-coded decimal (BCD) encoding of decimal digits has conventionally dominated decimal arithmetic algorithms, whether realized by hardware or in software.

An important and frequent operation in many applications is decimal multiplication. It is complex to implement in hardware due to the larger range of decimal digits ([0, 9]) and the inefficiency of binary codes to represent decimal values, so that decimal multipliers have lower performance and larger area than comparable binary multipliers. For example, because of the high-area requirements of a pipelined parallel implementation, decimal multiplication in IBM Power6 and Z/system high-end processors [2], [3] is performed serially using a BCD (Binary Coded Decimal) carry-propagate adder and hardware assists. Several decimal serial and parallel multipliers have been proposed for ASIC [5], [6] and FPGA [7] platforms. FPGA implementations are generally based on techniques originally developed for VLSI architectures. The special built-in characteristics of FPGA architectures [2] make it difficult to use many well-known methods to speedup computations (for example, carry-save and signed-digit arithmetic's). Therefore, beyond adapting existing techniques we explore new decimal multiplication algorithms more suitable for FPGAs.

There are two major challenges to design BCD multiplier: firstly, Binary to BCD converter and second, the multiplication process. So we are considering these challenges, a high speed modified BCD to binary converter has been proposed in this paper, which is more efficient and logically correct as the proposed implementation in [6,8]. Vertical-cross process is used to increase efficiency of multiplication on hardware and divide and conquer approach is introduced for multi-digit multiplication with it.

II-Literature work

Arvind Kumar Mehta, Mukesh Gupta, High Performance Vedic BCD Multiplier and Modified Binary to BCD Converter, IEEE 2013, In this paper they have proposed two different algorithms: one for binary to BCD conversion and another for NxN Vedic BCD multiplication and synthesized results of Vedic 2x2 BCD multiplier depicts it's efficiency in terms of slices and time of delay Now, this paper will boost the on-going research of the scholars in the field of decimal arithmetic. they also said that they can implement circuitry of decimal Division

using *straight division methods*, multi-precision decimal square root using the *Dwandwa square-root algorithm*, decimal cube root using *Vedic cube root technique*; which are used simple multiplication and division. At last, Decimal Square and cube by using *Duplex property* and *Anurupya Sutra* of ancient Indian Vedic mathematics. These methods are mainly proposed only for the BCD number system; not for the binary system.

Carlos Eduardo Minchola Guardia, IMPLEMENTATION OF A FULLY PIPELINED BCD MULTIPLIER IN FPGA, IEEE, 2012 their paper has reassessed several implementations of N-x M-digit multiplications on Xilinx FPGAs. This work presents the design of several BCD multipliers and their implementations on Virtex-6 FPGA. Previous techniques and designs proposed are analyzed to carry out performance comparison in terms of area-delay. Their proposed pipelined multiplication is based on a multiplier operand coded into SD radix-10 recoding. A parallel generation of decimal partial products is reduced by carry save adder techniques and decimal adders

III-Method adopted

Figure one shows a flow of proposed work as can be seen there are three major modules which has been developed very first a BCE to binary and also a Binary to BCD convertors requires the actual modification is been proposed in all these conversion methods also the method adopted for multiplication also new digit A and B multiplication using vertical-cross method.

Step 1: Multiply the numbers in the one's place and put the product directly under the ones. (A(LSB half) *B(LSB half))

Step 2: Cross multiply, we would form fractions by taking the top number's tens digit multiplied by the bottom number's ones place. Then take the top number's tens place multiplied by the bottom number's tens place. Add both products. {(A(LSB half) *B(MSB half))+ (A(MSB half) *B(LSB half))}

Step 3: Multiply again, the numbers in the tens place and place the answer to the left of the previous step's answer. (A(MSB half) *B(LSB half))

Step 4: Add all the partial products with previous step's carry if it is.

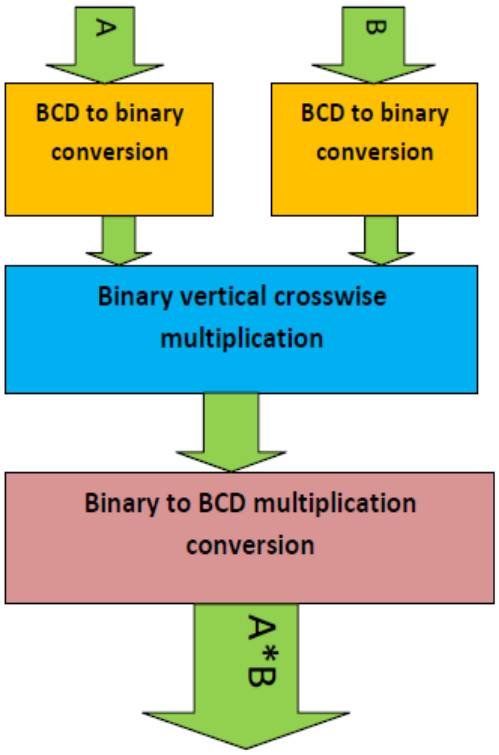

Figure 1: the proposed BCD multiplication module

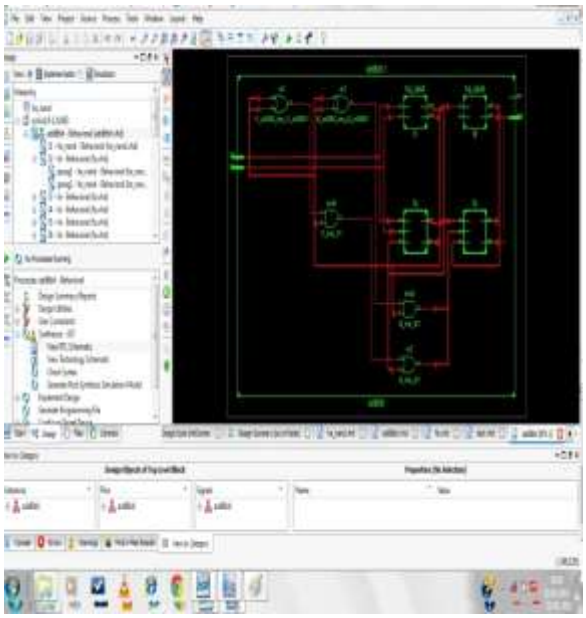

Figure 2: RTL schematic of BCD adder

The 8 bit BCD adder also been developed with a optimised and modified addition structure technique

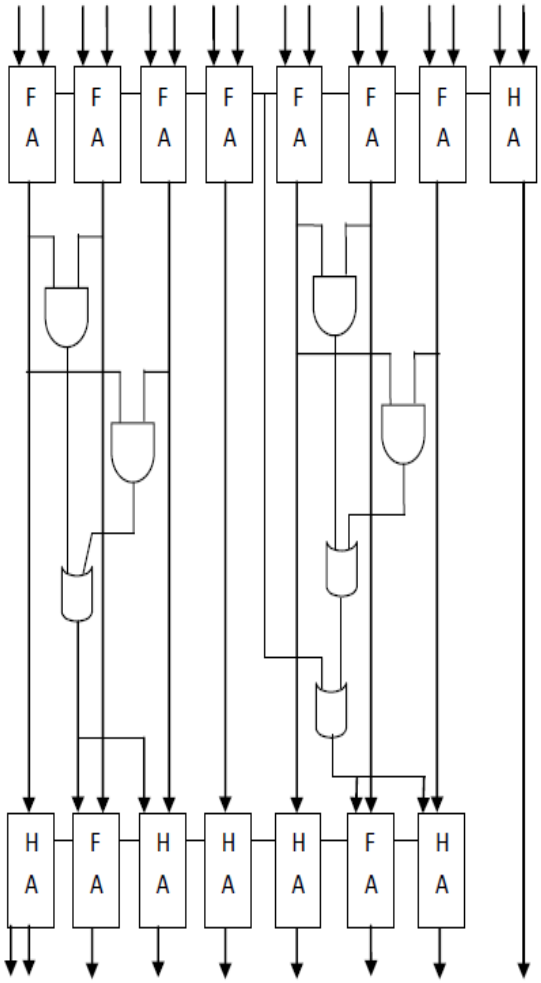

Figure 3: proposed BCD adder

The 3 shown above is our proposed BCD adder and as can be seen we have reduced many adders in it and so it is area optimised.

IV-Results

Till now proposed paper work has successfully design the 8 bit BCD adder which will further used in 8 bit BCD multiplication and the RTL schematic of proposed 8 bit BCD adder is shown in figure 2

Figure 4 below shows the synthesis report of proposed BCD adder

Figure 5 below shows the simulation of proposed BCD adder the simulation is been observed for many test input scenario but present only for few in the figure 5.

Figure 4: synthesis report of BCD adder

Figure 5: simulation of proposed BCD adder

V- Conclusion

In this paper we have proposed two different algorithms one for BCD adder and another for NxN vertical and crosswise BCD multiplication and synthesized results of 8+8 BCD adder depicts its efficiency in terms of slice and time of delay. This paper has reassessed several implementations of NxM-digit multiplications on Xilinx FPGAs. This work presents the design of several BCD multipliers and their implementations on Virtex-6 FPGA.

In next work we will used the proposed BCD adder for designing an 8 bit BCD multiplication.

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