Single Phase Seven-Level Inverter for Grid Connected Systems using PWM Technique

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***Abstract* – This paper presents a single-phase seven-level inverter for grid-connected systems using the pulse width-modulation (PWM). Battery storage systems are connected together in parallel configuration to a seven-level inverter to produce output voltages in seven levels: V_{dc},$2V_{dc}/3$,$V_{dc}/3$,0,$-V_{dc}$,$-2V_{dc}/3$ and-$V_{dc}/3$.The proposed inverter topology uses three reference signals instead of one to generate PWM signals for the switches. The reference signals V_{ref1},V_{ref2} and V_{ref3} are identical to each other except for an offset value that is equivalent to the amplitude of the carrier signal $V_{carrier}$. A Proportional-Integral (PI) current control scheme is employed to keep the output current sinusoidal and to have high dynamic performance to maintain the power factor at near unity. Simulation results are presented to validate the proposed inverter configuration.**

***Keywords*:**multi level inverter**,** pulse width-modulated (PWM) inverter**,** proportional-integral current control.

I. INTRODUCTION

Power-electronic inverters are becoming popular for various industrial drives applications. In recent years also high-power and medium-voltage drive applications have been installed. To overcome the limited semiconductor voltage and current ratings, some kind of series and/or parallel connection will be necessary. Due to their ability to synthesize waveforms with a better harmonic spectrum and attain higher voltages, multi-level inverters are receiving increasing attention in the past few years. The multilevel inverter was introduced as a solution to increase the converter operating voltage above the voltage limits of classical semiconductors. The multilevel voltage source inverter is recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output. The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources. The so-called multi level starts from three levels. As the number of levels reach infinity, the output THD (Total Harmonic Distortion) approaches zero. The number of the achievable voltage levels, however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout, and packaging constraints. Multilevel inverters synthesizing a large number of levels have a lot of merits such as improved output waveform, a smaller filter size, a lower EMI (Electro Magnetic Interference), and other advantages. The principle advantage of using multilevel inverters is the low harmonic distortion obtained due to the multiple voltage levels at the output and reduced stresses on the switching devices used. Improvements in fast switching power devices have led to an increased interest in voltage source inverters (VSI) with pulse width modulation control (PWM).It is generally accepted that the performance of an inverter, with any switching strategies, can be related to the harmonic contents of its output voltage. Power electronics researchers have always studied many novel control techniques to reduce harmonics in such waveforms. Up-to-date,there are many techniques, which are applied to multilevel inverter topologies. Pulse Width Modulation (PWM) is widely employed to control the output of static power inverters. The reason for using PWM is that they provide voltage and/or current wave shaping customized to the specific needs of the application under consideration. It is lastly performance and cost criteria which determines the choice of a PWM method in a specific application. PWM inverters can control their output voltage and frequency simultaneously. And also they can reduce the harmonic components in load currents. These features have made them power candidate in many industrial applications such as variable speed drives, uninterruptible power supplies, and other power conversion systems. However, the reduction of harmonic components in output currents is still the focus of major interest to alleviate the influences of electromagnetic interferences or noise and vibrations.

In general, neutral point clamped PWM three-phase inverter which uses four switching elements in each arm has the five-level voltage waveforms that results in considerable suppression of the harmonic currents comparing with the conventional full-bridge type three-level PWM inverters. However, this is not the case of single-phase PWM inverter. In these days, the popular single-phase inverters adopt the full-bridge type using approximate sinusoidal modulation technique as the power circuits. The output voltage of them has three values: zero, positive and negative supply dc voltage levels. Therefore, the harmonic components of their output voltage are determined by the carrier frequency and switching functions. Moreover, the harmonic reduction of them is limited to a certain degree.

The proposed single-phase Seven-level PWM inverter whose output voltage has Seven values: zero, Quarter, half and full supply dc voltage levels (positive and negative, respectively), so called a Seven level single-phase PWM inverter. The inverter can reduce the harmonic components compared with that of traditional full-bridge five-level PWM inverter under the condition of identical supply dc voltage and switching frequency. Operational principles and switching functions are analysed. The proposed inverter improves the dynamic performances. To assess the proposed inverter, it is compared with the conventional single-phase Five-level PWM inverter under the conditions of identical supply dc voltage and switching frequency. Simulation results are presented to verify the validities of the proposed inverter.

II. CONVENTIONAL FIVE LEVEL H - BRIDGE INVERTER

Multi level inverters are increasing the output voltage magnitude and reduce the output voltage and current harmonic content. Many different strategies for the multi level Pulse Width Modulation (PWM) exist. Usually the modulator is chosen to match the hardware topology. However the choice does not always correspond to the PWM strategy with generates the least harmonic content. This least harmonics PWM strategy can be used for all hardware topologies.Multi level PWM inverters, (including five level inverters), have significant operational advantage such as the ability to drive a motor with nearly sinusoidal current waveforms and at high output voltages.

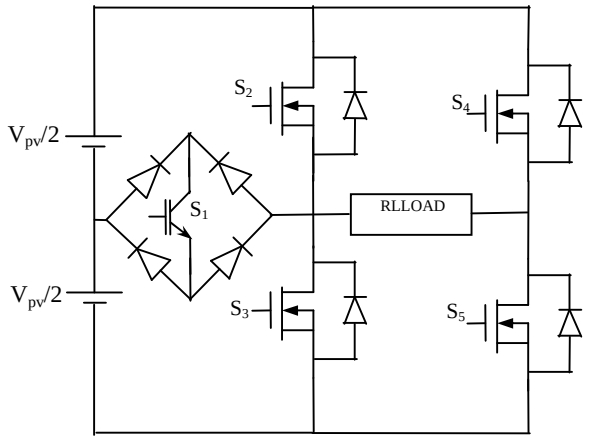

Fig. 1.Single-phase five level inverter

2.1. Operating Principle:

The operating principle of the conventional inverter is to generate five output voltage levels is shown in figure.1, i.e. ,0, $+V_{pv/2}$, $+V_{pv}$,$-V_{pv/2}$, $-V_{pv}$. An auxiliary circuit consists of four diodes and a switch S4 is used between the dc-bus capacitors and the full bridge inverter. Proper switching control of the auxiliary circuit can generate half level of PV supply voltage, i.e., $+V_{pv/2}$ and $-V_{pv/2}$. Two reference signals V_{ref1} and V_{ref2} will take turns to be compared with the carrier signal at a time. If V_{ref1} exceeds the peak amplitude of the carrier signal $V_{carrier}$, then V_{ref2} will be compared with the carrier signal until it reaches zero. At this point onward, V_{ref1} takes over the comparison process until it exceeds $V_{carrier}$.Switches S1-S3 will be switching at the rate of carrier switching frequency, while S4and S5 will operate at a frequency that is equivalent to the fundamental frequency. The table.1 illustrates the level of V_{inv} during S1-S5 switch on and off.

Table.1. Inverter Output Voltage during S1-S5 Switch on and off

S_1	S_2	S_3	S_4	S_5	V_{inv}
ON	OFF	OFF	OFF	ON	$+V_{pv/2}$
OFF	ON	OFF	OFF	ON	$+V_{pv}$
OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	0
ON	OFF	OFF	ON	OFF	$-V_{pv/2}$
Off	OFF	ON	ON	OFF	$-V_{pv}$

Hence the circuit topology might be preferred not only under the aspect of harmonic content reduction due to several level of the output voltage as an essential feature of multi level scheme but also under the aspect of full utilization of semiconductor device incase that high voltage of dc-link could be applied.

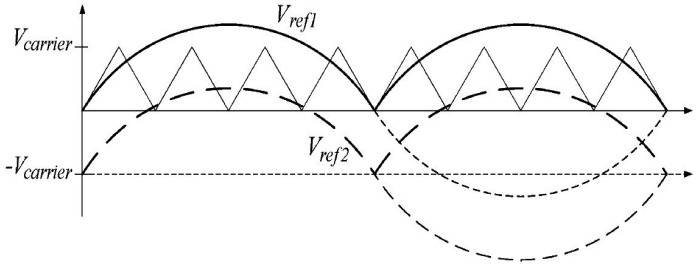

Fig. 2.PWM Pulse generation with 2 reference waves

The five level inverter has very simple commutation sequence which could make it possible to freely change output phase voltages between arbitrary two voltage levels, requiring no additional commutating circuitry. Commutation procedure between some levels should be divided into each one level communication of unit change of voltage in order to guarantee voltage stress of both main switches and main diodes with in unit level voltage during transient time. One level communication can be carried out by first turning off the most upper (lower) main switch in one state and turning on the opposite lower (upper) main switch in off state after a required dead time. It should be noted that such communication sequence facilitates utilization of switching devices even with different turn off times.

III.SIMULINK MODEL OF THE CONVENTIONAL FIVE LEVEL INVERTER

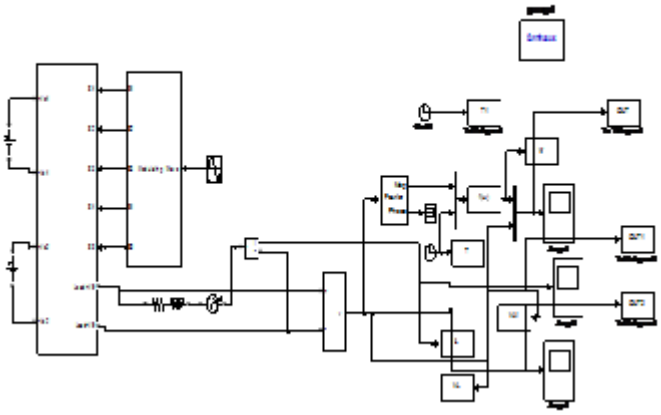

Fig.3. Overall Simulink Diagram of Five-Level Inverter

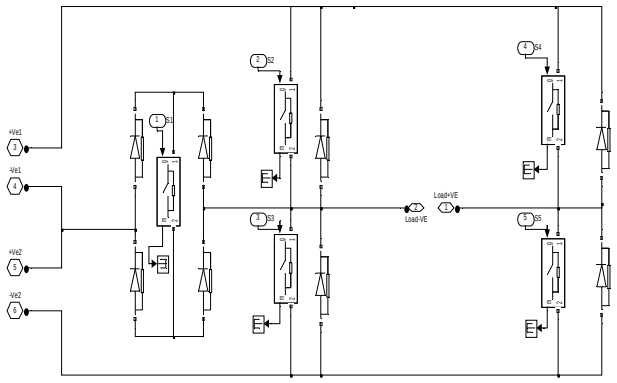

Fig.4. Simulink Diagram of Five-Level H-Bridge Inverter Circuit Diagram

3.1.Switching Strategy:

Simulations were performed by using MATLAB/Simulink to verify that the proposed inverter can practically be implemented in a PV system. It helps one to confirm the PWM switching strategy for the five-level inverter. Then, this strategy can be implemented in a real-time environment, i.e., the DSP to produce PWM switching signals for the switches.Fig.5 shows the way the PWM switching signals are generated by using two reference signals and a triangular carrier signal. The resulting PWM signals for switches *S*1–*S*5 are shown in Fig. 6 (a)–(e).

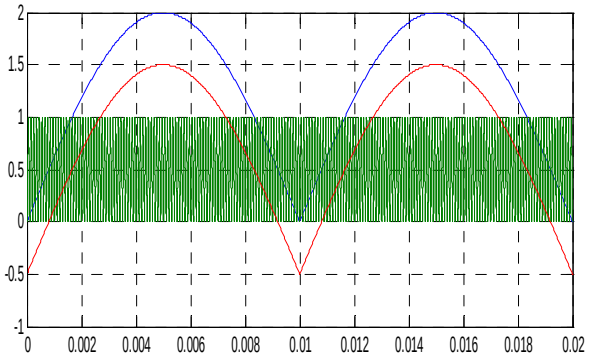

Fig.5. PWM Signal Generation

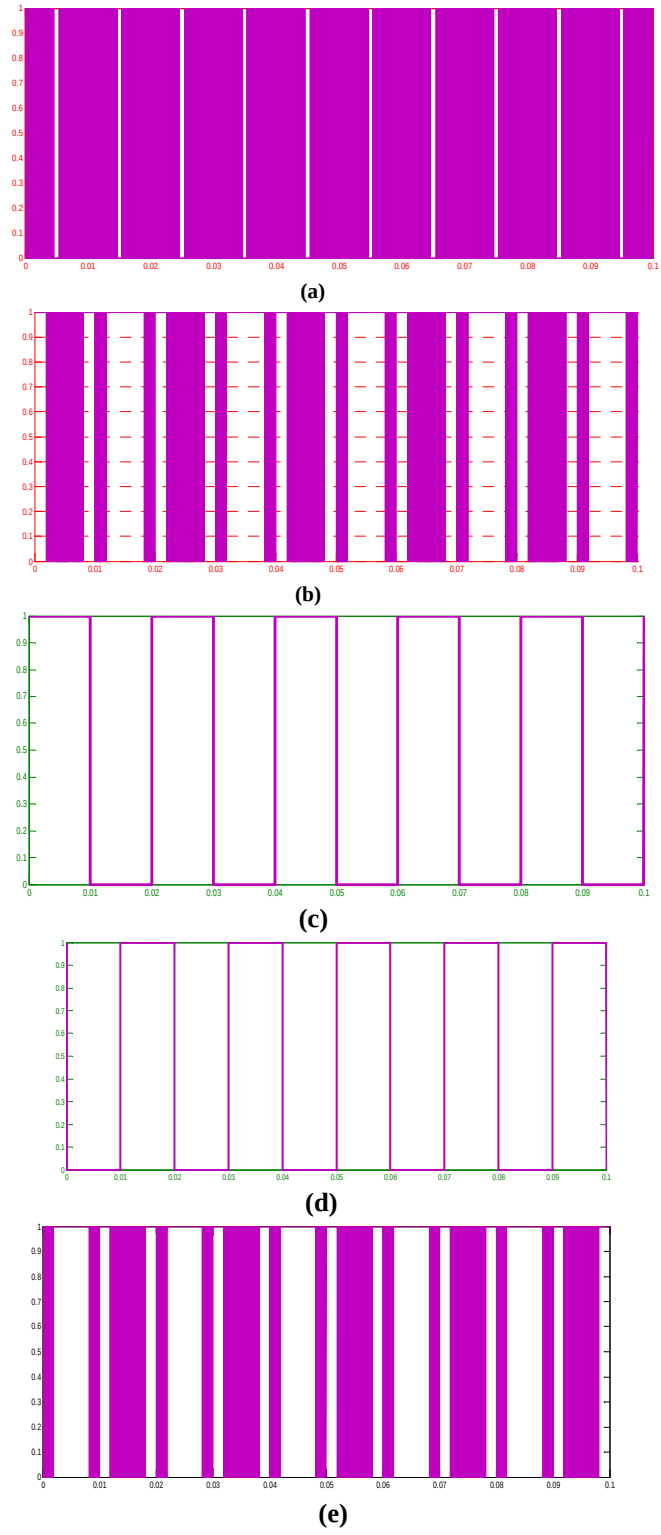

Fig.6. Pulses for H-Bridge Inverter PWM Switches (a) S1, (b) S2,(c) S3,(d) S4,(e) S5.

IV.PROPOSED SEVEN LEVEL H-BRIDGE INVERTER

4.1.Introduction:

As the world is concerned with fossil-fuel

exhaustion and environmental problems caused by conventional power generation, renewable energy sources, particularly solar and wind energy, have become very popular and demanding. Photovoltaic (PV) sources are used today in many applications because they have the advantages of being maintenance and pollution free. Solar-electric-energy demand has grown consistently by 20%–25% per annum over the past 20 years, which is mainly due to the decreasing costs and prices. This decline has been driven by the following: 1) an increasing efficiency of solar cells; 2) manufacturing-technology improvements; and 3) economies of scale. A PV inverter, which is an important element in the PV system, is used to convert dc power from the solar modules into ac power to be fed into the grid.

A single-phase grid-connected inverter is usually used for residential or low-power applications of power ranges that are less than 10 kW. Types of single-phase grid-connected inverters have been investigated . A common topology of this inverter is full-bridge three-level. The three-level inverter can satisfy specifications through its very high switching, but it could also unfortunately increase switching losses, acoustic noise, and level of interference to other equipment. Improving its output waveform reduces its harmonic content and, hence, also the size of the filter used and the level of electromagnetic interference (EMI) generated by the inverter's switching operation. Multilevel inverters are promising; they have nearly sinusoidal output-voltage waveforms, output current with better.

Various topologies for multilevel inverters have been proposed over the years. Common ones are diode-clamped, flying capacitor or multicell, cascaded H-bridge, and modified H-bridge multilevel. This project recounts the development of a novel modified H-bridge single-phase multilevel inverter that has two diode embedded bidirectional switches and a novel pulse width modulated (PWM) technique. The topology was applied to a grid-connected photovoltaic system with considerations for a maximum-power-point tracker (MPPT) and a current-control algorithm.

4.2. Proposed seven level H-bridge MLI:

The proposed single-phase seven-level inverter was developed from the five-level inverter. It comprises a single-phase conventional H-bridge inverter, two bidirectional switches, and a capacitor voltage divider formed by *C*1, *C*2, and *C*3, as shown in Fig.7. The modified H-bridge topology is significantly advantageous over other topologies, i.e., less power switch, power diodes, and less capacitor for inverters of the same number of levels. Photovoltaic (PV) arrays were connected to the inverter via a dc–dc boost converter. The power generated by the inverter is to be delivered to the power network, so the utility grid, rather than a load, was used. The dc–dc boost converter was required because the PV arrays had a voltage that was lower than the grid voltage. High dc bus voltages are necessary to ensure that power flows from the PV arrays to the grid. A filtering inductance *Lf* was used to filter the current injected into the grid. Proper switching of the inverter can produce seven output votage levels (V_{dc},$2V_{dc}/3$,$V_{dc}/3$,0,$-V_{dc}$,$-2V_{dc}/3$,$-V_{dc}/3$) from the dc supply voltage.

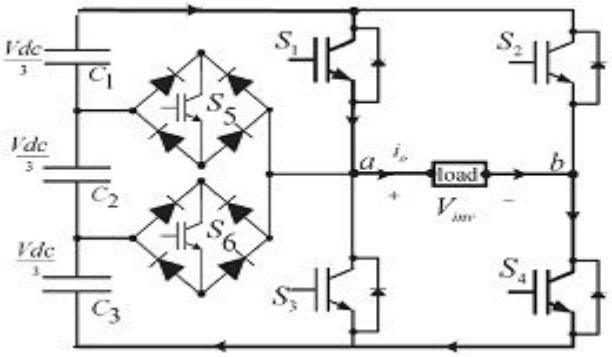

Fig.7.Proposed 7-Level H-Bridge Inverter

4.3. MODES OF OPERATION:

The required seven levels of output voltage were generated as follows.

1) Maximum positive output (V_{dc}): S1 is ON, connecting the load positive terminal to V_{dc}, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is V_{dc}. Fig.7.1 shows the current paths that are active at this stage.

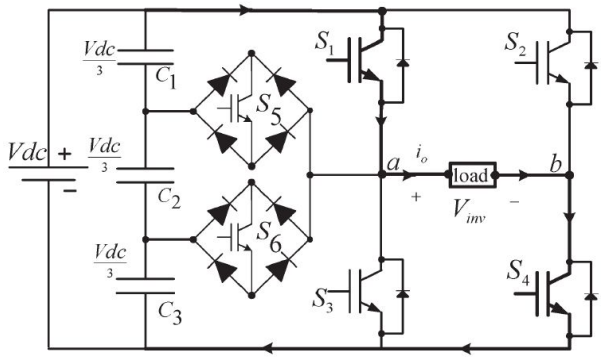

Fig.7.1. Switching combination required to generate the output voltage $V_{ab} = V_{dc}$

2)Two-third positive output ($2V_{dc}/3$): The bidirectional switch S5 is ON, connecting the load positive terminal and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; thevoltage applied to the load terminals is $2V_{dc}/3$. Fig.7.2.shows the current paths that are active at this stage.

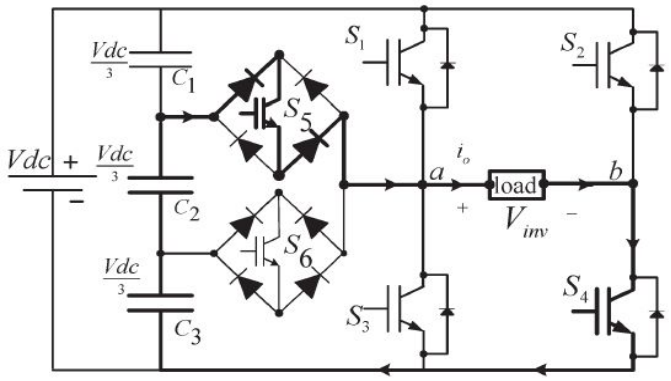

Fig.7.2. Switching combination required to generate the output voltage $V_{ab} = 2V_{dc}/3$

3) One-third positive output ($V_{dc}/3$): The bidirectional switch S6 is ON, connecting the load positive terminal ,and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $V_{dc}/3$. Fig.7.3 shows the current paths that are active at this stage.

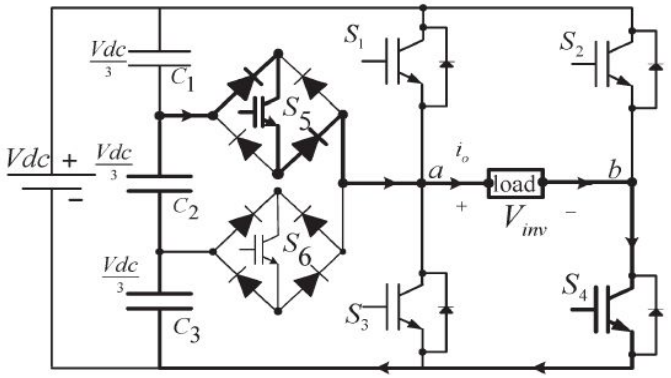

Fig.7.3. Switching combination required to generate the output voltage $V_{ab} = V_{dc}/3$

4) Zero output: This level can be produced by two switching combinations; switches S3 and S4 are ON, or S1 andS2 are ON, and all other controlled switches are OFF; terminal ab is a short circuit, and the voltage applied to the load terminals is zero. Fig.7.4. shows the current paths that are active at this stage.

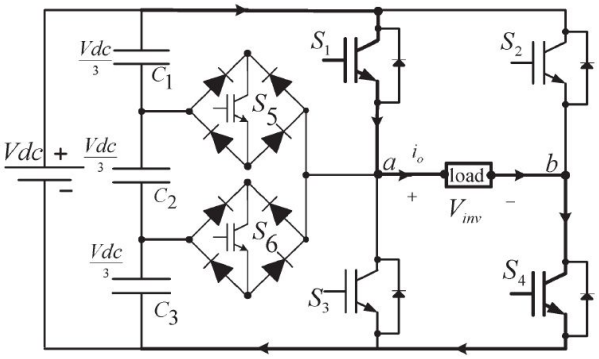

Fig.7.4. Switching combination required to generate the output voltage $V_{ab} = 0$

5)One-third negative output ($-V_{dc}/3$): The bidirectional switch S5 is ON, connecting the load positive terminal, and S2 is ON, connecting the load negative terminal to V_{dc}. All other controlled switches are OFF; the voltage applied to the load terminals is $-V_{dc}/3$. Fig.7.5. shows the current paths that are active at this stage.

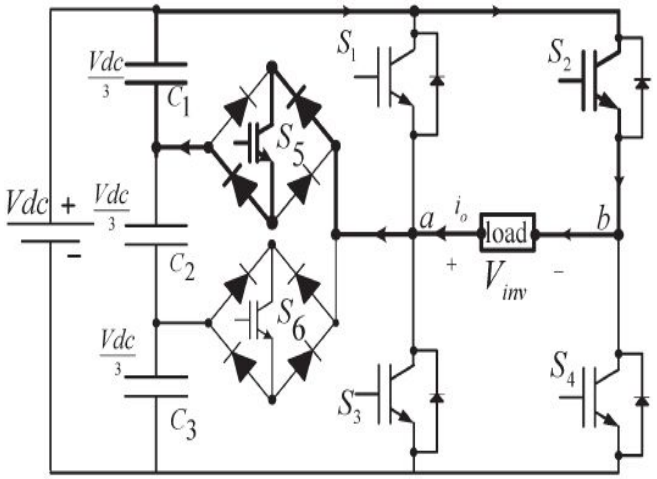

Fig.7.5. Switching combination required to generate the output voltage $V_{ab} = -V_{dc}/3$

6) Two-third negative output ($-2V_{dc}/3$): The bidirectional switch S6 is ON, connecting the load positive terminal, and S2 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $-2V_{dc}/3$. Fig.7.6.shows the current paths that are active at this stage.

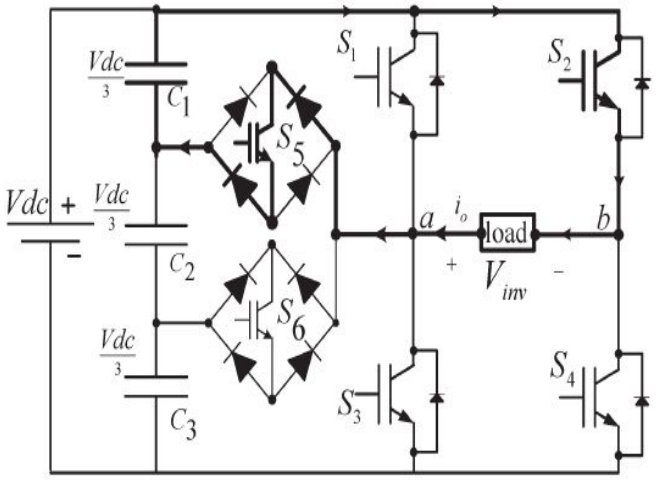

Fig.7.6.Switching combination required to generate the output voltage $V_{ab} = -2V_{dc}/3$

7) Maximum negative output ($-V_{dc}$): S2 is ON, connecting the load negative terminal to Vdc, and S3 is ON, connecting the load positive terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $-V_{dc}$. Fig.7.7. shows the current paths that are active at this stage.

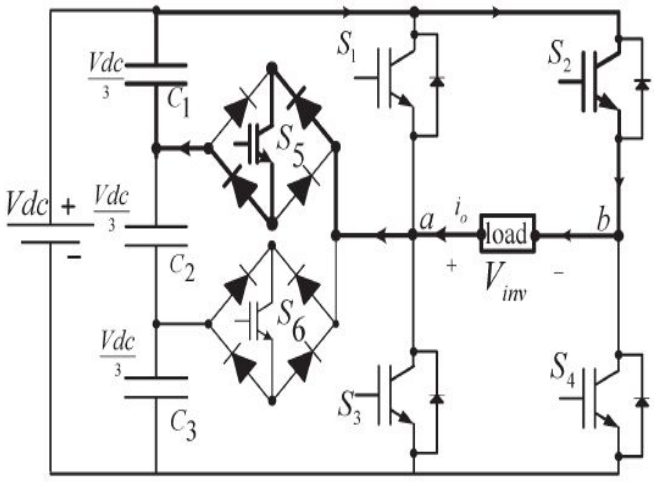

Fig.7.7. Switching combination required to generate the output voltage $V_{ab} = -V_{dc}$

Table 2 shows the switching combinations that generated the seven output-voltage levels ($0, -V_{dc}, -2V_{dc}/3, -V_{dc}/3, V_{dc}, 2V_{dc}/3, V_{dc}/3$).

v_0	S_1	S_2	S_3	S_4	S_5	S_6
V_{dc}	on	off	off	on	off	off
$2V_{dc}/3$	off	off	off	on	on	off
$V_{dc}/3$	off	off	off	on	off	on
0	off	off	on	on	off	off
0*	on	on	off	off	off	off
$-V_{dc}/3$	off	on	off	off	on	off
$-2V_{dc}/3$	off	on	off	off	off	on
$-V_{dc}$	off	on	on	off	off	off

Table 2. Output Voltage According to the Switches On–Off Condition

A novel PWM modulation technique was introduced to generate the PWM switching signals. Three reference signals (V_{ref1}, V_{ref2}, and V_{ref3}) were compared with a carrier signal ($V_{carrier}$). The reference signals had the same frequency and amplitude and were in phase with an offset value that is equivalent to the amplitude of the carrier signal. The reference signals were each compared with the carrier signal.

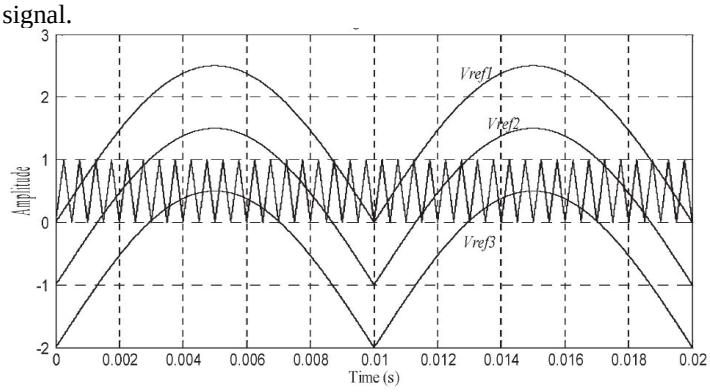

Fig.8. PWM switching signal generation by using three reference signals

If V_{ref1} had exceeded the peak amplitude of $V_{carrier}$, V_{ref2} is compared with $V_{carrier}$ until it had exceeded the peak amplitude of $V_{carrier}$. Then, onward, V_{ref3} would take charge and would be compared with $V_{carrier}$ until it reached zero. Once V_{ref3} had reached zero, V_{ref2}would be compared until it reached zero. Then, onward, V_{ref1} would be compared with $V_{carrier}$. Fig.8. shows the resulting switching pattern. Switches S1, S3, S5,and S6 would be switching at the rate of the carrier signal frequency, whereas S2 and S4 would operate at a frequency that is equivalent to the fundamental frequency.

V.COMPARISION BETWEEN CONVENTIONAL AND PROPOSED SYSTEMS

5.1. Simulation results of conventional five level inverter

One leg of the inverter is operating at a high switching rate that is equivalent to the frequency of the carrier signal, while the other leg is operating at the rate of fundamental frequency (i.e., 50 Hz). The switch at the auxiliary circuit (S1) also operates at the rate of the carrier signal. As mentioned earlier, modulation index M will determine the shape of inverter output voltage V_{inv} and grid current I_g. Fig. 9 - 11 shows the simulation results of V_{inv} and I_g for different values of M.

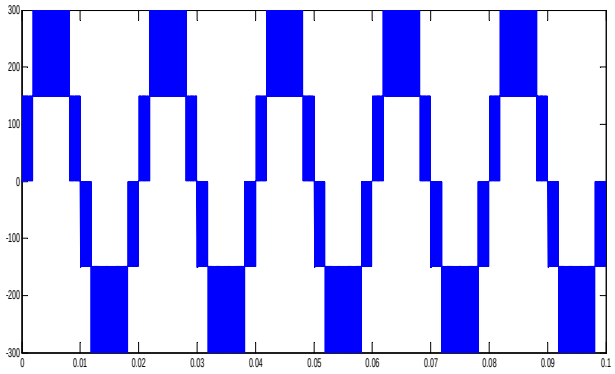

Fig.9. Five Level H-Bridge Inverter Output Voltage

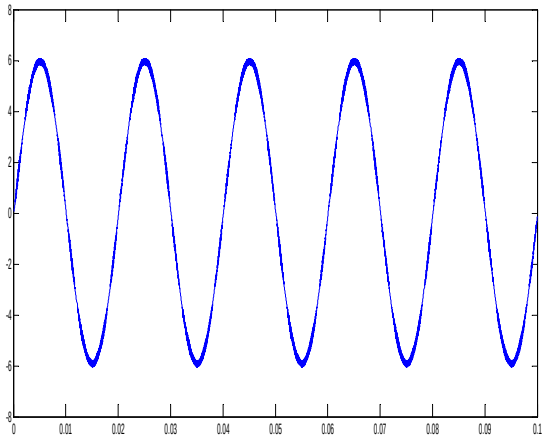

Fig.10. Five Level H-Bridge Inverter Output Current

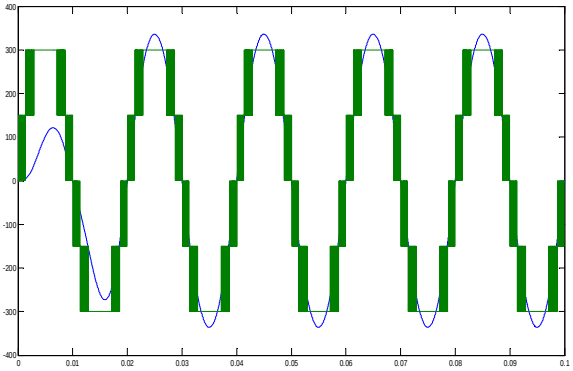

Fig.11. Inverter output voltage (V_{inv}) and grid current (I_g) for V_{inv} for M >1.0

5.2.Simulation results of proposed seven level inverter

Fig. 12-13 shows the simulation results of V_{inv} and I_g for different values of M.

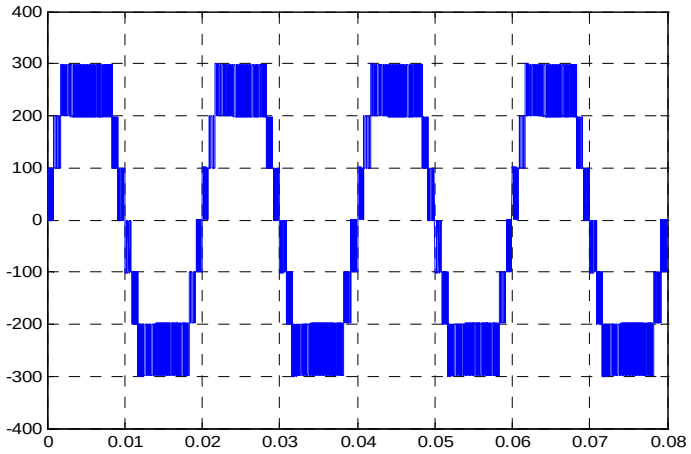

Fig.12.seven Level H-Bridge Inverter Output Voltage

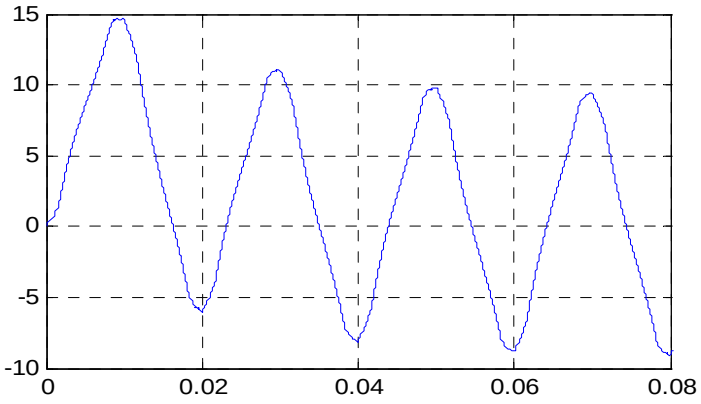

Fig.13.Seven Level H-Bridge Inverter Output Current

VI.CONCLUSION

Multilevel inverters have become an effective and practical solution for increasing power and reducing harmonics of ac waveforms. The main advantages of multilevel PWM inverters are 1) The series connection allows higher voltage without increasing voltage stress on switches.2) Multilevel waveforms reduce the dv/dt at the output of an inverter.3) At the same switching frequency, a multilevel inverter can achieve lower harmonic distortion due to more levels the output waveform in comparison to a single cell inverter. 4) Lower switching losses. 5) Higher voltage capability. 6) Higher power quality. 7) They are 8) The efficiency is very high (>98%) because of the minimum switching frequency 9) They can improve the power quality and dynamic stability for utility systems.10) They are suitable for medium to high power applications. Thus the multi-level inverters are used in various fields.

The simulation results shows that the proposed seven-level PWM inverter has many merits such as reduce number of switches, lower EMI, less harmonic distortion. And the THD of the proposed inverter is considerably alleviated and the dynamic responses are also improved significantly. However the proposed Seven-level inverter involves some advantages over the conventional inverter.

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