HIGH VOLTAGE GAIN BOOST CONVERTER BASED ON THREE- STATE COMMUTATION CELL FOR USING PV PANELS IN A SINGLE CONVERSION STAGE BY R-L LOADS

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Abstract *- **This paper presents a novel high voltage gain boost converter topology based on the three-state commutation cell for battery charging using PV panels and a reduced number of conversion stages. The presented converter operates in zero voltage switching (ZVS) mode for all switches. By using the new concept of single-stage approaches, the converter can generate a DC bus with a battery bank or a photovoltaic (PV) panel array, allowing the simultaneous charge of the batteries according to the radiation level. The operation principle, design specifications, and experimental results from a 500-W prototype are presented in order to validate the proposed structure. The proposed method focuses on a single soft switching non isolated DC-DC converter interconnecting battery charger, photovoltaic panels, and a high gain boost converter. This method aims to reduce the number of conversion stages, thus increasing the converter efficiency and simplifying the control system. The obtained results are discussed and compared to each other. The proposed method is programmed and tested in a standard IEEE distribution system using MATLAB software.***

Keywords – Photovoltaic power systems, Battery chargers, DC-DC power conversion.

I. INTRODUCTION

The increasing use of renewable energy in applications regarding distributed generation systems such as photovoltaic panels, fuel cells, and wind turbines leads power electronics researchers to new challenges. In this kind of application, one of the major concerns is the need of a high output DC voltage bus (from 200 to 400 Vdc), which is necessary to supply inverters, UPS, etc., from low input voltage levels. This issue has lead to the conception new several converter topologies. Nowadays, non-isolated DC-DC converters with high voltage gain have been highlighted in different applications.

The traditional high-frequency isolated converters typically required a transformer responsible for processing the total rated paper, with consequent increase of size, weight, and volume and reduction of efficiency. Converters with switched capacitors develop significant current peaks which limit the efficiency and the maximum processed power. A study on energy-efficiency of switched-capacitor converters was present by the authors presented some design rules useful for developing high-efficiency switched-capacitor converters based on their analysis. It was presented several modular converter topologies based on a switched-capacitor cell concept, a soft-switched scheme was used in order to reduce the switching loss and electromagnetic interference.

In a survey of high step up DC-DC converters based on coupled inductors and multiplier cells are presented and the major challenges were summarized. Some topologies employ coupled inductors, with consequently reduce the voltage stress across the switches, although the input current is discontinuous and the use of an LC filter may be necessary. A voltage doubler rectifier as the output stage of an interleaved boost converter with coupled inductors was presented. The obtained voltage gain is twice that of traditional boost converters due to the doubler stage, as coupled inductors provide additional voltage gain, although voltage stress across the switches is not increased. It was described a cascade high step-up DC-DC converter based on quadratic boost converter with coupled inductor in the second boost converter. A study of a topology based on two for-switch bridges around a LC circuit that does not utilize iron core transformers applied in megawatt level power transfers was presented. If the authors described a high step-up ZVT interleaved boost converter applied to grid connected PV power system. This interleaved boost converter use an active-clamp circuit as the first power processing stage, which can boost a low voltage from PV array which can boost a low voltage from up to the high DC bus. A topology using the boost converter output terminal

and flyback converter output terminal serially connected to increase the output voltage gain with the coupled inductor was presented. A family of high-efficiency, high step-up DC–DC converters with simple topologies was proposed. The proposed converters, use diodes and coupled windings instead of active switches to realize functions similar to those of active clamps, perform better than their active-clamp counterparts. The topology introduced in consists in an interleaved boost converter, where the inductor current ripple and the current stress through the main switches are reduced. Besides, reduction of volume, size and weight is expected because the inductors are designed for twice the switching frequency. The converter presented the uses voltage multiplier cells that allow high voltage step-up with reduced stress regarding the semiconductor elements. The interleaved configuration allows the very reduction of the input inductors and the output capacitors, at the cost of high component count as additional multiplier cells are includes. A similar topology based on the three-state commutation cell was proposed in where the current sharing problem of the interleaved converter can be eliminated.

The converter shown in presents low input current ripple and uses autotransformer with is designed for part of the rated power, while it is possible to achieve high voltage gain with reduced voltage stress across the switch. However, the use of such converter is limited to duty cycle value higher than 0.5. Summarizing, the aforementioned topologies employ such techniques: the use of high frequency transformers, coupled inductors associated with voltage multiplier cells or switched capacitors. Although the development of novel topologies with wide conversion ratio and high efficiency is necessary, their interconnection with photovoltaic panels (PV), battery banks, and the inverters DC link has a great interest for both industry and academy. Within this context, the use of single stage converters, as presented. If they employ a single stage topology to achieve both voltage step-up and DC-AC capabilities. However, in this kind of technique, the semiconductors deal with high voltage and current stresses, as result in low efficiency. Therefore, the interconnection among photovoltaic panels (PV), battery banks, and the inverters DC link is usually achieved by using two or more DC-DC converters Nevertheless in this architecture, the energy flows through many conversion stages. The proposed architecture allows such interconnection in a single stage which was introduced.

This paper deals a single stage soft switching non isolated DC-DC converter interconnecting battery charger, photovoltaic panels, and a high gain boost converter. The proposed topology aims to reduce the number of conversion stages, thus increasing the converter efficiency and simplifying the control system.

II. PROPOSED TOPOLOGY

A. Conception of the topology

In the low voltage side, the bidirectional characteristic of the topology allows the MOSFET bridge to be supplied by either the battery or the PV array. Besides, the use of resonant capacitors in the full-bridge capacitors provides zero voltage switching (ZVS) of the switches. The integrated topology resulting from the boost converter and the three-state switching cell is shown . The main advantage of this topology is the low voltage stress across the active switches, low input current ripple, and simplicity, what results in higher efficiency. Some high voltage gain topologies are supposed to contain three dc links as shown, where VDC_3 feeds the inverter with a higher voltage than that of the remaining ones. According to the proposal, the battery bank and the photovoltaic panel can be connected to the low voltage side at VDC_1 or VDC_2, depending on the available voltage levels.

Considering typical applications under 2 kW, battery bank voltage levels can be 12 V, 24 V, or 48V (in order to avoid the connection of many units in series) and photovoltaic panels can be arranged to establish a dc link with voltage level equal to about twice that of the former link. The proposed topology is formed by one input inductor L_{IN}, four controlled power switches S_1-S_4, two rectifier diodes D_1 and D_2, two transformers T_1 (windings T_{1a} and T_{1b}) and T_2 (windings T_{2a}, T_{2b}, T_{2c} and T_{2d}) and four output capacitors C_1-C_4. Even though additional components are included, current sharing is maintained between (S_1, S_2, T_{1a}, T_{2a}) and (S_3, S_4, T_{1b}, T_{2c}). Then, besides the reduced current stress through the components, the instantaneous current during the turn off of the switches is significantly reduced for D>50%, thus leading to minimized switching losses. Also, the transformer is designed for about only 70% of the total output power.

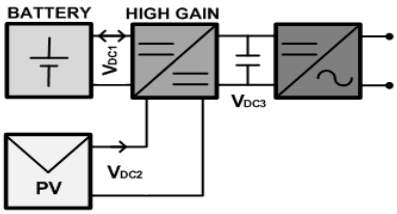

Figure 1:(a) Proposed Architecture

The proposed converter has two operation regions, which work analogously. The duty cycle is applied to the lower switches of each leg (S_2 and S_4), which operate in opposite phase. The converter behavior and the operation region

are defined by the applied duty cycle. If the duty cycle is higher than 50%, the lower switches work in overlapping mode. However, if the duty cycle is lower than 50%, then only the upper switches are in overlapping mode. As the operation principle regarding the switches is analogous, only the case for D>50% is presented.

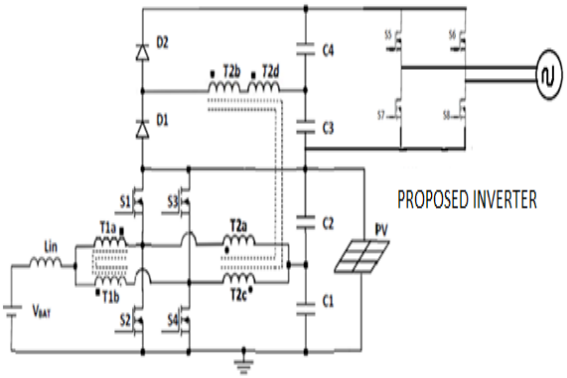

Figure 1:(b) Block Diagram of Proposed System

III. OPERATION OF SIX STAGE CONVERSIONS

The converter presents six operation stages, while presents the theoretical waveforms. As it can be observed, the current through the input inductor has a frequency which is twice higher than the switching frequency, which characterizes the three-state commutation cell behavior. This current is then equally shared between the windings of the autotransformers, which leads to reduced current stresses. The windings T_{2a} and T_{2c} correspond to the transformer primary side, which are responsible for stepping the voltage up and allowing the switches to operate in ZVS mode, increasing the system efficiency.

A. First Stage

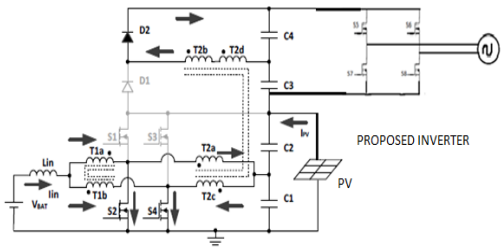

Figure-2(a) First Stage

In First Stage :[t_0 – t_1] - This stage begins when S_1 is turned off, causing a current flow through the anti-parallel diode of switch S_2, allowing the turn on in ZVS mode. At this moment, S_3 is turned off, and S_4 is turned on. The current flowing through the input inductor 'I_{IN}' increases linearly and is equally divided between the two switching cells, reducing the associated stresses of the active semiconductors. The current in the primary side T_{2a} decreases linearly, while the current through T_{2c} increases linearly. This stage ends when the currents in T_{2a} and T_{2c} reach zero, and the current through S_2 is equal to that through S_4.

B. Second Stage

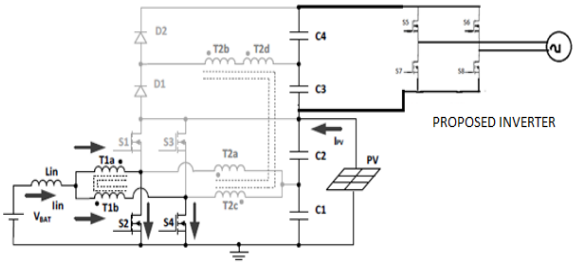

Figure 2:(b) Second Stage

In Second Stage [t_1 – t_2] – Current 'I_{IN}' still increases linearly and is equally divided through the commutation cells. Additionally, all the rectifier diodes are reverse biased. The current through T_{2a} and T_{2c} remains null. This stage ends when S_4 is turned off.

C. Third Stage

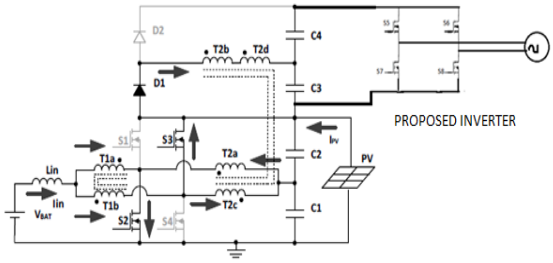

Figure 2(c) Third Stage

In Third Stage [t_2 – t_3] – This stage begins when S_4 is turned off, causing the current to flow through the anti-parallel diode of S_3, allowing the turn on in ZVS mode. At this moment, S_2 is already turned on. The current flowing through the input inductor 'I_{IN}' decreases linearly, while the currents through T_{1a} and T_{1b} increase and decrease linearly, respectively. The current in the primary side T_{2a} decreases linearly, while the current through T_{2c} increases linearly. This stage ends when S_4 is turned on and S_3 is turned off.

D. Fourth Stage

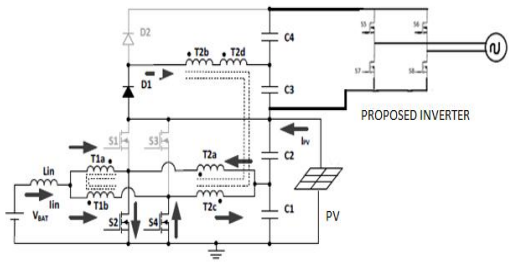

Figure 2:(d) Fourth Stage

In Fourth Stage [$t_3 - t_4$] – This stage begins when S_4 is turned on. When S_2 is turned on, the input current 'I_{IN}' increases linearly, and so do the currents through T_{1a} and T_{1b}. Also, the current through S_4 increases and has flows in the opposite direction. The current through T_{2a} linearly increases, while the one through T_{2c} decreases. This stage ends when the currents in T_{2a} and T_{2c} reach zero, and the current through S_2 is equal to the one in S_4.

E. Fifth Stage

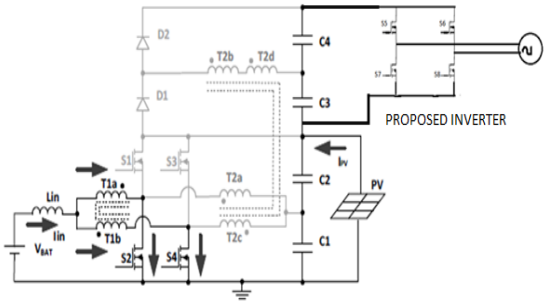

Figure 2:(e) Fifth Stage

In Fifth Stage [$t_4 - t_5$] – This stage is similar to the second one. In this stage, 'I_{IN}' is still increases linearly and is equally divided between the commutation cells. Besides, all the rectifier diodes are reverse biased. The current through T_{2a} and T_{2c} remain null. This stage ends when S_2 is turned off.

F. Sixth Stage

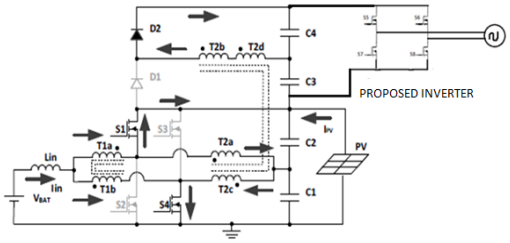

Figure 2:(f) Sixth Stage

In Sixth Stage [$t_5 - t_6$] – This stage begins when S_2 is turned off, causing a current flow through the anti-parallel diode of S_1, allowing its turn on in ZVS mode. At this moment, S_3 is already turned off and S_4 is turned on. The current flowing through the input inductor 'I_{IN}' decreases linearly. The current in the primary side T_{2a} increases linearly, while the current through T_{2c} decreases linearly. This stage ends when the currents through T_{2a} and T_{2c} become null, and the current through S_2 is equal to the one through S_4. After this stage, a new switching cycle begins from the first stage.

IV- EQUIVALENT CIRCUITS USING STATIC GAIN

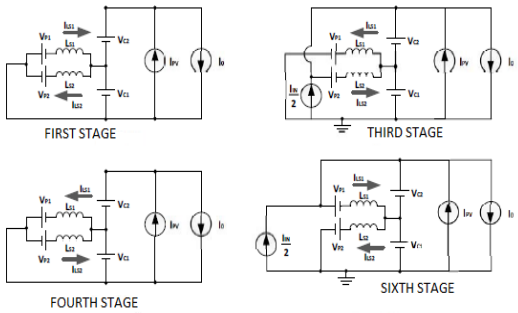

Figure 3:(a) Equivalent Circuits used static gain

D>50%

Considering that the duty cycle is applied to the lower switches, there are two possible operation modes. For D>50%, there is an overlapping period for the lower switches, which remain turned on simultaneously during a certain time interval. On the other hand, for D<50%, there is an overlapping period of the upper switches. Static Gain for D>50% The equivalent circuits from which were derived equations are given below.

The output voltage can be obtained as:

$$V_0=V_{C1}+V_{C2}+V_{C3}+V_{C4} \quad (1)$$

Where,

$$V_{C3}=V_{C4}=n.(V_{P1}+V_{P2})$$

V_{P1} and V_{P2} represent the transformer secondary voltage refluxed on primary side.

Since the voltage across the capacitor C_1 is equal to the voltage across the battery bank, V_{C1} and V_{C2} can be obtained as:

$$V_{C1}=V_{BAT} \quad (2)$$

$$V_{C2}=\frac{D.V_{BAT}}{1-D} \quad (3)$$

From the equations of the currents through the inductors L_{S1} and L_{S2} on the first stage (4), second stage (5), third stage(6) and from the time interval

equations given in (7), the voltage across capacitors C_3 and C_4 can be obtained as(8).

$$\begin{cases} I_{LS1(t)} = I(0) - \left(\frac{V_{C1}+V_{P1}}{L_S}\right).t \\ I_{LS2(t)} = -I(0) + \left(\frac{V_{C1}-V_{P2}}{L_S}\right).t \end{cases} \quad (4)$$

$$I_{LS1}(t) = I_{LS2}(t) = 0 \quad (5)$$

$$\begin{cases} I_{LS1}(t) = \left(\frac{V_{C1}-V_{P1}}{L_S}\right).t \\ I_{LS2}(t) = \left(\frac{V_{C2}-V_{P2}}{L_s}\right).t \end{cases} \quad (6)$$

$$\begin{cases} \Delta_{t1} = \Delta_{t4} = \frac{((1-D).T_s.(n.V_{C1}-V_{C4}+n.V_{C2}))}{V_{C4}} \\ \Delta_{t2} = \Delta_{t5} = -\frac{(T_S.(2.V_{C1}.n.(1-D)-V_{C4}+2.V_{C2}.n.(1-D)))}{2.V_{C4}} \\ \Delta_{t3} = \Delta_{t6} = (1-D).T_s \end{cases} \quad (7)$$

$$V_{C3} = V_{C4} = \frac{n.T_s.V_{BAT}^2}{(1-D).T_s.V_{BAT}+4.I_0.L_S.n} \quad (8)$$

From the previous equations, the static gain can be obtained as:

$$G_{D>50\%} = \frac{V_0}{V_{BAT}} = \frac{1}{(1-D)} + \frac{2.n}{[(1-D)+\alpha]} \quad (9)$$

The static gain depends exclusively on the duty cycle 'D', the transformer turns ratio 'n', and the normalized load current 'α'.

$$\alpha = \frac{4.n.I_0.L_s}{V_{BAT}.T_S} \quad (10)$$

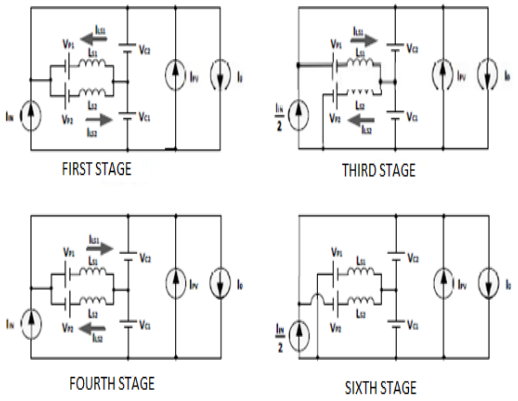

Figure 3(b) Equivalent Circuit used static gain D<50%

The voltages across capacitors C_3 and C_4 for D<50% are given by,

$$G_{D<50\%} = \frac{V_0}{V_{BAT}} = \frac{1}{(1-D)}.\left[\frac{2.n.D^2}{D^2+\alpha.(1-D)}+1\right] \quad (11)$$

$$td_{MIN_{S_{INP}}} = -\frac{\frac{I_{IN}}{2}-\left[\frac{\alpha.D.T_S}{2.L_S.(D+\alpha)}\right]+\sqrt{\left(\frac{I_{IN}}{2}\right)^2-2.\frac{I_{IN}}{2}.\left[\frac{\alpha.D.T_S}{2.L_S.(D+\alpha)}\right]+\left[\frac{\alpha.D.T_S}{2.L_S.(D+\alpha)}\right]^2-4.C_S.V_{P1}.\left[\frac{D.V_{P1}}{2.L_S.(D+\alpha)}\right]}}{\frac{D.V_{P1}}{2.L_S.(D+\alpha)}}$$

(12)

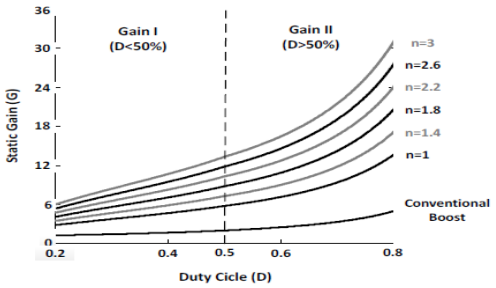

Figure 3:(c) Static gain versus Duty cycle values of 'n'

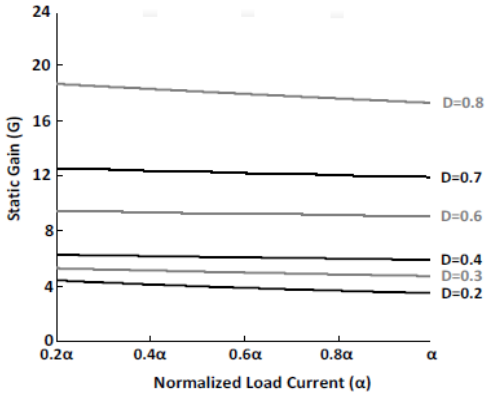

Figure 3:(d) Static gain Vs I_L Values D.

On the other hand, the maximum dead time that allows soft switching depends on the time interval necessary for the current to become zero during the first stage. Then the maximum dead time can be obtained as

$$td_{MAX_{S_{INP}}} = T_{S.\alpha} - \frac{I_{IN}.L_S.(D+\alpha)}{D.V_{PV}} \quad (13)$$

The commutation analysis for the upper switches can be performed analogously, while expression(14) can be easily derived

$$td_{MAX_{S_{SUP}}} = \frac{[T_S.V_{IN}.(D-1).(\alpha-D+1).\left[T_S.V_{IN}.\alpha-4.I_{PV}.L_S.n+\frac{2.T_S.V_{IN}.n.\alpha}{4.n.(D-1)}+\frac{T_S.V_{IN}.\alpha^2}{2.D.(D+\alpha}\right.}{V_{IN}.T_S.\alpha}$$

(14)

V-A- PROPOSED CONVERTER CONTROL

The strategy described it can be used in the proposed converter, where it is necessary to measure only three quantities that are the PV panel voltage (V_{PV}), the PV panel current (I_{PV}), and the voltage across the battery bank (V_{BAT}).

Let us suppose that constant power is supposed to be injected in the inverter stage. Considering that the battery has low charge, the MPPT can be performed in any radiation and output power condition. The power difference is naturally transferred to or from the battery and the inverter can easily support the resulting dc bus voltage variation. If the battery is fully charged, the MPPT is not performed and the operation point is changed until the current through the battery becomes zero.

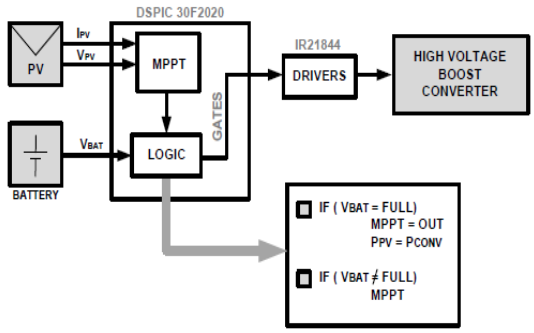

Figure 4:(a) Control Strategies of proposed converter

As it can be observed, the current through the input inductor has a frequency which is twice higher than the switching frequency, which characterizes the three-state commutation cell behavior.

B-SOFT-SWITCHING CONDITION

This section presents the analysis of minimum and maximum dead times necessary to obtain the soft-switching condition for the switches. In order to obtain soft switching, the leakage inductance of the transformer and the intrinsic capacitance of the switches are considered. Then, presents the equivalent circuit during the equivalent circuit during the turn off time of switch S_2. where it can be seen that the sum of such quantities gives the output voltage. This result also shows good voltage sharing across the output capacitors. This issue has to the conception new several converter topologies.

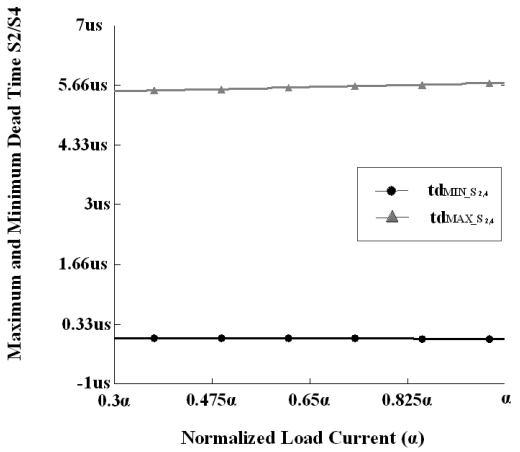

Figure 4:(b) Soft Switching condition for lower switches

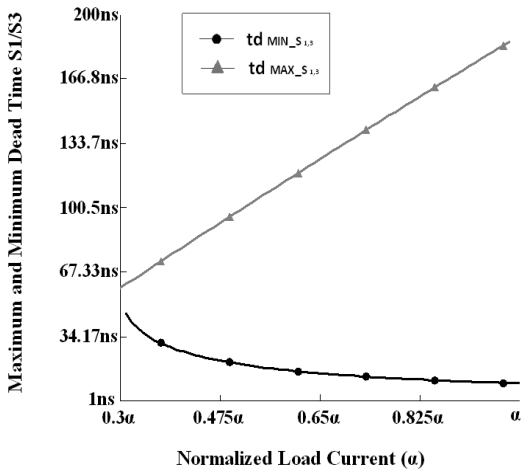

Figure 4:(c) Soft Switching condition for upper switches

It shows the soft-switching condition for the upper and lower switches by varying with the normalized load current and for different values of duty cycle. From this figure, it can be observed that the duty cycle variation plays a small role in the commutation condition if compared with the switching interval.

C-EXPERIMENTAL RESULTS

This section presents the higher order experimental results obtained from the converter operating in rated power condition. It presents the voltages across the output capacitors, where it can be seen that the sum of such quantities gives the output voltage. This result also shows good voltage sharing across the output capacitors.

It presents the voltage and the current through S1, where the operation ZVS mode is noticed. As it can be seen the conduction of the

body diode can be avoided as S1 and S3 are used as synchronous rectifiers what reduce losses. Switch S3 presents the same behavior, although the waveforms are phaseshifted by 180° .

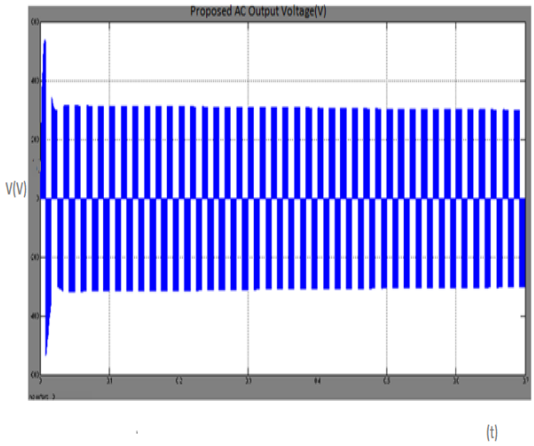

Figure 4:(d) AC Proposed Output Voltage

It presents the voltage and the current through S2, whose operation is complementary to S1. It can be seen that S2 operates in ZVS mode. Also, the current at the instant of the turning off is reduced what favors the turning off behaviour. It presents the open loop converter dynamic behavior, where the bidirectional characteristic between the input voltage sources (batteries and photovoltaic panels) becomes evident. From such waveforms, one can be observe the behavior of the currents through the battery, the panel, and the load Ro, as well as the voltages across the panel and the load when a load step is performed. A current step simulating the insertion of the photovoltaic panel is introduced at 45 ms, while the panel is responsible for supplying most of the energy and charging the batteries. Its current direction is inverted.

VI- CONCLUSIONS

A boost converter with high voltage gain has been presented in this paper. The relevant equations for the design procedure, the operation principle, and the main theoretical waveforms are discussed in detail. The main advantage of the topology is the wide voltage step-up ratio with reduced voltage stress across the main switches. Experimental results obtained from a 500 W prototype have validated the concept, with high efficiency over a wide load range and smaller efficiency at the rated condition (94%), confirming the satisfactory performance of the structure.

Although such curve is satisfactory for PV applications further optimization can be investigated in order to reduce conduction losses and improve efficiency in the rated condition. The concept of integrated converters in a single-stage approach seems to be promising, thus leading to the proposal of additional topologies feasible to photovoltaic and fuel cell applications.

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