An Efficient Low Leakage Current Comparison Based Domino

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Abstract– In this paper we present an efficient current comparison based domino .The presented logic style based on comparison of mirrored current of the pull-up network with its worst case leakage current. This comparison stage employs a clock gated PMOS and NMOS transistors. Thus, the contention current and power consumption and delay are reduced. The Parasitic capacitance on the dynamic node also decreased by yielding a smaller keeper. The simulated data presented is obtained using TANNER EDA tool with 180 nm technology. In terms of power consumption, power delay product and energy delay product, the new current comparison domino offers significant improvement compared to existing logic styles.

Keywords– Domino logic, leakage-tolerant, noise immunity, wide fan-in.

I. INTRODUCTION

In recent years, the power problem has emerged as one of the fundamental limits facing the future of CMOS integrated circuit design. Energy-efficiency is one of the most required features for modern electronic systems designed for high-performance and/or portable applications. As the technology scales down the threshold voltage (V*th*) of the transistor also lowers in the same proportionate. Scaling of threshold voltage results in exponential increase of sub threshold leakage current in the evaluation transistor and makes the domino logic less noise immune. Energy-efficiency is one of the most required features for modern electronic systems designed for high-performance and/or portable applications.

Domino logics are utilized in the digital circuits where high speed and area characteristics are critical. It has many advantages such as high speed operation, minimum used area and power consumption savings. Domino logic overcomes the cascaded problem faced by the dynamic logic gates. Wide fan in domino logic finds a variety of applications in microprocessors, digital signal processors, and dynamic memory. However, in wide fan-in dynamic gates, especially for wide fan-in OR gates [2], robustness and performance significantly degrade with increasing leakage current. As a result, it is difficult to obtain satisfactory robustness performance tradeoffs. Using proposed domino logic wide fan-in OR gate is implemented and simulation results obtained. In wide fan-in gates, the capacitance of the dynamic node is large, speed is decreased dramatically. In addition, noise immunity of the gate is reduced due to many parallel leaky paths in wide gates. Although upsizing the keeper transistor can improve noise robustness, power consumption and delay are increased due to large contention. These problems would be solved if the PDN implements logical function is separated from the keeper transistor by using a comparison stage in which the current of the pull-up network (PUN) is compared with the worst case leakage current. The novelty of the proposed new current-comparison-based domino (CCD) circuit for wide fan-in applications is increases performance and decreases leakage power consumption.

The rest of this paper is arranged as follows. After the literature review in Section II, the proposed circuit is described in Section III. Section IV includes simulation results for the proposed circuit using TANNER EDA tool version compared with other conventional circuits. Section V concludes the results.

II. LITERATURE REVIEW

A literature survey is done for previously available various techniques to know their significance and limitations. Conventional higher fan-in domino OR logic and several other domino circuits proposed in the literature. These circuit techniques can be divided into two categories. In the first category, circuit techniques change the controlling circuit of the gate voltage of the keeper such as conditional-keeper domino (CKD)[5], high speed domino (HSD)[6], leakage current replica (LCR) keeper domino[7], and controlled

keeper by current-comparison domino (CKCCD)[8].In the second category, designs including the proposed designs change the circuit topology of the footer transistor or reengineer the evaluation network such as diode partitioned domino (DPD)[9]. The main goal of these circuit design techniques is improved noise immunity and circuit performance, especially in wide fan-in circuits.

Standard footless domino (SFLD) [4] is a conventional standard domino. A standard footless domino circuit is shown in Fig. 1.In this design, a pMOS keeper transistor is employed to prevent any undesired discharging at the dynamic node due to the leakage currents and charge sharing of the pull-down network (PDN) during the evaluation phase, hence improving the robustness. The conventional feedback keeper uses an inverter and weak pMOS transistor to hold the output high. The keeper ratio *K* is defined as

$$K = \frac{\mu p(\frac{W}{L})\text{Keeper}-\text{transistor}}{\mu n\left(\frac{W}{L}\right)\text{evaluation}-\text{network}} \quad (1)$$

Where *W* and *L* denote the transistor size, and μn and μp are the electron and hole mobilities respectively. However, the traditional keeper approach is less effective in new generations of CMOS technology. Although keeper upsizing improves noise immunity, it increases current contention between the keeper transistor and the evaluation network. Thus, it increases power consumption and evaluation delay of standard domino circuits. These problems are more critical in wide fan-in dynamic gates due to the large number of leaky nMOS transistors connected to the dynamic node. The drawbacks analyzed with the existing works are increase in leakage current, noise immunity, decrease in contention current robustness, power consumption and delay.

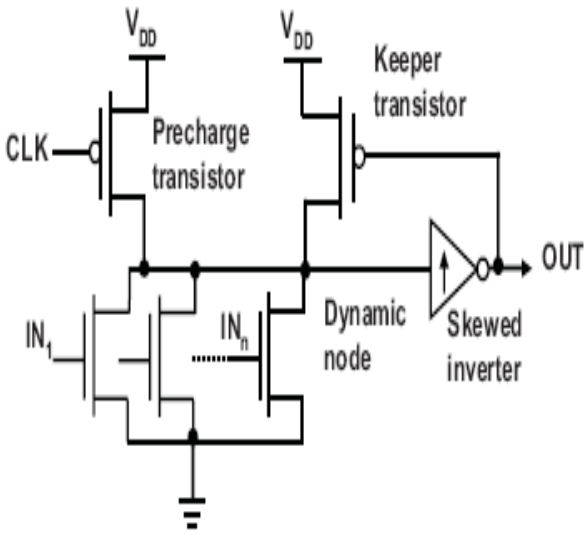

Fig.1. SFLD[4], Conventional standard domino

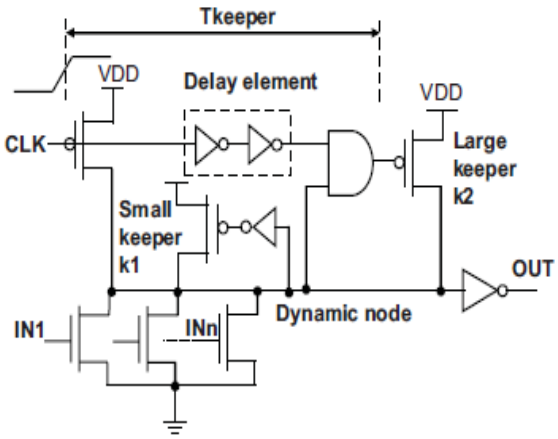

Fig.2. CKD[5]

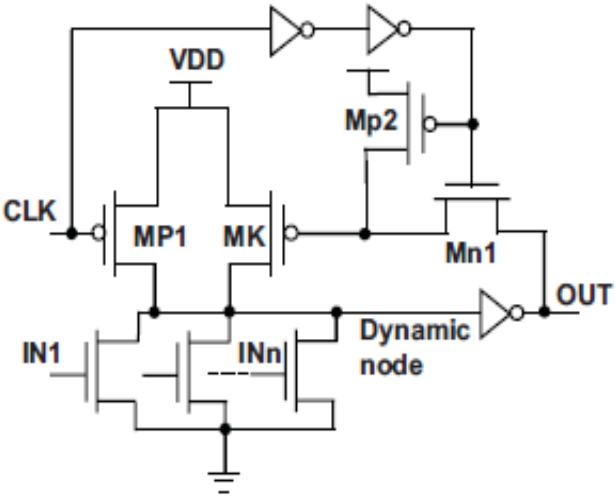

Fig.3. HSD [6]

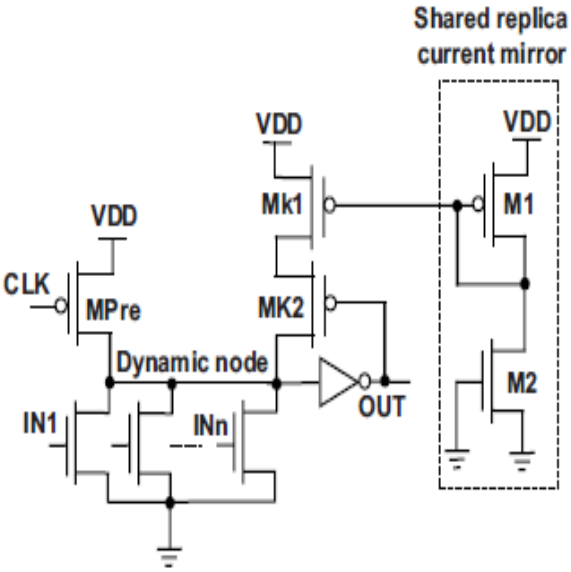

Fig.4. LCR Keeper [7]

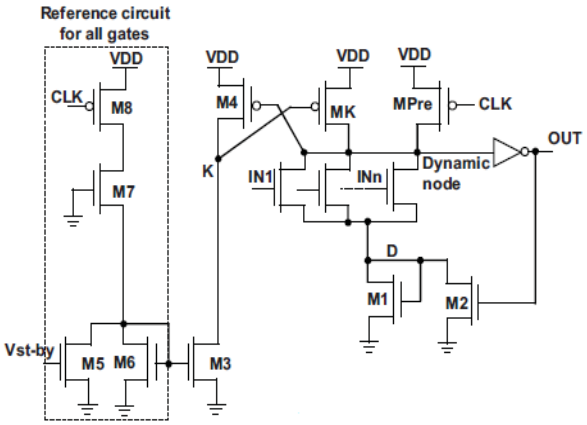

Fig.5. CKCCD [8]

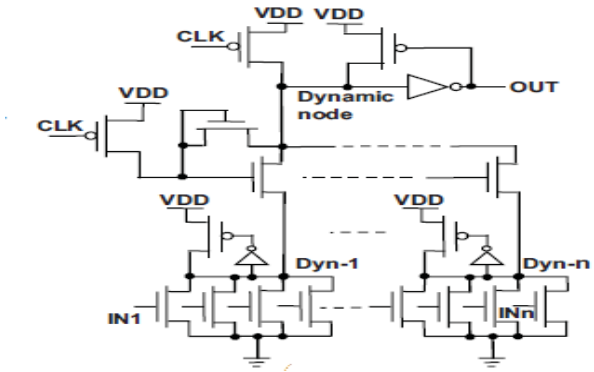

Fig.6. DPD [9]

III. PROPOSED DESIGN

The proposed design works in such a way that it contributes towards reduced power dissipation by reducing the capacitance, leakage current and current contention. The problems can be solved by separating the keeper transistor from the PDN which implements the logic function by using a comparison circuit. This circuit compares the worst case leakage current. Normally in domino logic, in the Pull Up Network (PUN) only one pMOS transistor is used instead of 'n' transistors where 'n' corresponds to the fan-in. the main logic will be implemented with the PUN. By reducing the number of transistors capacitance decreases. Few transistors means limited switching of the capacitor. Thus dynamic power consumption reduced, because the main source of dynamic power consumption is capacitance switching. Leakage current occurs due to unnecessary flow of current between the drain and the source of the transistor. This leakage current can be avoided by the "stacking effect". Stacking effect [4] says that when two or more transistors in series are at off condition, the leakage current can be reduced. A keeper transistor is used so that this transistor supplies a

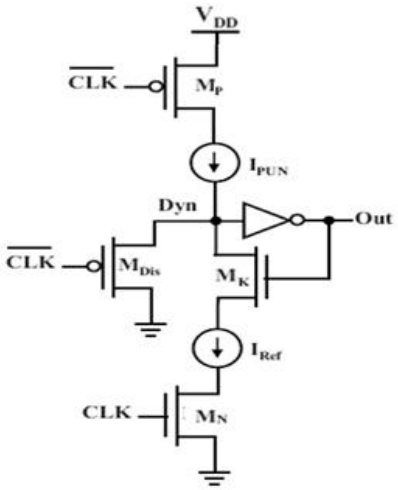

Fig.7 Concept of proposed circuit CCD

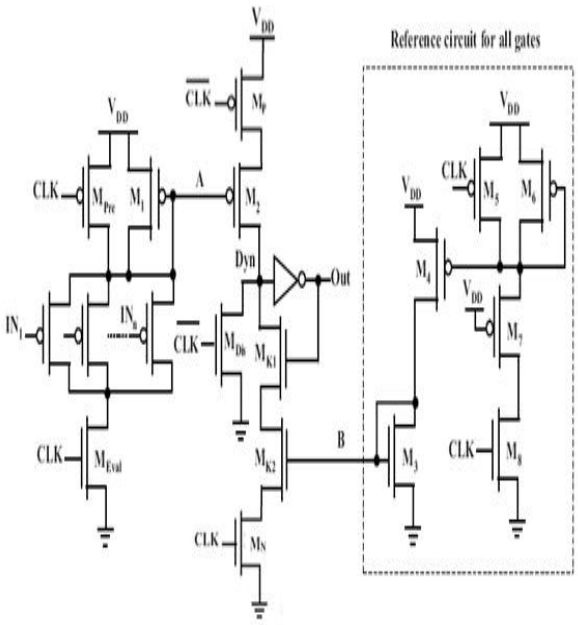

Fig.8 Implementation of wide OR gate using proposed CCD

small current from the supply to the dynamic node. Therefore charge stored is preserved for the needed conditions. Current contention is also a serious problem. By disabling the keeper for particular amount of time temporarily during the dynamic gate switching, the current contention problem is avoided. The proposed wide fan-in domino gate OR gate is shown in Figure 4. In the proposed circuit current of the PUN is reflected by transistor M2 and also compared with reference current, which replicates the leakage current of the PUN. The reference circuit shown in the figure generates the reference current. The proposed circuit is implemented with pMOS circuit to implement the logic function of OR gate. The source and body terminals of the pMOS transistor are connected together so that the body effect is eliminated. The transistor

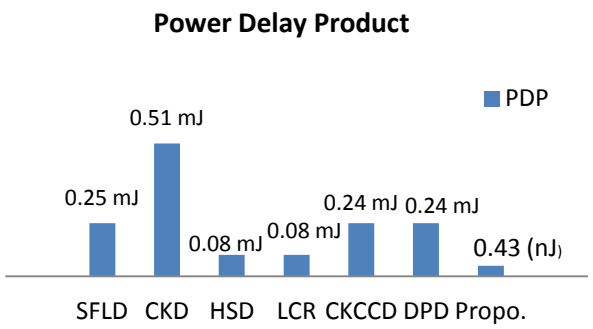

Fig.9 Power delay product of 4 fan-in OR gate in various domino logics.

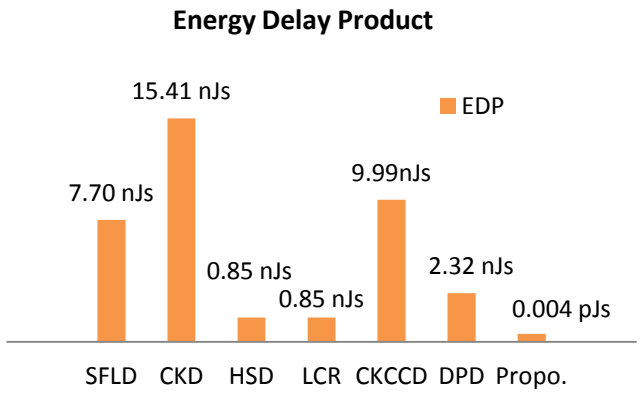

Fig.10 Energy delay product of 4 fan-in OR gate in various domino logics.

M1 is in diode configuration which means the drain and the gate are connected together. This helps in decreasing the leakage current reduction by using the stacking concept. Addition of M1 results in leakage reduction of evaluation network by stacking effect. The stacking effect decreases the drain source voltage of evaluation transistors and hence decreases the Drain Induced Barrier Lowering (DIBL). The DIBL is caused due to threshold fluctuation which in turn is caused due to high current flow between the drain and the source. So by decreasing power Vds, DIBL is reduced. Only one pull-up transistor is connected to the dynamic node instead of the n-transistor in the n-bit OR gate to reduce capacitance on the dynamic node, yielding a higher speed. Two clock gated transistors used here. Pull-up transistor connected to dynamic node controlled by CLK' gated pMOS transistor and keeper transistors controlled by the clock gated nMOS. With reference to the circuit schematic shown in Fig. 4.2, two phases of the proposed circuit are explained in detail as follows.

1) *Predischarge Phase*: Input signals and clock voltage are in high and low levels, respectively in this phase. Therefore, the voltages of the dynamic node (Dyn) and node A have fallen to the low level by transistor M_{Dis} and raised to the high level by transistor M_{Pre}, respectively. Hence, transistors M_{Pre},M_{Dis}, M_{k1}, and M_{k2} are on and transistors M_1, M_2, and M_{Eval} are off. Also, the output voltage is raised to the high level by the output inverter.

2) *Evaluation Phase*: In this phase, clock voltage is in the high level and input signals can be in the low level. Hence, transistors M_{Pre} and M_{Dis} are off, transistor M_1, M_2, M_{k2}, M_n, M_p and M_{Eval} are on, and transistor M_{k1} can become on or off depending on input voltages. So by incorporating the above said methodologies effective power dissipation reduction is achieved.

IV. SIMULATION RESULTS AND COMPARISONS

The proposed circuit was simulated using Tanner EDA tool with 180nm technology. The supply voltage used in simulation is 1.8 volt. From Table 1 it is visible that average power consumption, EDP and PDP of proposed domino logic reduced.

TABLE I

Comparison of Different Logic Style OR Gates of 4 Fan-In

	Avg Power	Max Power	Min Power	PDP	EDP
SFLD	8.563 (w)	0.863 (mw)	0.047 (nw)	0.25 (mJ)	7.708 (nJs)
CKD	17.11 (w)	3.992 (mw)	1.021 (nw)	0.51 (mJ)	15.41 (nJs)
HSD	8.562 (w)	90.81 (mw)	1.374 (nw)	0.08 (mJ)	0.856 (nJs)
LCR	8.563 (w)	0.864 (mw)	0.173 (nw)	0.08 (mJ)	0.856 (nJs)
CKCCD	6.248 (w)	1.457 (mw)	20.67 (nw)	0.24 (mJ)	9.998 (nJs)
DPD	23.26 (w)	6.657 (mw)	1.636 (nw)	0.23 (mJ)	2.326 (nJs)
Proposed	43.58 (µw)	1.547 (mw)	1.694 (pw)	0.43 (nJ)	0.004 (pJs)

Figure 9 and Figure 10 shows the graphical illustration of the comparison of power delay product(PDP) and energy delay product(EDP) between various domino logics of 4 fan-in OR gate. It shows a reduction in PDP and EDP compared to the other domino logic styles.

Simulated waveform of 4 fan-in OR gate is shown in Figure 11. Using proposed domino logic OR gates of 4, 8, 16, 32 and 64 inputs are implemented and simulated. The results are shown in table 2.Graphical representation of average power consumed by proposed domino OR gate of 4,8,16,32 and 64 fan-in shown in Fig.12

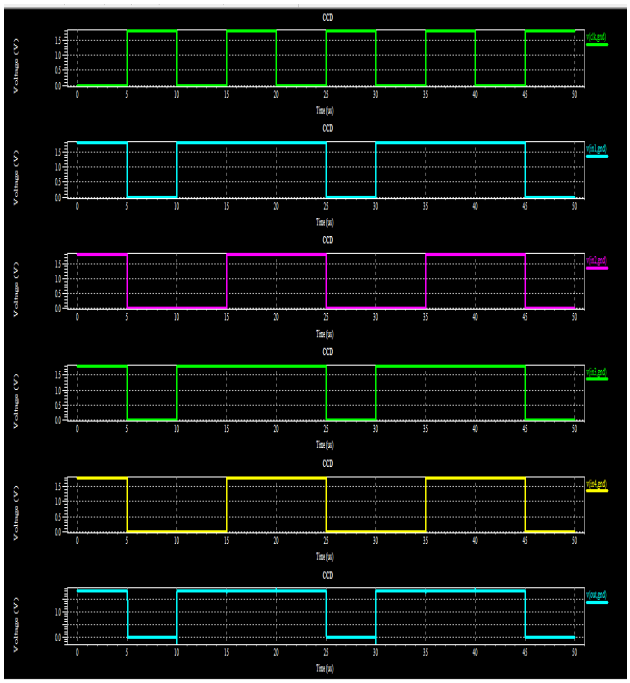

Fig.11 Simulated waveform of 4 input OR gate implemented in the proposed domino circuit.

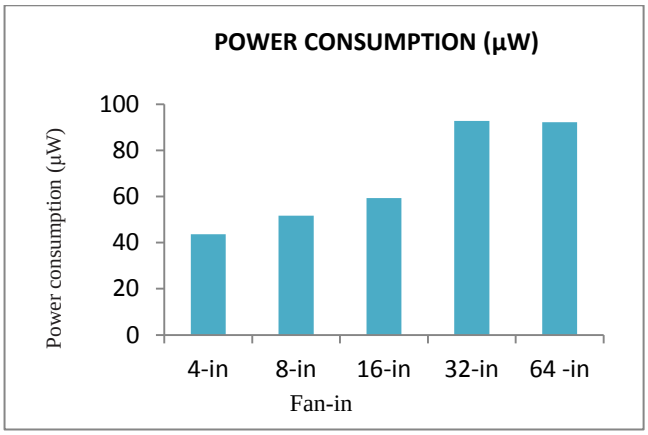

Fig.12 Average power consumed by proposed domino in 180 nm technology

V. CONCLUSION

The leakage current of the evaluation network of dynamic gates was dramatically increased with technology scaling, especially in wide domino gates, yielding reduced noise immunity and increased power consumption. Thus, new designs were necessary to obtain desired noise robustness in very wide fan-in circuits. Moreover, increasing the fan-in not only reduced the worst case delay, it also increased the here. The main idea is to compare the evaluation current of gate with the leakage current. By using this technique, the proposed domino circuit reduced the parasitic capacitance on the dynamic node this helps to reduce average power consumption, PDP and EDP. From the simulation results, it can be concluded that the total leakage power has been drastically reduced.

Table II

Performance Analysis of Proposed Domino Logic

Fan-in	Average power	Max. power	Min power	PDP	EDP
4-in	43.587 (µw)	1.547 (mw)	1.694 (pw)	0.436 (nJ)	0.004 (pJs)
8-in	51.640 (µw)	4.850 (mw)	330.433 (pw)	1.807 (nJ)	0.063 (pJs)
16-in	59.361 (µw)	16.286 (mw)	210.509 (pw)	2.077 (nJ)	0.072 (pJs)
32-in	92.668 (µw)	29.663 (mw)	248.706 (pw)	3.243 (nJ)	0.113 (pJs)
64 -in	92.123 (µw)	59.618 (mw)	385.598 (pw)	4.146 (nJ)	0.187 (pJs)

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