"45 nanometer innovative NMOS Low Pass Filter as Sample and Hold Circuit"

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Abstract: **Communication system is never implemented without a low pass filter, especially at the receiver side. In this research work, a low pass filter has been introduced using NMOS. These filters are implemented as basic sample and hold circuit. It also has application in many devices such as rectifier, in Phase Locked Loop for providing DC input to Voltage Controlled Oscillator. The simulation has been performed using Multisim and layout has been generated using Microwind 3.1. The process technology that has been introduced is 45 nanometer.**

Keyword: **45 nm, Low Pass Filter, Microwind 3.1, Multisim, NMOS, Sample and Hold Circuit**

I. INTRODUCTION

A filter is an electronic circuit which is used to filter out selective portions from a given bandwidth range. There are many filters such as low pass, high pass; band pass and band reject filters. Broadly speaking, filters are classified as Active and passive filters. A low pass filter is most commonly used filter in electronics and communication.

An active low pass filter using NMOS is shown here. This circuit forms the basic sample and hold circuit. A NMOS turns itself ON when input applied is Logic High. A "precharge" signal is applied at the Gate terminal, which is nothing but a pulse signal. A VDD supply is connected at the source end and RC network is connected across the drain terminal. The output is taken from capacitor. The schematic diagram is generated using S-Edit in Tanner EDA tool, as shown below,
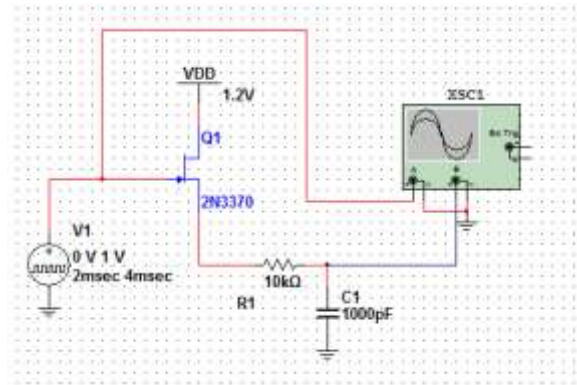

Figure 1.1 Schematic layout of NMOS Low pass filter in Multisim

II. WORKING

The working of this NMOS filter is as follows:

When Precharge is having a low value than the threshold value of NMOS, it remains in cut-off state and output is low. When the precharge pulse is at Logic High and greater than the threshold value of NMOS, it turns ON and conducts. The VDD supply charges the capacitor up to (VDD-VTH). After precharge is again low, the NMOS is in OFF state and now the output is still high because the capacitor is now providing the output by discharging itself. The input and output waveforms are shown below using T-Edit Tanner EDA. The capacitor has a value of 1pF and resistance is 5000 ohms. The supply voltage is 1.2 volts.

For generating a layout. Microwind 3.1 has been used. Precharge is provided through polysilicon.
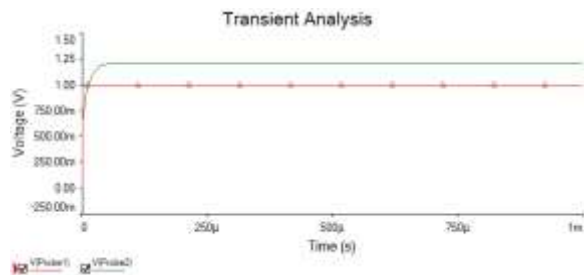
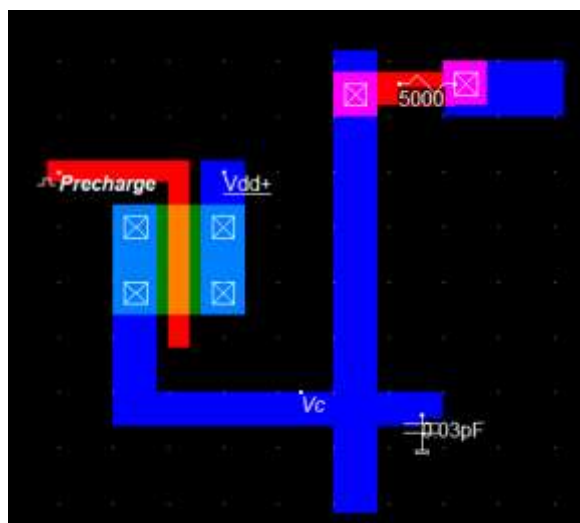Figure 1.2 Input and Output waveform of NMOS Low Pass Filter in Multisim

Figure 1.3 NMOS Low Pass Filter Layout using Microwind 3.1 in 45 nanometer Process Parameter
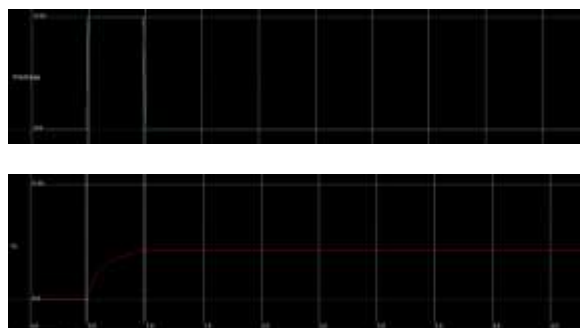

Figure 1.4 NMOS Low Pass Filter Input and Output Waveforms using Microwind 3.1 in 45 nanometer Process Parameter

The resistor is polysilicon resistor since it offers low resistance than other resistors.

The power dissipation achieved is 0.6µW. The W/L ratio selected for this low pass filter is

	Width (µm)	Length (µm)
NMOS	0.180	0.040

III. CONCLUSION

A NMOS low pass filter serving the purpose of simple sample and hold circuit has been introduced in 45 nm process technology. The output generated can be used as input to a VCO in type I PLL. Also it can provide DC output for many DC operated device.

IV. REFERENCES

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