# IMPEDANCE SOURCE OF FIVE LEVEL CASCADED MULTILEL INVERTER

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*Abstract:-* **This paper deals with simulation of impedance source H-Bridge five level inverter. The impedance network in the cascaded multilevel inverter circuit will perform buck/boost operation. This impedance network reduces one stage (buck-boost) of power conversion system. Using impedance source in multilevel inverter there is no problem of shoot through. Using Multilevel inverter topology the voltage stress across switching devices is reduced and the overall harmonics profile is improved do to multilevel output voltage. Multilevel inverter topology have an alternative to the normal two level inverters, especially in high power application do to above advantages. There are several multilevel inverter topologies but the best topology is cascaded Multilevel Inverter. such as simple circuit layout, less components count and low THD level in the out.**

*KEYWORDS:* **Z-Source inverter, Electromagnetic interference and multilevel inverter.**

## I.INTRODUCTION

In a traditional voltage-source inverter, the two switches of the same-phase leg can never be gated on at the same time because doing so would cause a short circuit (shoot through) to occur, which would destroy the inverter. In addition, the maximum output voltage obtainable can never exceed the dc bus voltage. Each converter generates a square wave voltage waveform with different duty ratios, which together form the output voltage waveform. These limitations can be overcome by the new *Z*-source inverter [1],[2]. In addition, the reliability of the inverter is greatly improved because the shoot through caused by electromagnetic interference (EMI) noise can no longer destroy the circuit. Thus, it provides a low-cost and reliable. Multilevel inverters synthesizing a large number of levels have a lot of merits such as improved output waveform, a smaller filter size, a lower EMI (Electro Magnetic Interference), and other advantages.

Using multilevel technique, the output voltage amplitude is increased, switching devices stress is reduced and the overall harmonics profile is improved. Several multilevel topologies are reported [1, 2, 3], and the most popular topology is Cascaded Multilevel Inverter (CMI). It offers several advantages compared to other topologies such as simple circuit layout, less components counts, modular in structure and avoid unbalance capacitor voltage problem. However as the number of output level increases, this topology becomes highly cumbersome because the number of power devices is increases.

## II.IMPEDANCE NETWORK

The circuit diagram of impedance network is shown in the Fig. 1. It consists of a pair of capacitors and inductors respectively. The value of capacitors and inductors can be chosen based on the output voltage requirement. A diode is connected in the impedance network as shown Fig. 1 to block the reverse flow of current. A voltage type impedance source inverter can assume all active and null switching states of VSI. Unlike conventional VSI, a impedance source fed inverter has a unique feature of allowing both power switches of a phase leg to be turned ON simultaneously (shoot-through state) without damaging the inverter. The impedance network changes the circuit configuration from that of a voltage source to an impedance source (i.e. Z-source). It allows the VSI to be operated in a new state called the shoot-through state in which the two switching devices in the same leg are simultaneously switched-on to effect short-circuit of the dc link [3]. During this state, energy is transferred from the capacitors to inductors, thereby giving rise to the voltage boost capability of the impedance source fed inverter. The impact of the phase leg shoot-through on the inverter performance can be analyzed by considering the circuit diagram shown in Fig. 1

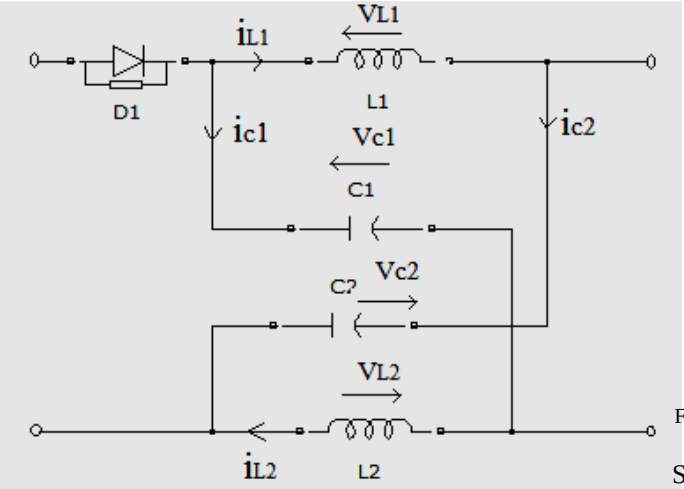



Fig.1 Impedance network

When the impedance network is in non – shoot – through state unlike normal voltage source inverter it can assume a third distinct state for inductive voltage boosting by turning ON two switches from any phase-leg simultaneously to create a short-circuit across the inverter dc-link (vi = 0V). Doing so will not damage any semiconductor devices because the energy supplied by the dc source and shunt capacitors is prevented from surging instantaneously by the Z-source inductors. Therefore (assuming *L*1 = *L*2 = *L* and *C*1 = *C*2 = *C*):

vL1 = vL2 = VL = VC1 = VC2 = VC ……. (1)

vL = vdc - VC …….. (2)

Vi = 2VC - vdc ……. (3)

## INVERTER III.IMPEDANCE SOURCE FIVE LEVEL CASCADED MULTILEVEL

Simulated configuration of impedance source Five level cascaded multilevel inverter is shown in Fig.2. It consists of eight IGBT/Diode switches. Each H bridge consists of four switches respectively.

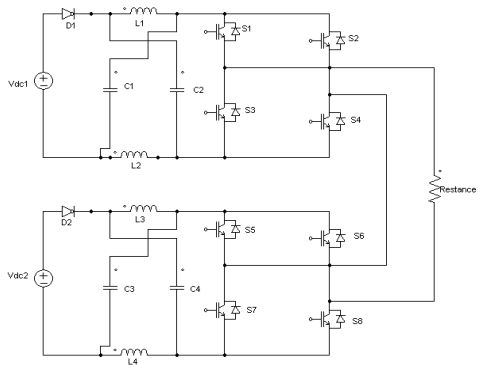



Fig.2 Five level Impedance Source of Cascaded multilevel inverter

Source for each H bridge is fed from impedance network. This voltage will be less or greater than input dc voltage. Nature of the load is pure resistive. Based on the values of inductor pairs and capacitor pairs in a impedance network magnitude of $V_{dc}$ is chosen. Since each H bridge in an inverter circuit can provide three voltage levels(zero, positive dc voltage and negative dc voltage). So switching state is defined for H bridge in an inverter circuit as shown in below table.1.

Table1: switching states

| Out put voltage | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 |
|---|---|---|---|---|---|---|---|---|
| $2V_o$ | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| $V_o$ | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| $-V_o$ | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| $-2V_o$ | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

## IV. PWM TECHNIQUES

The number of control methods to control Z-source inverter, that include the sinusoidal PWM techniques, three types of PWM control algorithms: simple boost control (SBC), maximum boost control(MBC), constant boost control (CBC).

The modulation index also called as amplitude modulation ratio (M) which is the main control factor is defined as the ratio of amplitude of reference wave to the amplitude of carrier wave

$$M = \frac{Vref}{Vcar}$$

The linearity between the modulation index and the output voltage is achieved by under
modulation index (M < 1).

## SIMPLE BOOST CONTROL

Actually, this control strategy inserts shoot through in all the PWM traditional zero states during one switching period. This maintains the six active states unchanged as in the traditional carrier based PWM . the implementation of simple boost control method is illustrated in fig.3. Two straight lines are employed to realize the shoot through duty ratio (Do). The first one is equal to the speak value of the three-phase sinusoidal reference voltages while the other one is negative of the first one. When the triangular carrier wave fore is greater than the upper envelope, $V_{PH}$ or lower than the bottom envelope $V_n$, the circuit turns into shoot-throught state, otherwise it operates as traditional carrier-based PWM.

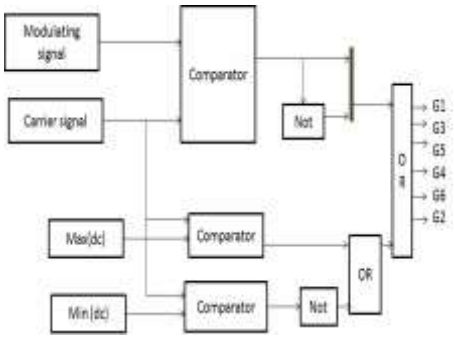



Fig3. Shown the Implementation Diagram of SBC

Shoot-through pulses are inserted in to the switching waveforms by logical OR gate. To produce switching pulses, three phase reference wave forms having value with modulation index(M) are compared with the same high frequency triangular signal. Comparator compares these two signals and produces pulses (when Vsin>Vtri, on and Vsin<Vtri,off). These pulses are than sent to gates of the power IGBT's through isolation and gate drive circuit, Fig.4. show the pulse generation of the three phase leg switches($S_1$, $S_3$ and $S_5$ positive group/upper switches and $S_2$ , $S_4$ and $S_6$ negative group/lower switches). For a complete switching period. $T_{is}$ total switching period. $T_o$ is the zero state time period and $D_o$ is the shoot-through duty ratio. In this paper, the control of ZSI is done by this control technique(SBC).

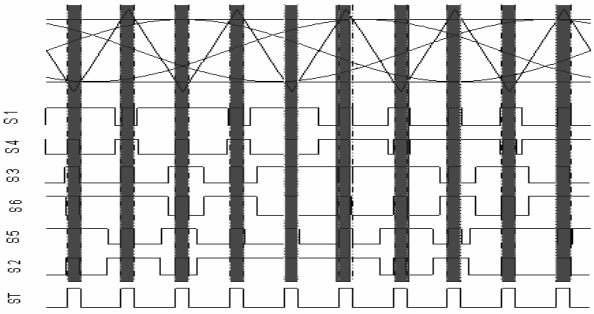



Fig 4: PWM Signals from Simple Boost control

Important mathematical expressions:

The voltage gain of the inverter with simple boost control

$$G=M*B\text{----------(4)}$$

$$G = \frac{M}{1-Do} = \frac{M}{1-2(1-M)} = \frac{M}{2M-1} - -$$

G is inverter voltage gain;

M is modulation index;

B is boost factor;

$D_o$ is duty ration;

The voltage stress across the inverter devices is given by

$$V_{inv}= B*Vo\text{----------(6)}$$

$$B=2G-1\text{---------(7)}$$

$$V_{inv} = (2G-1)*V_O = \frac{Vo}{2M-1}\text{------(8)}$$

## V.MULTICARRIER PWM STRATEGIES

There are four carrier-based PWM schemes for mentioned topologies.

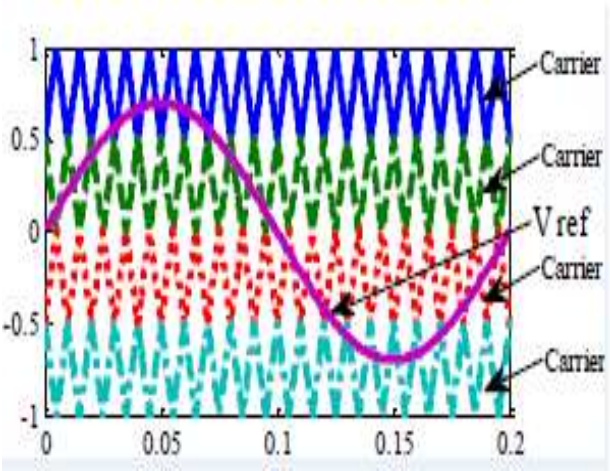
*a) Alternative Phase Opposition Disposition (APOD), where each carrier signal is phase shifted by180 from adjacent carrier;*

*b) Phase Opposition Disposition (POD), where the carrier signals above the sinusoidal reference zero*

*point are 180 out of phase with those below the zero point;*
*c) Phase Disposition (PD), where all carrier signals are in phase.*

Fig.5 shows carrier-based PWM strategies. APOD, POD and PD modulations are used to control most of multilevel inverter structures.
There are several methods to control Z-source inverter that can be classified into shoot-through states insertion methods. In the first method, six shoot-through states will be inserted in one switching cycle. The second method two shoot-through states will be directly inserted in one cycle



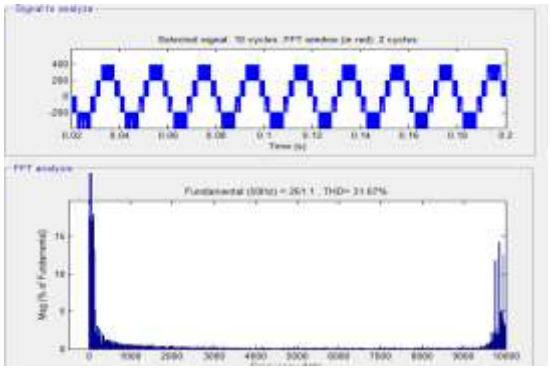

strategies Fig. 5 shows carrier-based PWM.

## VI.RESULT DISCUSSIONS

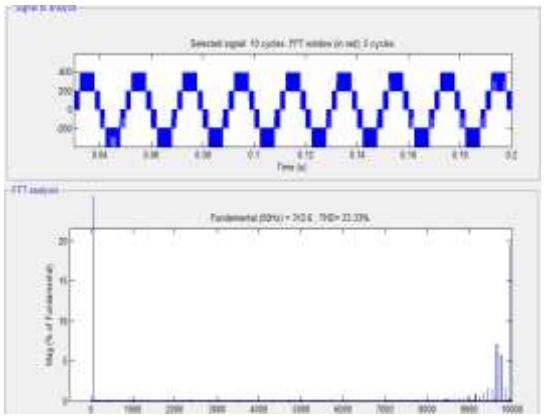
Experimental output voltage waveform for impedance source five level cascaded Multilevel Inverter is show in fig input dc voltage for frist and second H-bridge is given as 100v.

| | Parameters |
|---|---|
| Source | 200V |
| LC network | L=50mH |
| | C=400mf |
| Inveter | $f_c$ =10khz |
| | $f_r$ =50hz |
| | M=0.6, K=1 |
| | $T_o$/T=0.5 |
| Lord | R=1000Ω |

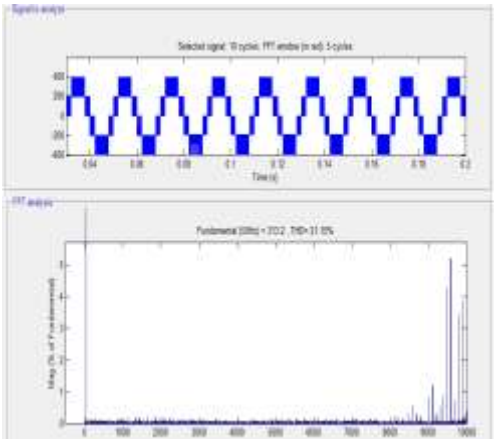
Experimental output voltage wave form for impedance source five level cascaded multilevel inverter is shown in below figs.6.7.8. Load used for this simulation is resistive load of 1000Ω. This can be observed in below output voltage waveform.



Experimental output of APOD modulation as shown above fig.6



Experimental output of POD modulation as shown above fig.7



Experimental output of PD modulation as shown above fig.8

For the above experimental output 380v and waveform THD of 21.3% is obtained which is show in above figs

The below table will show the different modulation index with Output Voltages and THD%

| | PD | | POD | | APOD | |
|---|---|---|---|---|---|---|
| Ma | $V_{rms}$ | THD | $V_{rms}$ | THD | $V_{rms}$ | THD |
| 1.2 | 305 | 21.15 | 285.6 | 23.33 | 256.1 | 31.67 |
| 1.1 | 294 | 23.05 | 275.2 | 24.39 | 246.5 | 32.40 |
| 1 | 277 | 26.08 | 258.8 | 27.59 | 231.5 | 34.66 |
| 0.9 | 249.1 | 32.94 | 232.3 | 34.07 | 207.5 | 40.60 |
| 0.8 | 221.5 | 37.56 | 206.6 | 38.56 | 184.6 | 44.8 |

## VII.CONCLUSION

From the simulation output of impedance source cascaded multilevel inverter the ripple contents and the harmonics in the output voltage of the inverter is reduced. Impedance source cascaded multilevel inverter topology have ability to produce any desired output ac voltage, even greater than the line voltage, regardless of the input voltage, thus reducing motor ratings and provide ride-through during voltage sags without any additional energy storage elements and impedance network in each bridge can do both buck and boost operation based on the values of inductors and capacitors in the network. The presented simulation results have been obtained by using MATLAB sim power system tool.SSS

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