DESIGN AND DEVELOPMENT OF DRIVER AND CONTROLLER MODULE FOR HIGH POWER LASER DIODE ARRAY

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***Abstract*- Design of laser diode array driver one of the crucial and challenging activity for the development of high power laser source. The performance of the laser diode arrays (LDA) driver directly affect the performance of the laser source i.e. output energy stability, pulse to pulse timing jitter, life of the device etc. [1]. The designed driver used a high-power MOSFET as a current control device, sense resistor as a feedback device for sampling current and FPGA for control and operations logics. The driver comprises the programmable selection options for diode current, pump pulse duration and repetition rates. The LDA needs to be operated in quasi-continuous (QCW) mode with stable output power at 1Hz to 20 Hz repetition rate. Each LDA requires operating constant pulse current of 50A to 120A to obtain the desired output power of 1000W to 2400W for a duration of 150 µs to 200 µs. The driver and controller module consists of pulse generator circuit, high value capacitor bank, high pulse current & fast switching MOSFET, pulse width control, constant current amplitude control and current protection circuits. The output pulse power of the LDAs will be controlled and stabilized using FPGA [2]. In this paper, we describe our works for designing of compact driver and controller module for high power laser diode array.**

Keywords- LDA, MOSFET, FPGA.

I. INTRODUCTION

The LDA (Laser Diode Array) have been widely used in high power laser applications in recent years because of its high efficiency, monochromatic, small size, light weight and long life, but the LDA operating life and characteristics strongly depend on the drive current [3][4]. As LDA is operated by driving the electric current, the power output fluctuates for a small change in the input current. So the driver is very important part of the system and it need to be designed so that the power output is constant over a period of time. This constant power output can be achieved by using a constant current controller.

The FPGA (Field Programmable Gate Arrays) have become an alternative solution for the realization of digital control systems, which were previously dominated by microprocessors [5]. FPGA-based controllers offer advantages such as high speed, capability to carry out complex functionality, and low power consumption. These are attractive features from the compact system design point of view. Another advantage of FPGA is the flexibility and capability to perform parallel tasks.

In this paper, the complete design approach is presented in which FPGA-based current controller is utilized to design a driver and controller module for high power laser diode array.
16bit DAC and ADC are used according to the design requirement in as shown in Fig.1. The complete system is implemented by dividing system functions into reconfigurable modules and need to go through three phases: 1) System design in an environment such as ORCAD/PSPICE 2) hardware implementation and 3) testing.

II. SCHEME OF OPERATION

The driver and controller module involves FPGA, Power supply, DC-DC converter, Capacitor bank, DAC, ADC, MOSFET Driver, Power MOSFET, Over Current Protection circuit, Laser Diode Array and a Sense

resistor. The block diagram is shown in Fig.1. First as per the received data command the set value between 50-120Amperes is to be selected.

The input to the capacitor bank is calculated based on the charging and discharging parameters. Once the data command is given to the FPGA the DAC generates analog Voltage as output which drives the power MOSFET. Based on the V_{GS} i.e., Gate to Source Voltage the drain to source of the Mosfet conducts and the pulse current gets grounded via Sense resistor.

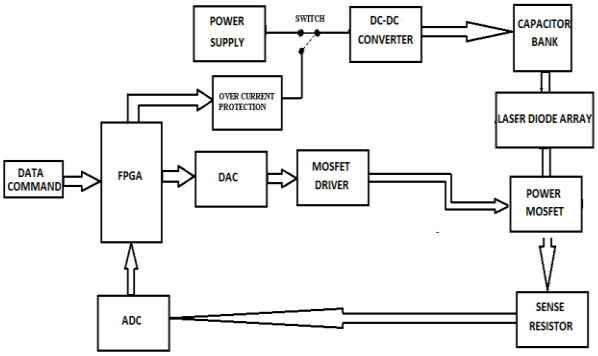

Fig. 1 Block Diagram of LDA

The current is sensed by a sense resistor and Voltage across the sense resistor is converted into digital bit pattern by ADC which forms the closed loop feedback. In FPGA VHDL software, the current value is to be calculated and subtracted with the set value which generates an error. This error can be minimized. When the generated error is beyond the particular value the over current protection circuit will become active and disconnects the mains power supply.

III. THE HARDWARE OF THE DRIVER

The driver and controller module consists of pulse generator circuit, high value capacitor bank, high pulse current & fast switching MOSFET, pulse width control, constant current amplitude control and current protection circuits.

The pulse generator circuit generates rectangular pulses with required pump pulse width and repetition rate. A high Value Capacitor bank is used to source high currents for pump pulse durations. An over current protection circuit disconnects the supply when current exceeds the limit value. A high pulse power MOSFET used as a current control device. MOSFET utilizes the change of the voltage between the gate and the source to change the quality of inducting electric charge in the diode surface and then controls the drain current. N-channel enhancement power MOSFET (IRFB4710PBF) is used in this driver. Its maximum drain current is 300A and this could meet the requirement of the design completely. The output characteristic curve of the Power MOSFET is as Fig. 2 shows.

According to the datasheet the threshold voltage of Power MOSFET is 3.3 V to 5.5 V and as shown in Fig.-2 the voltage between gate and source must reach about 7.3V in order to achieve the drain current 50 A. The required gate voltage is loaded on the gate of MOSFET through emitter follower MOSFET driver from DAC. In addition the slope of shifting characteristic curve is larger; therefore the slight change of the voltage between gate and source will cause the great change of drain current. A reference clock is generated by a crystal oscillator and given to FPGA for timing reference.

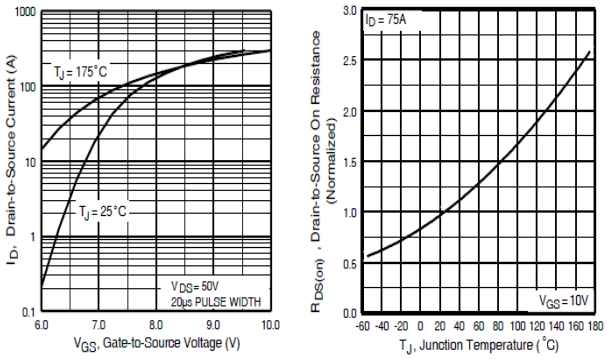

Fig. 2 Output characteristic curve of MOSFET

IV. DESIGN OF FPGA

The FPGA consists of different modules like, Data Command Interface, Current selection logic, PID controller and Frequency Divider. From data command serial data, serial clock and transfer pulse are given to serial to parallel converter

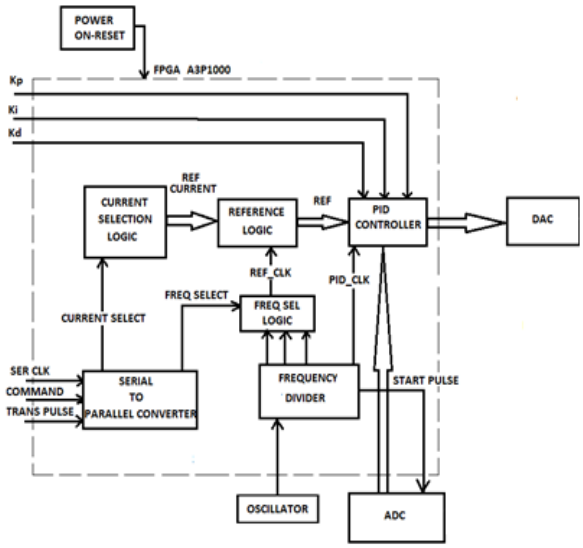

Fig. 3 Internal Block Diagram of FPGA

The entire block diagram is divided into 2 PCB cards i.e., one is the main PCB card and another is capacitor bank card. The main PCB card is interfaced to the computer system and the capacitor bank card is interfaced to the main PCB as well as to the DC_DC converter.

A. Data Command Selection

The system works depending on the data command given from the computer. The 16 bit data command format is given in the Fig.4 Here LSB bits 0- 4 are used for selection of current, bits 5-10 are used for selection of frequency, bit 11-14 are used for pulse width selection and bit 15 is for ON-OFF selection of the system.

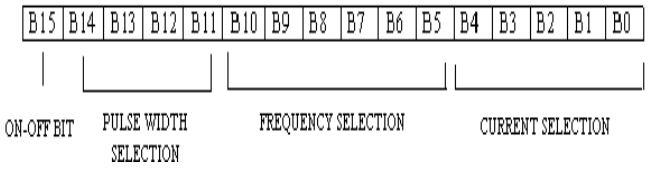

Fig. 4 Data command selection pattern

V. THEORETICAL CALCULATIONS

In order to attain high pulse current a high value capacitor bank is used. We have to choose the capacitance value according to the allowable droop voltage and available charging time.

A) Charging of the capacitor is represented by equation,

$$I = \frac{Vs}{R} e^{-\frac{t}{RC}};$$

B) Discharging of the Capacitor is represented by equation,

$$Vc = Vs\ (e^{-\frac{t}{RC}});$$

Where Vc- voltage across capacitor, Vs- supply voltageand RC- time Constant.

VI. EXPERIMENTAL SETUP & RESULTS

FPGA is implemented to control the High Power LDA(Laser Diode Array) along with 12-bit analog to digital converter,12-bit digital to analog converter, Capacitor Bank, Sense resistor and other circuitry as shown in Fig.5

The testing is carried out using LDA and the out results show the LDA output across the sense resistor as shown in Fig.6. Testing is carried out for 500mV and 25µs.

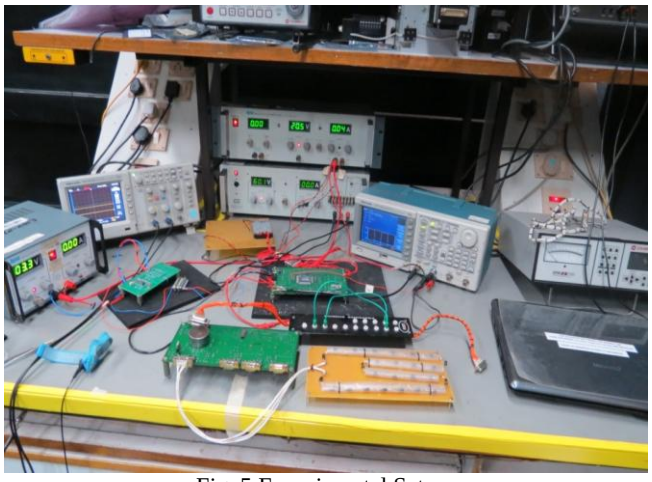

Fig. 5 Experimental Setup

Fig. 6 LDA otput

VII. CONCLUSION

The Laser Diode Array (LDA) is designed for driving current between 50A – 120A to obtain desired output power from the Laser diode. The circuit design is implemented in ORCAD PSPICE and the feedback system is designed using VHDL programming. The circuit wiring has been done and the Testing is carried out using two PCB's (FPGA card, Capacitor Card) and the results were published.

ACKNOWLEDGMENT

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