Simulation of Buck-Boost Converter Using Coupled Inductor

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***Abstract*— This paper proposes a new Buck –Boost converter using coupled inductor, which not only retains the functions of both buck and boost converters, but also extends the conversion range. The proposed generic and topology independent model is compatible with matlab and can be run on any electronic circuit simulator. In this paper 12V-48V to 28V dc-dc conversions are verified using matlab /simulink software.**

***Keywords*— Buck converter, Boost converter, PWM, Coupled inductor.**

I. INTRODUCTION

Many applications powered by batteries call for high performance, high step-up dc-dc converters. As an example, for a high intensity discharge (HID) lamp ballast used in automotive headlamps in which the start-up to 400V[1],[2], the dc-dc converters needs to boost the 12V of the battery voltage up to 100V during steady-state operation. Another example of a higher step-up application is the front-end converter with dual inputs. The convergence of computer and telecommunications industries makes the well defined 48V battery plant a good choice for offering hours of reverse time during outages of the ac mains[3]-[5]. Although both powered by the 48V dc power plant, the dc input converter more efficient and less complex than the uninterruptable power supply (UPS)[3],[5],[6]. The dc input converter must boost the 48V of the dc bus voltage to about 380V- 400V. Generally speaking the high step-up dc-dc converters for these applications have the following common features.

1.High step-up voltage gain. Generally, about a tenfold step –up gain is required.

2. High efficiency.

3. No isolation is required.

There are two major concerns related to the efficiency of a higher step-up dc-dc converter: large input current and high output voltage. The large input current results from low input voltage therefore, low-voltage-rated devices with low $R_{DS\text{-}On}$ are necessary in order to reduce the conduction losses. Another concern is the severe reverse - recovery problem that occurs in the output rectifier due to the high output voltage.

The dc-dc converter for supplying power to the microprocessor requires a large step-down conversion such as 48V source to 1.5V output. But the large step down cannot be easily realized by conventional buck converter due to high switching loss caused by the extremely narrow duty cycle.

Tapped-inductor converters [7]-[11] may be available for overcoming this problem, because a large step down conversion is easily achieved by selecting the turn-ratio of the tapped-inductor windings .However, these tapped-inductor converters have similar characteristics to a typical flyback(buck-boost)converter in the case of the high step-down conversion with large turn-ratio. Therefore the magnetic core size of the tapped –inductor is larger than that of the typical buck converter. And snubber or active clamp circuits should be necessary for reducing the switching surge of the main switch. In addition, drive circuit for the main switch will be complex and may be pulse transformer should be necessary.

This paper proposes a novel tapped- inductor Buck-Boost Converter .This converter looks like the conventional tapped –inductor converter with an active –clamp circuit ,but the clamp capacitor is connected in series to the tapped inductor converter has similar characteristics to a typical Conventional converters.

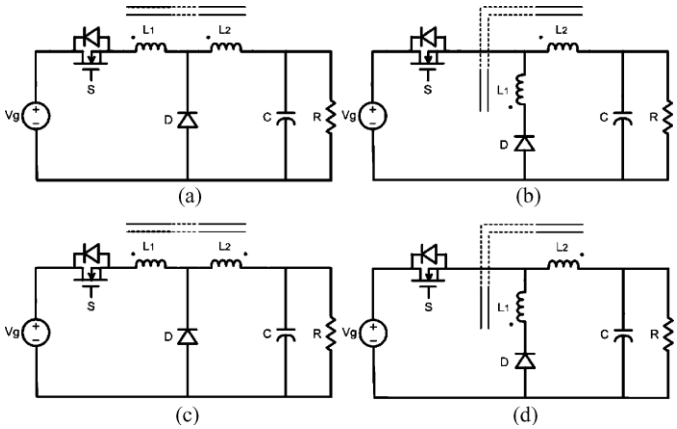

Fig. 1. Buck-derived converters with tapped inductors.

II. BASIC SWITCHING CONVERTER TOPOLOGY

The basic buck and boost converters can be transformed into a number of new topologies by bringing in the tapped inductor. The proposed tapped-inductor buck-derived converters are shown in Fig. 1, with their corresponding voltage conversion ratios plotted in Fig. 2. The proposed tapped-inductor boost derived topologies and their corresponding voltage conversion ratios are given in Figs. 3 and 4. Here, *D* is the duty ratio of switch S, *M* is the voltage

conversion ratio, and *n* is the turn ratio of the tapped inductors, which is defined as $n = n2 : n1$. As the turn ratio *n* tends to infinity, the conversion ratio of the buck-derived converters approach the characteristic of a basic buck topology. On the other hand, as the turn ratio *n* goes to zero, the conversion ratio of the boost-derived converters approach the characteristic of a basic boost topology. Inspection of the conversion ratio plots, as given in Fig. 1(a), reveals that the proposed buck-derived converter achieves wider voltage stepdown than a basic buck converter. Also, by examining Fig. 3(a), it becomes evident that the suggested boost-derived converter attains a wider voltage step-up than a basic boost converter. The converter topologies shown in Figs. 1(a) and 3(a) are strikingly similar. The idea proposed here is that these two topologies may be combined to form a new two-switch topology, with an extended conversion range. Same conclusion can be reached comparing the converters given in Figs. 1(c) and 3(c) The proposed BUCK-BOOST range converter topology is described in next section.

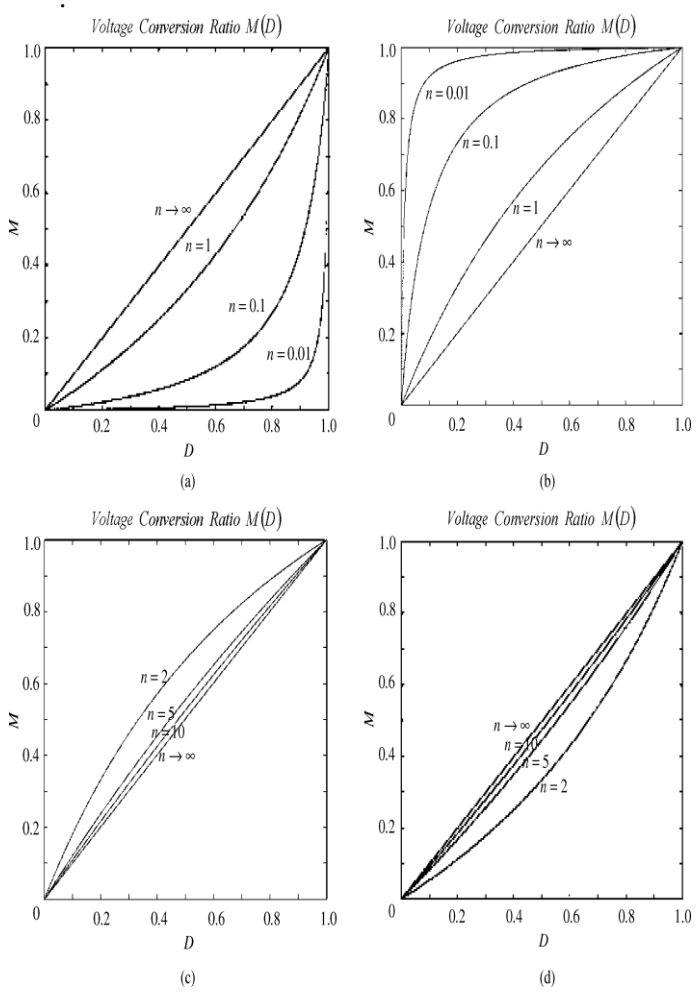

Fig. 2. Voltage conversion ratio of buck-derived converters with tapped inductors. (a) $0 < n < \infty$. (b) $0 < n < \infty$. (c)$n > 1$. (d)$n > 1$.

III. BUCK-BOOST DC-DC CONVERTER

A. Proposed BUCK-BOOST DC-DC Converter Topology

The proposed Buck-Boost dc–dc converter is illustrated in Fig. 5.The converter is comprised of two active switches S1 and S2, tapped inductors L1 and L2 with turns ratio $n = n2 : n1$, diode D, and capacitive output filter C.

Specifically, note that the tapped inductor in Figs. 1 and 3 is reconfigured into a pair of coupled inductors in Fig. 5. Being equivalent electrically, this reconfiguration is beneficial from a practical point of view. In Fig. 5, S1 and S2 are connected to a common junction or midpoint. The midpoint is periodically switched by S1 to ground, which allows recharging the bootstrap power supply and reliable operation of the flying driver of the top switch S2. Consequently, a standard half-bridge driver chip can be used with the low-side driver operating the bottom switch S1 and the bootstrap high-side driver activating the top switch S2.

Buck-Boost can operate either in the step-down or the buck mode or in the step-up or the boost mode. To operate the Buck-Boost in the buck mode, the switch S1 is assigned a high-frequency switching signal with a predetermined duty cycle *D*, whereas S2 is switched complementarily to S1. The diode D is kept ON by the inductor L2 current, which is assumed to be continuous. To operate Buck-Boost converter in the boost mode, the controller keeps S2 switch continuously ON and issues the required duty cycle signal for the S1 switch. Thus, the diode D is forced to switch on and off complementarily to S1.

In both modes, the capacitor C filters the pulsating current *and provides a smoothed output voltage for the load* R.

B. Control Scheme

For the proper operation of Buck-Boost, a modified PWM control circuitry is required. The implementation is not unique. One possible realization of the modulator is shown in Fig. 6. Here, a window comparator is employed to derive the required switching signals for S1 and S2 by comparing the sawtooth ramp with amplitude of Vm to the two control voltages VC and V'C. The control voltage VC for the upper comparator is delivered by an external source, whereas the lower comparator input signal V'C is derived by the PWM circuitry, down shifting the control voltage VC by Vm: V'C = VC − Vm. The relationship between the control voltage VC and the sawtooth ramp amplitude Vm can be expressed by means of a variable m as VC = mVm. Buck-Boost operates in the buck mode when $0 < VC < Vm$, i.e., when $0 \leq m < 1$. Here, the upper comparator generates the required duty cycle for the S2 switch, whereas the lower comparator is in "1" state and commands the NAND gate to provide the complimentary duty cycle for the S1 switch. Therefore, Buck-Boost operates similarly to a synchronous buck converter. On the other hand, for $Vm < VC < 2Vm$, or $1 \leq m < 2$, the upper comparator is in

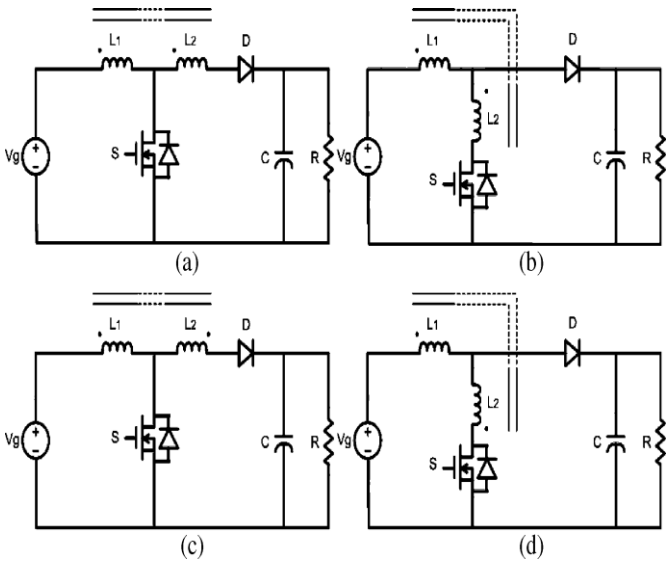

Fig. 3. Boost-derived converters with tapped inductors

"1" state and keeps S2 continuously ON, whereas the lower comparator and the NAND gate provide the required duty cycle for the S1 switch. Thus, the converter enters the boost mode.

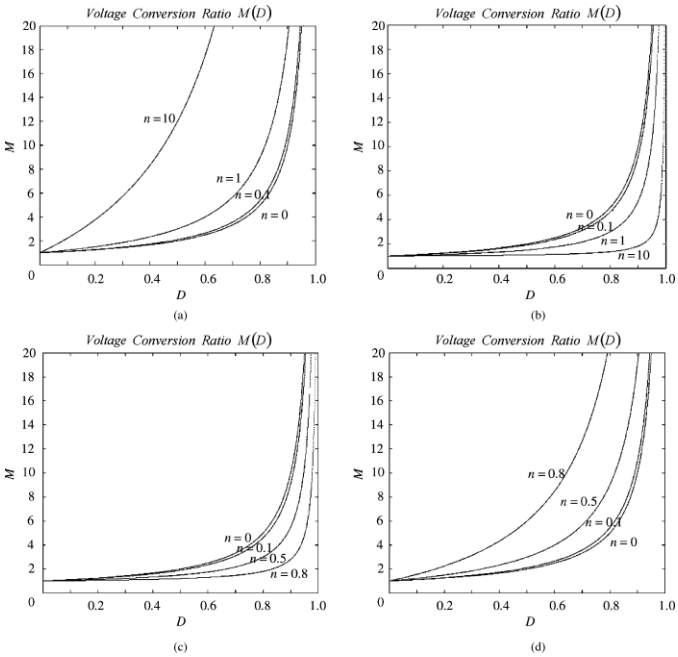

Fig. 4. Voltage conversion ratio of boost-derived converters with tapped inductors. (a) $0 < n < \infty$. (b) $0 < n < \infty$. (c) $0 < n < 1$. (d) $0 < n < 1$.

C. Operating Principle of the BUCK BOOST Converters

In the following, the steady-state operation of the proposed Buck Boost converter is described. The analysis is performed assuming that the circuit is comprised of ideal components. The coupling coefficient of the tapped inductor is assumed to be unity. Under continuous inductor current (CCM) condition, the proposed Buck Boost converter exhibits four topological states, as shown in Fig. 7. Here, the large output filter capacitor is replaced by an ideal voltage source. The waveforms and timing of Buck Boost for both buck and boost modes are illustrated in Fig. 8.

1) Buck Mode: State 1 ($t0 \leq t < t1$) is the buck-mode charging state [see Figs. 7(a) and 8(a)]. Here, the switch S2 is turned on and S1 is turned off. The diode D conducts and the coupled inductors L1 and L2 are charged. The energy is also transferred from dc source to load.

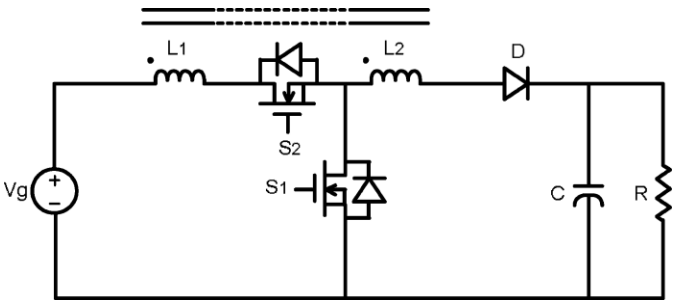

Fig. 5. Buck Boost dc–dc converter topology

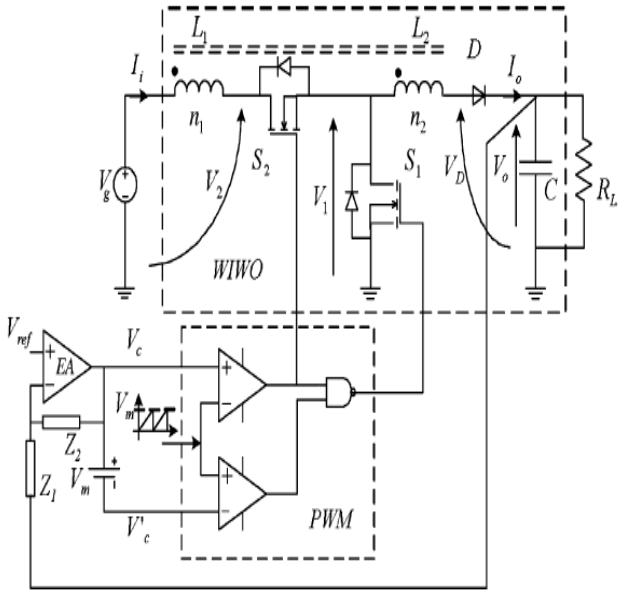

Fig.6. PWM Control Circuitry For Proposed converter

State 2 ($t1 \leq t \leq t2$) is the buck-mode discharging state [see Figs. 7(b) and 8(a)]. Here, the switch S2 is turned off also cutting off the current in the L1 winding, whereas S1 is turned on and the diode D conducts L2 current to the load.

2) Boost Mode: State 3 ($t\_0 \leq t < t\_1$) is the boost-mode charging state [see Figs. 7(c) and 8(b)]. Here, the switches S1 and S2 are turned on charging the L1 inductor. The diode D is cut off by the negative voltage induced in L2 winding. The output voltage is supported by the capacitor C.

State 4 ($t\_1 \leq t \leq t\_2$) is the boost-mode discharging state [see Figs. 7(d) and 8(b)]. Here, the switch S2 is still ON here

as S1 is turned off. Both windings L1 and L2 conduct through the diode D and discharge the stored energy to the output.

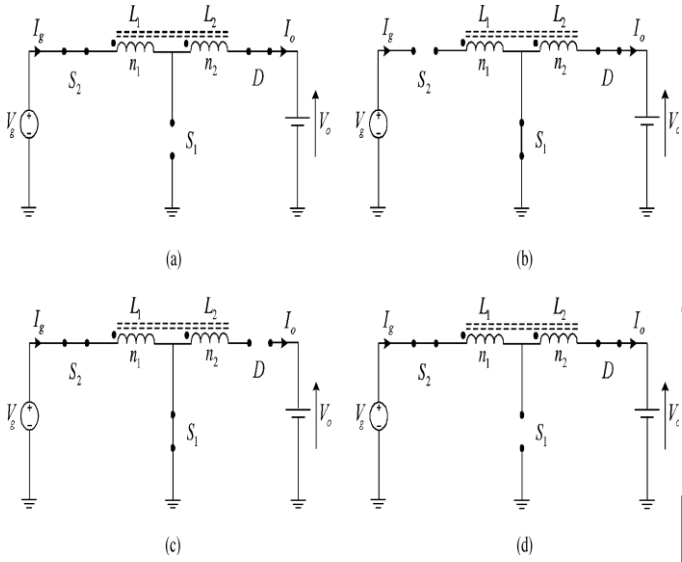

Fig.7. Four topological states of the WIWO converter. (a) Buck-mode charging state. (b) Buck-mode discharging state. (c) Boost-mode charging state. (d) Boost-mode discharging state.

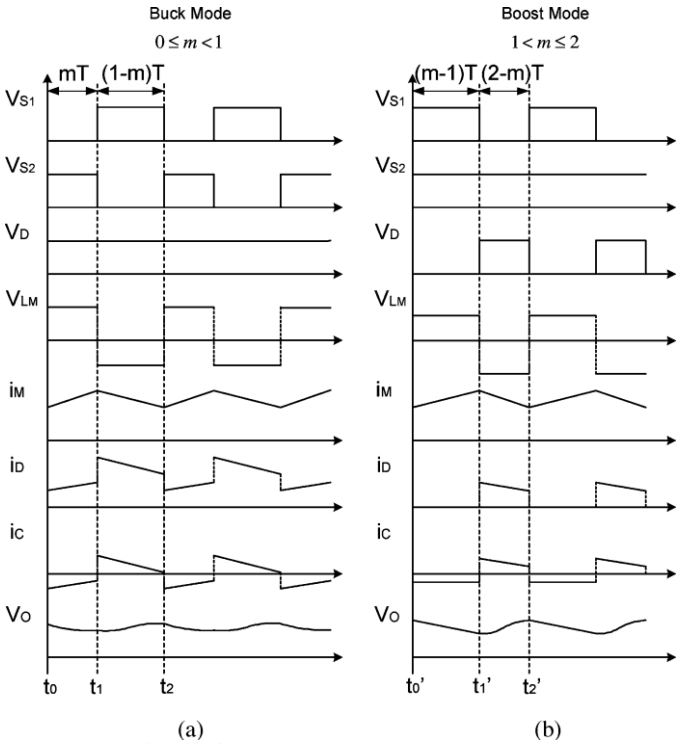

Fig.8. Waveforms of the WIWO dc–dc converter. (a) Buck mode. (b) Boost mode.

IV. SIMULATION RESULTS

Simulation Circuit:

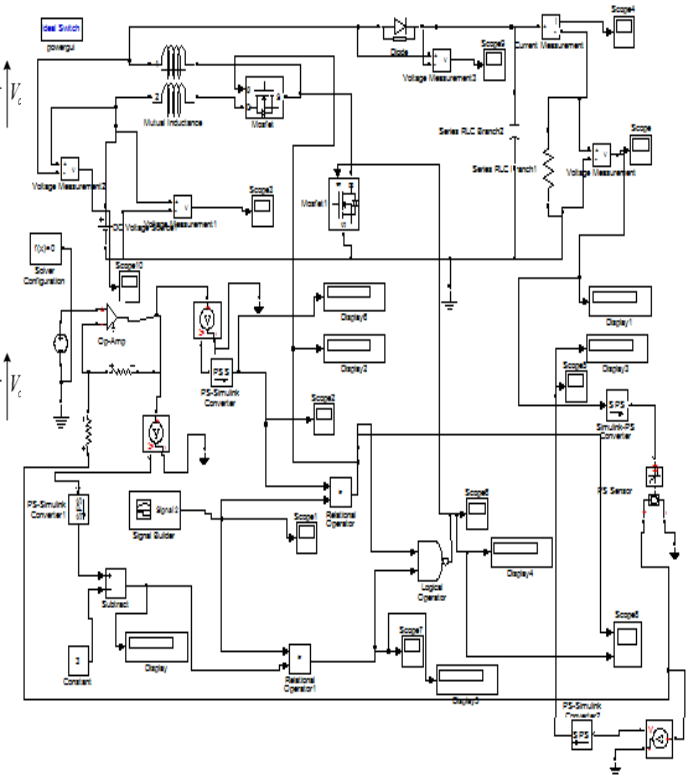

Fig:9.Matlab Circuit For Proposed Converter

SIMULATED OUTPUTS FOR BUCK CONVERTER 48V-28V

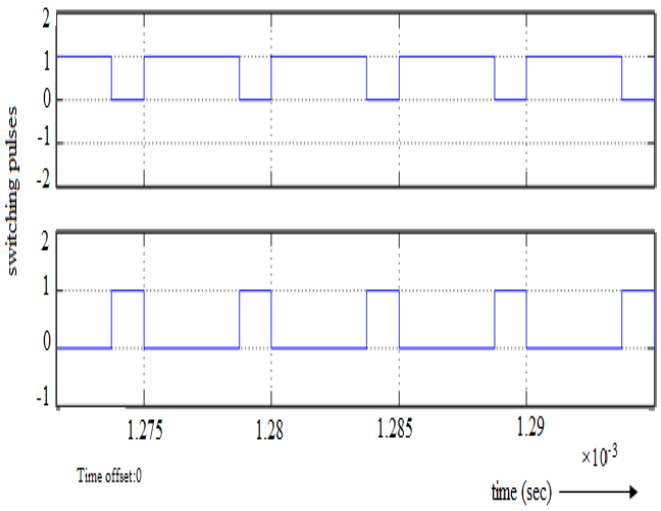

Fig:10 Switching Pulses (S2 & S1)

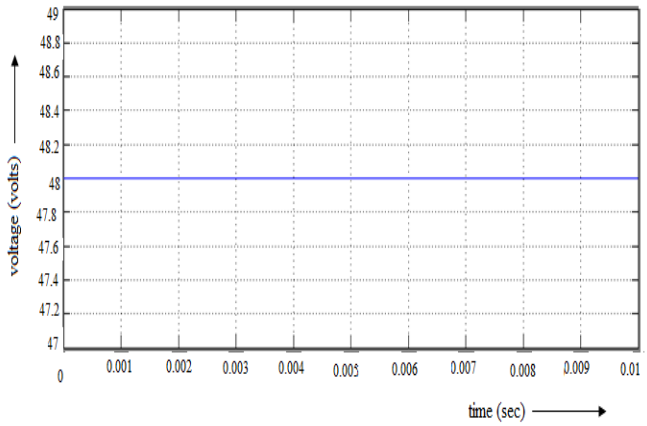

Fig: 10.1 Input voltage Vg

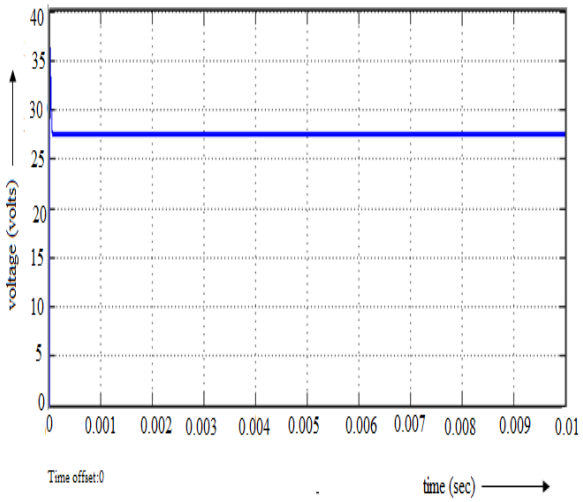

Fig: 10.2 0utput voltage

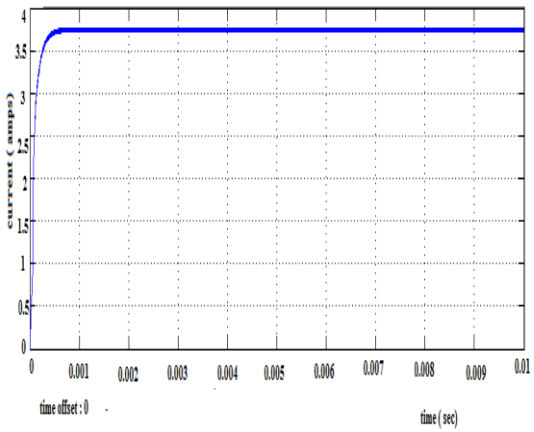

Fig:10.3Out Put Current

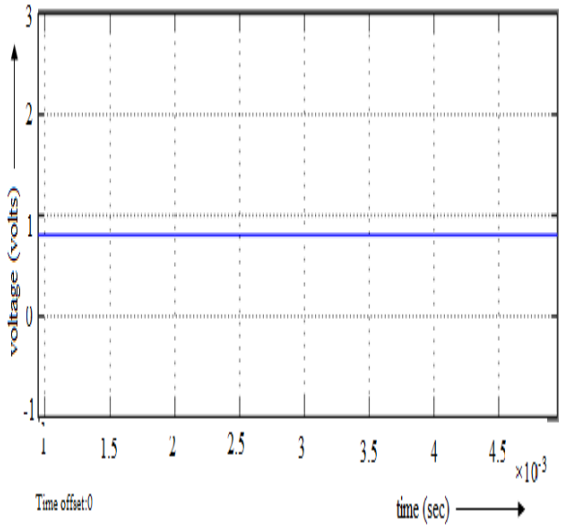

Fig:10.4Diode voltage

The buck converter converting 48V Input to 28V Output (buck mode) are Shown in the Fig.10.In the buck mode, S_2 is the leading switch, gated by the duty cycle. Switch S_1 is switched complementarily, similar to a synchronous converter. Switch Voltages.

The S_2 switch conducts; both windings carry the same current.At the S_2 is turned off, the leakage inductance of L_1 Developed a turn-off voltage spike across S1

SIMULATED OUTPUTS FOR BOOST CONVERTER 12V-28V

The boost mode with 12V input and 28V output, under full load condition, are shown in figure11. To supply the power requirements of the load at lower input voltage range, buck-boost converter calls for greater input current, and therefore, turn-off voltage spike on S_1 is observed in figure 11.1.

In the boost mode, the switch s_1 is the leading switch that is issued the duty cycle command, the buck mode the S_2 switch is constantly ON, The drain voltage of S_2 and the drain voltage of S_1 are almost identical.

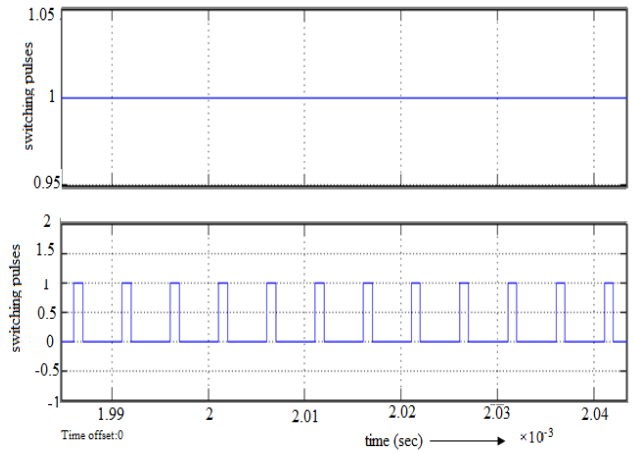

Fig:11 Switching Pulses (S2 & S1)

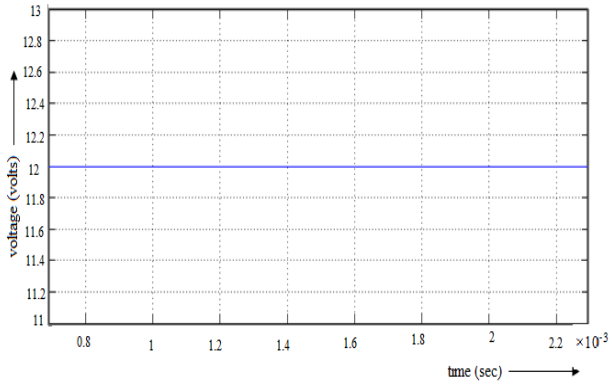

Fig:11.1 Input voltage Vg

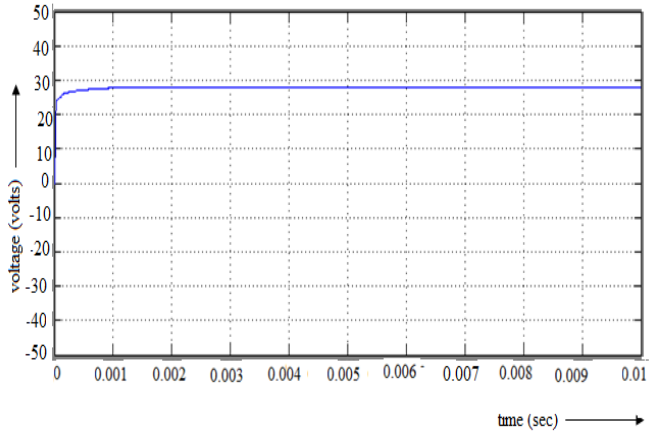

Fig:11.2 Output voltage Vo

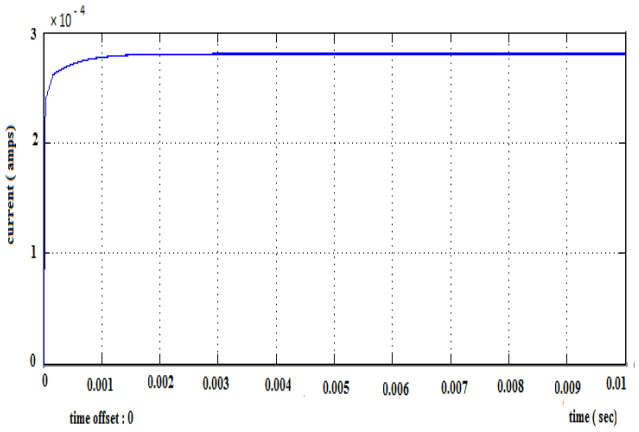

Fig:11.3 Out put current

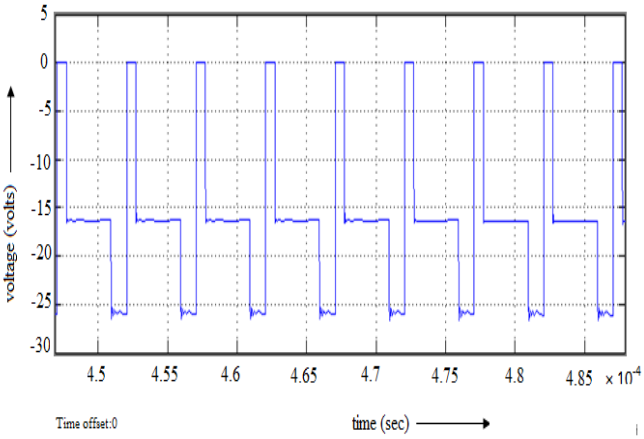

Fig:11.4 Diode Voltage

V. CONCLUSION

This paper has presented a new Buck Boost DC-DC converter, which is an integration of buck and boost converters with coupled inductors. The paper describes converter principles of operation and offers a comprehensive summary of analytical characteristics. Simulation results were also reported.

The new converter topology has several advantages. The buck boost converter retains the feature of both the buck and the boost converters. However, it achieves wide step up and step down dc-dc conversion range.

The advantageous buck feature allows turning off the output voltage on demand. The transition between the operating modes is inherently smooth and causes no transient disturbance in the average current.

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