Improve the Performance of Three Phases Cascaded Multilevel Inverter by using carrier PWM Topologies

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Abstract**: A new idea to enhance the performance of multilevel inverter that is an amalgamated rectangular reference function used to improve the performance of three phases cascaded multilevel inverter. In this paper we are using the bipolar trapezoidal amalgamated rectangular reference function is simulated for a phase shifted (PS) technique, level shifted (LS) technique and variable frequency (VF) techniques. In this level shifted strategy provides higher DC bus utilization and phase shifted strategy provides lowest distortions for moderate index m_a.**

Key words**: Three phase multilevel cascaded H- Bridge, phase shifted technique level shifted technique and variable frequency technique is used**

I.INTRODUCTION:

IN RECENT YEARS, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium voltage network Today, it is hard to connect a single power semi conductor switch directly to medium voltage grids (2.3, 3.3, 4.16, or 6.9 kV). For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels [1]–[3]. The principal motivation for multilevel topologies is the increase of power, the reduction of voltage stress on the switches, and the generation of high quality output voltages and sinusoidal currents.CMUs use more than one DC voltage source to generate an AC output voltage. Shanthi and Natarajan made a detailed comparative study of various unipolar multicarrier PWM strategies for single phase cascaded MU through simulation using MATLAB-SIMVLINK and dSPACEIRTI based implementation [4].To obtain a low distortion output voltage or a nearly sinusoidal output waveform, a triggering signal should be generated to control the switching frequency of each power semiconductor switch. They also simulated and implemented carrier overlapping bipolar PWM techniques for chosen single phase cascaded five level inverter. Ayob and Salam proposed a modulation technique for the cascaded multilevel inverter in [5].Generalization of the pulse width modulation sub harmonic method to control three phase multilevel voltage source inverter is considered in [6].The elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform [7].In this work, the triggering signals of multilevel converter are designed using the carrier based pulse width modulation (PWM) scheme, since the PWM provides high power with low harmonics. A three phase CHB grid connected multilevel converter circuit is designed and simulated using the MATLAB SimPowerSystems software

II. THREE PHASE 5-LIVEL CASCADED H-BRIDGE MULTILEVEL INVERTER

Three phase Inverter in Power-Electronics refers to a class of power conversion circuits that operate from a dc voltage source or a dc current source and convert it into a symmetric ac voltage or current

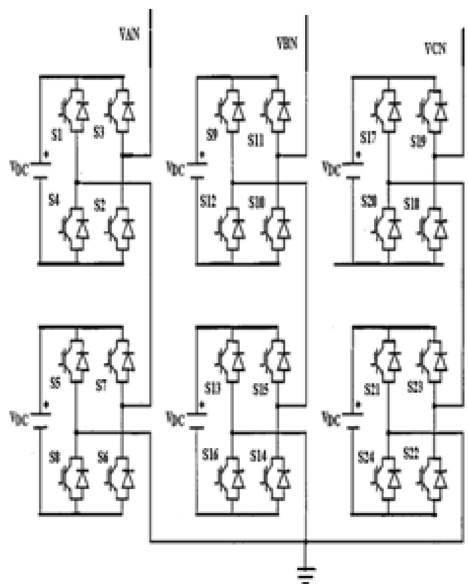

Fig.1 three phase five level cascaded H-bridge multilevel converter

The three phase structure of a five level cascaded multilevel inverter is illustrated in fig 1. The inverter composed of three legs, in each one is a series connection of three H-bridge inverter fed by independent dc sources. Each phase can generate five different voltage outputs +Vdc, +2Vdc, 0,-Vdc,-2Vdc using various combination of the switches. One of the terminals of each single phase five levels CHB multilevel inverter is connected as star, while the other terminal of each single phase CHB multilevel converter is connected to a three phase series load. For experimental lab scale model, the value of nominal phase to phase voltage is 300V, nominal frequency is 50Hz, active power is 3000W, inductive reactive power is 500 Var, in the circuit 24 IGBTs were used. Both IGBTs connected in series in half H-bridge cannot be turned on at the same time to avoid the shoot through fault.

III. SWITCHING TABLE

The Switching table of 5-level cascaded multilevel inverter is shown bellow

vdc	S1 S2 S6 S8	S9 S10 S14 S16	S17 S18 S22 S24
2vdc	S1 S2 S5 S6	S9 S10 S13 S14	S17 S18 S21 S22
0	S2 S4 S6 S8	S10 S12 S14 S16	S18 S20 S22 S24
- Vdc	S3 S4 S6 S8	S11 S12 S14 S16	S19 S20 S22 S24
-2vdc	S3 S4 S7 S8	S11 S12 S15 S16	S19 S20 S23 S24

Fig 2 switching table

IV. CONTROL TECHNIQUES

A number of PWM modulation strategies are used multilevel power conversion applications. This Multicarrier PWM modulation strategies can be categorized into the following groups like level shifted technique, phase shifted technique and variable frequency technique. This paper focuses on bipolar Trapezoidal Amalagated Rectangular modulation strategies which have been used in cascaded multilevel inverter. Level shifted technique is also categorized three types like a phase disposition technique (PD), phase opposition disposition technique (POD), Alternate phase opposition disposition technique (APOD).

A. PHASE DISPOSITION TECHNIQUE

In phase disposition modulation strategy 4 carrier waveforms are used. Where all carrier waveforms are in phase. Figure.3 shows the multicarrier arrangement for phase disposition technique.

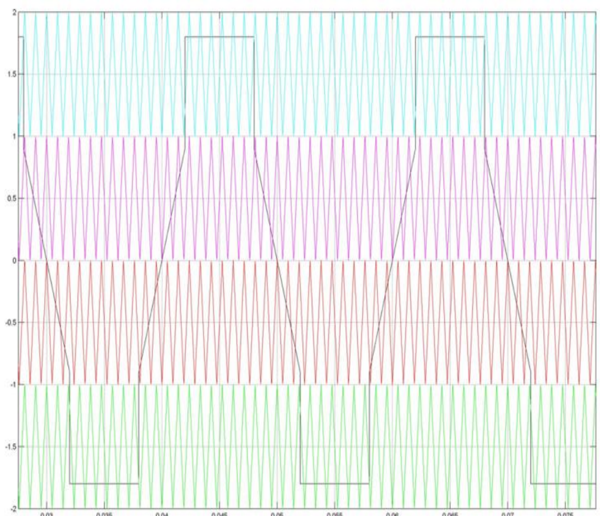

Fig.3 Multicarrier arrangement for PD technique

B. PHASE OPPOSITION DISPOSITION TECHNIQUE

For phase opposition disposition (POD) modulation all carrier waveforms above zero reference are in phase and are 180^0 out of phase with below zero. Figure.4 shows the multicarrier arrangement for phase opposition disposition technique.

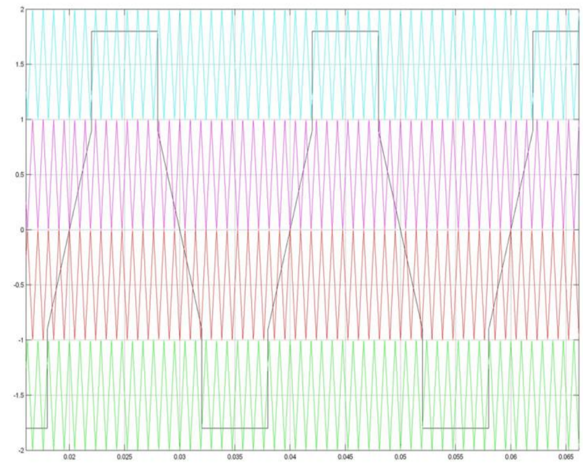

Fig.4 Multicarrier arrangement for POD Technique

C. ALTERNATE PHASE OPPOSITION DISPOSITION TECHNIQUE

Alternate phase disposition (APOD) modulation, every carrier waveform is out of phase with its neighbor carrier by 180^0. Figure.5 shows the multi carrier arrangement for APOD technique.

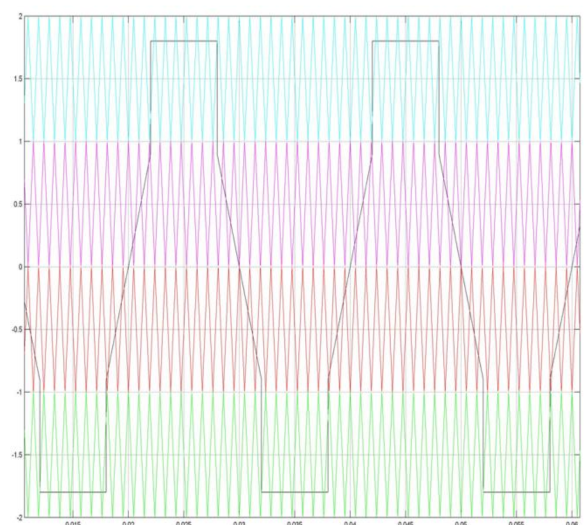

Fig.5 Multicarrier arrangement forAPODPWM Technique

D. PHASE SHIFT TECHNIQUE

In this phase shifted modulation technique carrier signals placement is usually all kinds of multilevel inverters. This phase shifted modulation requires n-1 carrier waveforms are shifted by 360^0/n-1, where n is number of levels. Figure 6 shows the multicarrier arrangement for PS technique.

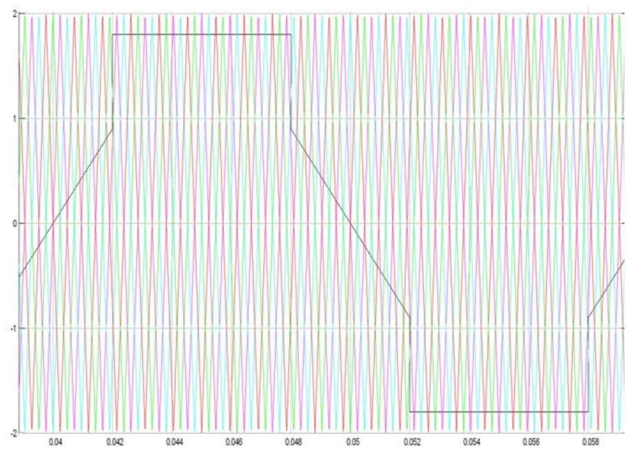

Fig.6 Multicarrier arrangement for PSPWM Technique

E. VARIABLE FREQUENCY (VF) PWM TECHNIQUE

In this variable frequency technique the frequencies of the 4 carrier waveforms are not the same. This variable frequency strategy is used as illustrated in figure 7 in which the carrier frequency of the intermediate switching is properly increased to balance the numbers of switching for all the switches.

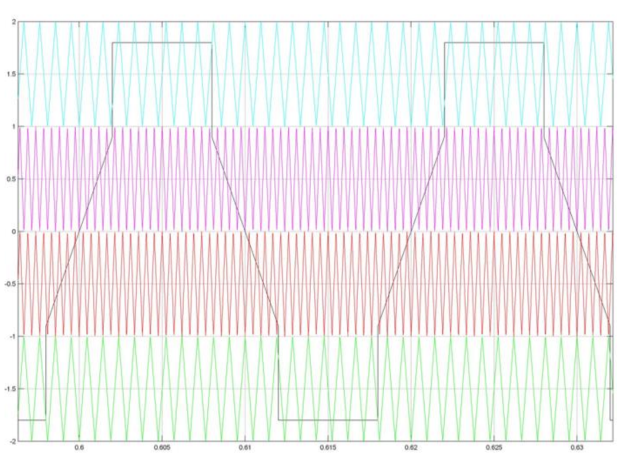

Fig.7 Multicarrier arrangement for VFPWM

V. SIMULATION RESULTS

The Three phase cascaded 5-level inverter is modeled by MATLAB-SIMULIN. Switching signals for the three phase 5-level CMI are developed using bipolar modulation technique discussed previously. Simulation is preformed for different values of m_a ranging from 0.8-1. The corresponding %THD AND Vrms values are measured using the FFT block and they are compared previous model of sine reference function. The Table 1 is shown for the Vrms value is more then the sine reference function and table 2 is shown for the %THD value is lesser then the sine reference function at modulation index m_a=1 for all technique like that of PD, POD, APOD, PS and VF control techniques.

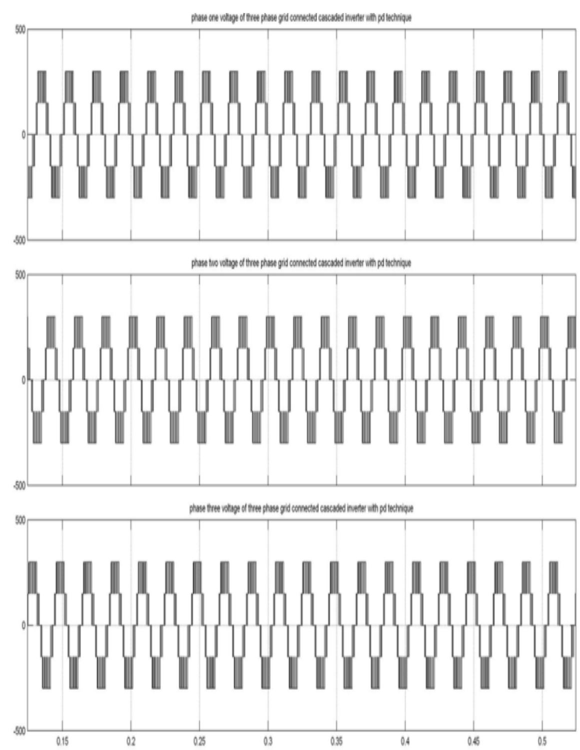

Fig .8 Output wave form of three phase cascaded inverter with PD technique

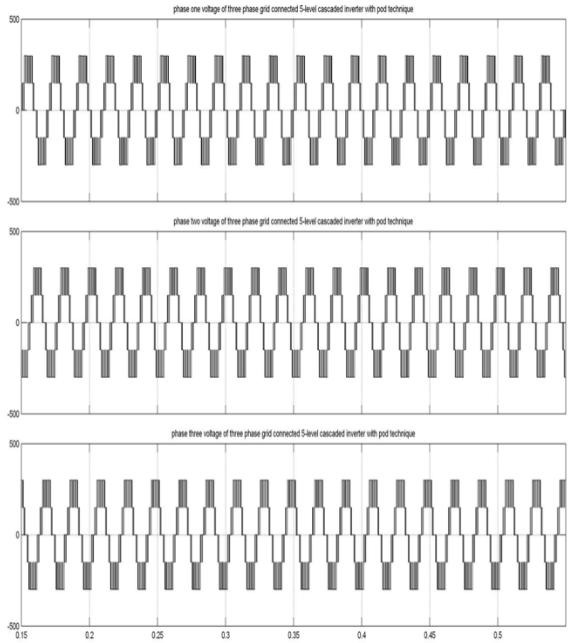

Fig.9 Output wave form of three phase cascaded inverter with POD technique

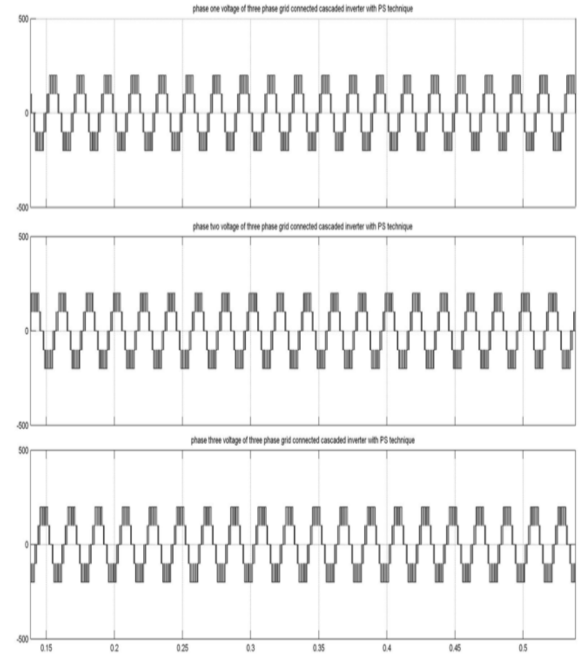

Fig .11 Output wave form of three phase cascaded inverter with PS technique

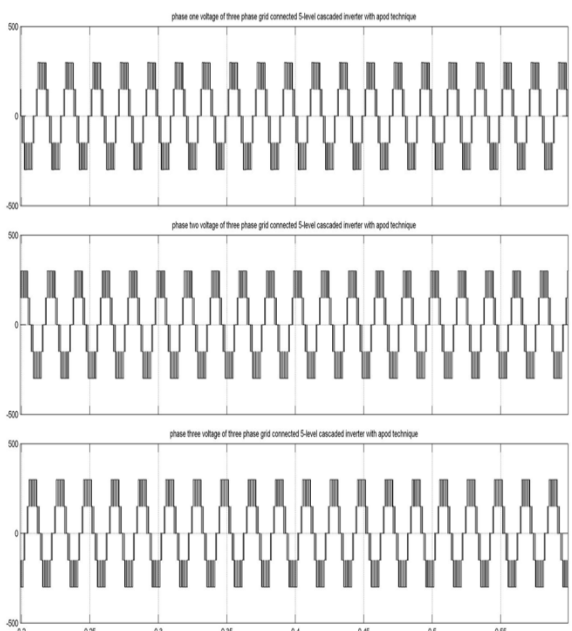

Fig.10 Output wave form of three phase cascaded inverter with APOD technique

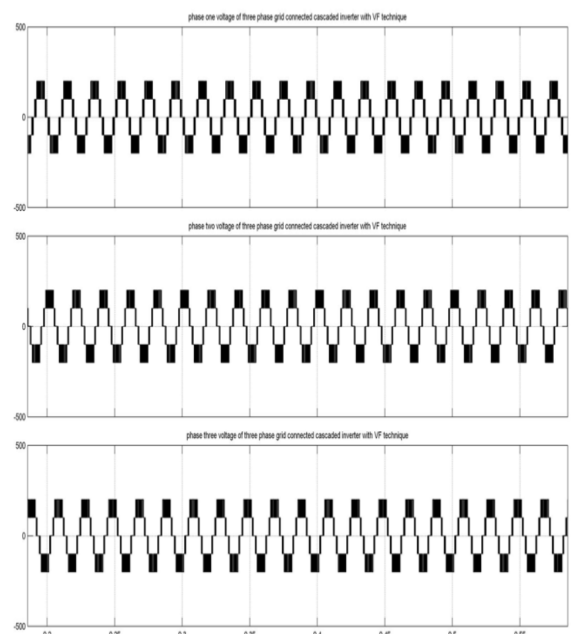

Fig.12 Output wave form of three phase cascaded inverter with VF technique

TABLE1 VRMS FOR DIFFERENT MODULATION INDICES

Bipolar Trapezoidal Amalagated Rectangular Reference						Sin wave reference function					
Modulation indices	PS	PD	POD	APOD	VF	Modulation indices	PS	PD	POD	APOD	VF
M_a=1	157	156.9	156.28	156.2	157.1	M_a=1	141.8	141.1	140.4	140.4	142.3
M_a=0.9	141.5	141	140.2	140.2	141.7	M_a=0.9	128.8	127.3	126.6	126.7	128.1
M_a=0.8	125.3	124.8	124.4	124.4	126.4	M_a=0.8	113.4	113.1	112.4	112.4	114.9

TABLE2 %THD FOR DIFFERENT MODULATION INDICES

Bipolar Trapezoidal Amalagated Rectangular Reference						Sin wave reference function					
Modulation indices	PS	PD	POD	APOD	VF	Modulation indices	PS	PD	POD	APOD	VF
M_a=1	157	156.9	156.28	156.2	157.1	M_a=1	141.8	141.1	140.4	140.4	142.3
M_a=0.9	141.5	141	140.2	140.2	141.7	M_a=0.9	128.8	127.3	126.6	126.7	128.1
M_a=0.8	125.3	124.8	124.4	124.4	126.4	M_a=0.8	113.4	113.1	112.4	112.4	114.9

VI. CONCLUSION

It is observed from Table 1 the bipolar trapezoidal rectangular reference function RMS output voltage is more than the sin reference function. It is observed from Table 2 the %THD value is less in the moderate index one for bipolar trapezoidal rectangular reference function compares to sin reference function. So level shifting technique provides higher DC bus utilization and phase shifting provides lowest distortion for moderate index $m_{a.}$

REFERENCES

[1] J. S. Lai and F. Z. Peng, “Multilevel converters–A new breed of power converters,” *IEEE Trans. Ind. Applicat.*, vol. 32, pp. 509–517, May/June 1996.

[2] L. Tolbert, F.-Z. Peng, and T. Habetler, “Multilevel converters for large electric drives,” *IEEE Trans. Ind. Applicat.*, vol. 35, pp. 36–44, Jan./Feb.1999
.

[3] R. Teodorescu, F. Beaabjerg, J. K. Pedersen, E. Cengelci, S. Sulistijo, B. Woo, and P. Enjeti, “Multilevel converters — A survey,” in *Proc. European Power Electronics Conf. (EPE’99)*, Lausanne, Switzerland,1999, CD-ROM.

4] B.Shanthi and S.P.Natarajan, 'Carrier overlapping PWM techniques for single phase cascaded five level inverter', International Journal of Science andTechniques of Automatic control & computer engineering (IJ-STA, Tunisia), Special issue on Control of Electrical Machines, pp. 590-601, December 2008.

[5] Ayob, S.M. and Salam, Z, 'A new PWM scheme for cascaded multilevel inverter using multiple trapezoidal modulation signals', Research report of University Teknology, Malaysia, pp.242-246, 2004.

[6] Carrara,G, Gardella, S., Marchesoni, M., Salutari, R. and Sciutto,G, 'A new multilevel PWM technique: a theoretical analysis', IEEE Trans.Power Electron .vo!.7, pp. 497-505, 1992.

[7] K. Surin and M. T. Leon, “Multilevel Power Converters”, Journal published in the Universityof Tennessee, 2000, Vol.31, pp 150.

[8] Sood V.K., (2004), HVDC and FACTS Controllers Application of Static Converters in Power Systems, Kluwer Academic Publishers, pp. 139-150.

[9] W. Bin, “High Power Converter and AC Drive”, 1st Edition, Wiley Interscience, 2006.

[10] Zhong D., Leon M.T, and John N.C, Harmonic Elimination for Multilevel converter with Programmed PWM Method, IEEE Transactions on Industry Applications, 2004, pp 2210-2215.

[11] D.Zhong, M.T.Leon and N.C. John “Harmonic Elimination for Multilevel Converter with Programmed PWM Method”, IEEE, Transactions on Industry Applications, 2004.

[12] P. T. Krein, B. M. Nee, and J. R. Wells, 'Harmonic elimination switching through modulation', in Proc . IEEE Workshop Comput.Power Electron.2004, pp. 123-126.

[13] R. Wells, X. Geng, P. L. Chapman, P. T. Krein, and B. M. Nee, 'Modulation-based harmonic elimination', IEEE Trans. Power Electron.,vol. 22, no. 1, pp. 336- 340, Jan. 2007.

[14] V. G Agelidis, A. Balouktsis, I. Balouktsis, and C. Cossar, 'Five-level selective harmonic elimination PWM strategies and multicarrier phaseshifted sinusoidal PW M: A comparison', in Proc. IEEE Power Electron.Specialists Conf, Recife, Brazil, Jun. 2005, pp. 1685-1691.

[15] M. S. A. Dahidah and V. G Agelidis, 'Selective harmonic elimination PWM control for cascaded multilevel voltage source converters: A generalized formula', IEEE Trans. Power Electron., vol. 23, no. 4, pp. 1620- 1630, Jul. 2008.

[16] J. Rodriguez, J. Lai, and F. Peng, 'Multilevel inverters:Asurvey of topologies, controls and applications', IEEE Trans. Ind. Electron., vol. 49, no. 4,pp. 724-738, Aug. 2002

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