# Simulation of Series, Parallel Configured 7 level Switched Capacitor Inverter with Inductive Load

Dosapati.Firoj Kumar<sup>#1</sup>, S.Chandra Sekhar<sup>#2</sup>

*#EEE Department, Anurag Engineering College Kodad, Nalgonda District, Telangana, India* <sup>1</sup>charan.dosapati@gmail.com  $^{2}$ hod.eee@anurag.ac.in

*Abstract—* **Switched capacitor converters have become more common in recent years. A multilevel inverter with a limited number of switching devices is proposed. That inverter consists of an H-bridge and an inverter which outputs of multilevel voltage by switching the DC voltage sources in series and in parallel. Then the researched inverter can huge numbers of voltage levels in the equal number of switching devices by using the conversion system. When we reduce the number of gate driving circuits, which leads to reduce the size and power consumption in the driving circuits. And also reduce the THD (Total Harmonic Distortion) of the output waveforms. Unlike traditional multilevel inverters, this topology does not require an external voltage balancing circuit, a complicated control scheme, or isolated dc sources to maintain its voltage levels while delivering sustained real power. The simulation results are carried by MATLAB/SIMULINK SOFTWARE.**

*Keywords***— Charge pump, multicarrier PWM, multilevel inverter, switched capacitor (SC).Introduction**

#### I. INTRODUCTION

In the last few year's electric vehicles (EVs), hybrid Electric vehicles (HEVs) are studied all over the world due to several advantages like increased fuel efficiency, lower emissions and better vehicle performance. These vehicles that have large electric drives[5]-[7] require advanced power electronic inverters to meet the high-power demands One of the limitation in these studies when the switching devices are operated at high voltage, switching frequency is restricted. The multilevel inverter has gained much attention in recent years due to its advantages in high power with low harmonics applications.

Multilevel inverters overcome this problem because their individual devices have a much lower voltage per switching and they operate [11]-[15] at high efficiencies because they can switch at a much lower frequency than PWM-controlled inverters. A multilevel inverter can reduce the device voltage and the output harmonics by increasing the number of output voltage levels. For this reason, multilevel inverters can easily provide the high power required of a large electric drives. The inverter can be used in hybrid electric vehicles (HEV)[9],[15] and electric vehicles (EV). Several multilevel inverter topologies have been developed like flying capacitor, neutral point clamped, Cascaded H-bridge (CHB)[7]. Among these topologies, the cascaded H bridge inverter has received much attention. To increase the output voltage levels, the number of H bridges must be connected in cascade, hence greater numbers of power semi conductor switches are required. Each switch requires a related gate drive and protection circuits. This may cause the overall system to be more expensive and complex. A charge pump outputs a larger voltage than the input voltage with switched capacitors [7], [8].

The proposed inverter does not have any inductors can be smaller than a conventional two-stage unit which consists of a boost converter and an inverter bridge, which make the system large. The structure of the inverter is simpler than [13] the conventional switched-capacitor inverters. THD of the output waveform of the inverter is reduced compared to the conventional single phase full bridge inverter as the conventional multilevel inverter. In this paper, an SC inverter whose structure is simpler than the conventional SC inverter is proposed. It consists of a Marx inverter structure and an Hbridge. The proposed inverter can output larger voltage than the input [3] voltage by switching the capacitors in series and in parallel. The proposed inverter does not have any inductors which make the system large[14]. The output harmonics of the proposed inverter are reduced by the multilevel output.

#### II. CIRCUIT DESCRIPTION

A voltage source Vin is the input voltage source. A low pass filter is composed of an inductor L and a capacitor C. There are many modulation methods to drive a multilevel inverter:



Fig. 1. Circuit topology of the switched-capacitor inverter using series/ parallel conversion

The space vector modulation the multicarrier pulse width modulation (PWM) the hybrid modulation the selective harmonic elimination and the nearest level control. In this paper, the multicarrier PWM method is applied to the proposed inverter.

LIST OF THE ON –STATE SWITCHES ON EACH STATE

<b>Relation between es</b> and $e_k$	On – state Switches	<b>Ideal Bus</b> Voltage $V_{bus}$
$e_{s} > e_{1}$	$S_1, S_4, S_{31}, S_{32}$	$3V_{in}$
$e_1 \ge e_s > e_2$	$S_1, S_4, S_{a1}, S_{b2}, S_{c2}$	$2V_{in}$
$e_2 \ge e_s > e_3$	$S_1, S_4, S_{b1}, S_{c1}, S_{b2}, S_{c2}$	$V_{in}$
$e_3 \ge e_s > e_4$	$S_2, S_4, S_{b1}, S_{c1}, S_{b2}, S_{c2}$	$\theta$
$e_4 \ge e_5 > e_5$	$S_2, S_3, S_{b1}, S_{c1}, S_{b2}, S_{c2}$	$-V_{in}$
$e_5 \ge e_s > e_6$	$S_2, S_3, S_{b1}, S_{c1}, S_{a2}$	$-2V_{in}$
$e_6 > e_s$	$S_2, S_3, S_{a1}, S_{a2}$	$-3V_{in}$

A voltage source  $V_{in}$  is the input voltage source. A low pass filter is composed of an inductor *L* and a capacitor *C*. There are many modulation methods to drive a multilevel inverter: the space vector modulation the multicarrier pulse width modulation (PWM) the hybrid modulation the selective harmonic elimination and the nearest level control. In this paper, the multicarrier PWM method is applied to the proposed inverter.



(a) The current ibus does not flow in the capacitors Ck,



(b) All capacitors are connected in Parallel



(c) The capacitor C1 is connected in series and the capacitor C3 is

Connected in parallel



(d) All capacitors are connected in series.

Fig. 2. Current flow of the proposed inverter  $(n = 2)$  on each state of  $(a)$ ,  $(b)$ ,  $(c)$  and  $(d)$ 

There are many modulation methods to drive a multilevel Inverter: the space vector modulation the multicarrier pulse width modulation (PWM) the hybrid modulation the selective harmonic elimination and the nearest level control. In this paper, the multicarrier PWM method is applied to the proposed inverter. Fig. 2 shows the current flow in the proposed inverter  $(n = 2)$  and Fig. 3 shows the modulation method of the proposed inverter  $(n = 2)$ . When the time t satisfies  $0 \le t < t_1$  in Fig. 3, the switches  $S_1$  and  $S_2$  are driven by the gate-source voltage  $V_{GS1}$  and  $V_{GS2}$ , respectively. While the switches  $S_I$  and  $S_2$  are switched alternately, the other switches are maintained ON or OFF state as shown in Fig. 3. Therefore, the states shown in Fig. 2(a) and (b) are switched alternately and the bus voltage *Vbus* takes 0 or *Vin*. When the time t satisfies  $t_1 \le t < t_2$  in Fig. 3, the switches Sa1, Sb1, and Sc1 are driven by the gate-source voltage  $V_{GSal}$ ,  $V_{GSbl}$ , and *VGSc1*, respectively. While the switches *Sa1, Sb1, and* Sc1are switched alternately, the other switches are maintained ON or OFF state as shown in Fig. 3.Therefore; the states shown in Fig. 2(b) and (c) are switched alternately. The capacitor C1 is charged by the current *−iC1* as shown in Fig. 2(b) during the state shown in Fig. 2(b). Therefore, the proposed inverter can output the bus voltage  $v_{bus}$  while the capacitor  $C_I$  is charged. The bus voltage  $v_{bus}$  in the state of Fig. 2(c) is

$$
vbus = V\dot{x} + V_{C1} \tag{1}
$$



### III. MODULATION METHOD OF THE PROPOSED INVERTER

switches are maintained ON or OFF state as shown in Fig. 3. Therefore, the states shown in Fig. 2(c) and (d) are switched alternately. The capacitor  $C_3$  is charged by the current  $-i_{C3}$  as shown in

switches  $S_{a2}$ ,  $S_{b2}$ , and  $S_{c2}$  are switched alternately, the other

Fig. 2(c) during the state shown in Fig. 2(c). The bus voltage  $v_{bus}$  in the state of Fig. 2(d) is

$$
vbus = Vin + VC1 + VC3 \tag{2}
$$

Where  $V_{C3}$  is the voltage of the capacitor C3. Therefore, the proposed inverter outputs  $V_{in}$  +  $V_{C1}$  or  $V_{in}$  +  $V_{C1}$  +  $V_{C3}$ alternately in this term. After  $t = t_3$ , the four states show in Fig. 2 are repeated by turns. Table I shows the list of the on-state switches when the proposed inverter  $(n= 2)$  is driven by the modulation method shown in Fig. 3. The ideal bus voltage  $V_{bus}$  in Table I means the bus voltage on each state when  $V_{C1}$  $= V_{C3} = V_{in}$  is assumed.

As the conventional SC inverter, the proposed inverter has a full bridge which is connected to the high voltage. Therefore, the device stress of the switches  $S_1 - S_4$  in the full bridge is higher than the other switches as the conventional SC inverter. The proposed inverter  $(n = 2)$  outputs a 7-levelvoltage by repeating the four states as shown in Fig. 2. Because the driving waveform *VGSa1* and *VGSa2* change alternately as shown in Fig. 3, the capacitors  $C_I$  and  $C_3$  are equally discharged .Assuming that the number of the capacitors is 2n − 1, the proposed inverter can outputs 4n − 1levels voltage waveform. The modulation index M is defined as the following equation because the amplitude of the output voltage waveform is

inversely proportional to the double amplitude of the carrier waveform.

$$
M = Aref 2AC \tag{3}
$$

In (3),  $A_{ref}$  is the amplitude of the reference waveform and Ac is the amplitude of the carrier waveform. The proposed inverter requires 10switching devices for the 7-level, and 16switching devices for the 11-level. On the other hand, the conventional SC inverter requires 20switching devices for the 7-level, and 28switching devices for the 11-level [9]. The conventional cascaded H-bridge (CHB) inverter requires 12 switching devices for the 7-level, and20 switching devices for the 11-level, when all the dc voltage sources take the same voltage [17]. Therefore, the proposed inverter has less number of switching devices than the conventional multilevel inverters.

#### IV. SIMULATION RESULTS

Here simulation is carried out in different cases, in that

- 1)Proposed Series/Parallel Multilevel Inverter Topology without Filter Proposed
- 2)Series/Parallel Multilevel Inverter Topology with Filter

## CASE 1: *Proposed Series/Parallel Multilevel Inverter Topology without Filter*

Where  $V_{CI}$  is the voltage of the capacitor  $C_I$ . Therefore, the proposed inverter outputs  $V_{in}$  or  $V_{in} + V_{CI}$ 

alternately in this term. When the time t satisfies  $t_2 \le t < t_3$  in Fig. 3, the switch  $S_{a2}$ ,  $S_{b2}$  and  $S_{c2}$  are driven by the gate-source voltage *VGSa2*, *VGSb2* and *VGSc2*, respectively. While the



Fig.4 Matlab/Simulink Model of Proposed Series/Parallel Multilevel Inverter Topology

Fig.4 shows the Model of Proposed Series/Parallel Multilevel Inverter Topology without Filter using Matlab/Simulink Platform.



Fig.5 shows the Output Voltage of Proposed Series/ Parallel Multilevel Inverter Topology without filter



Fig.6 shows the FFT Analysis of Output Voltage of Proposed Series/ Parallel Multilevel Inverter Topology, here we get 21.38%.



Fig.7 Matlab/Simulink Model of Proposed Series/Parallel Multilevel Inverter Topology with Filter

Fig.7 shows the Model of Proposed Series/Parallel Multilevel Inverter Topology with Filter using Matlab/Simulink Platform. With Filter







Fig.9 Matlab/Simulink Model of Proposed Series/Parallel MultilevelInverter Topology with Filter

### V. CONCLUSION

In this paper, a novel boost switched-capacitor inverter was proposed. The circuit topology was introduced. Multilevel inverters play a key role in many industries and used in high power applications. Such as drive control, grid connected systems and standalone systems. In comparison of various multilevel inverters to proposed inverter need low switch count, low gate drive circuit, low Switching loss and good voltage profile. The proposed method is enormously evaluated using Matlab/Simulink software with proposed converter and closed loop operation of inverter topology and get better. Steady state response, by using second higher order filter the THD is very low with high grid stability.

#### **REFERENCES**

- [1] [1] H. Liu, L. M. Tolbert, S. Khomfoi, B. Ozpineci, and Z. Du, "Hybrid cascaded multilevel inverter with PWM control method," in Proc. IEEE Power Electron. Spec. Conf., Jun. 2008, pp. 162– 166.
- [2] A. Emadi, S. S. Williamson, and A. Khaligh, "Power electronics intensive solutions for advanced electric, hybrid electric, and fuel cell vehicular power systems," IEEE Trans. Power Electron., vol. 21, no. 3, pp. 567–577, May 2006.
- [3] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," IEEE Ind. Electron. Mag., vol. 2, no. 2, pp. 28–39, Jun. 2008.
- [4] Y. Hinago and H. Koizumi, "A single phase multilevel inverter using switched series/parallel DC voltage sources," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2643–2650, Aug. 2010.
- [5] S. Chandrasekaran and L. U. Gokdere, "Integrated magnetics for interleaved DC–DC boost converter for fuel cell powered vehicles," in Proc. IEEE Power Electron. Spec. Conf., Jun. 2004, pp. 356–361.
- [6] Y. Hinago and H. Koizumi, "A switched-capacitor inverter using series/ parallel conversion," in Proc. IEEE Int. Symp. Circuits Syst., May/Jun. 2010, pp. 3188–3191.
- [7] J. A. Starzyk, Y. Jan, and F. Qiu, "A dc–dc charge pump design based on voltage doublers," IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., vol. 48, no. 3, pp. 350–359, Mar. 2001.
- [8] M. R. Hoque, T. Ahmad, T. R. McNutt, H. A. Mantooth, and M. M. Mojarradi, "A technique to increase the efficiency of highvoltage charge pumps," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53, no. 5, pp. 364–368, May 2006.
- [9] O. C.Mak and A. Ioinovici, "Switched-capacitor inverter with high power density and enhanced regulation capability," IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., vol. 45, no. 4, pp. 336– 347, Apr. 1998.
- [10] B. Axelrod, Y. Berkovich, and A. Ioinovici, "A cascade boostswitched capacitor- converter-two level inverter with an optimized multilevel output waveform," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 52, no. 12, pp. 2763–2770, Dec. 2005.
- [11] J. I. Rodriguez and S. B. Leeb, "A multilevel inverter topology for inductively coupled power transfer," IEEE Trans. Power Electron., vol. 21, no. 6, pp. 1607–1617, Nov. 2006.
- [12] X. Kou, K. A. Corzine, and Y. L. Familiant, "A unique faulttolerant design for flying capacitor multilevel inverter," IEEE Trans. Power Electron., vol. 19, no. 4, pp. 979–987, Jul. 2004.
- [13] S. Lu, K. A. Corzine, andM. Ferdowsi, "A unique ultracapacitor direct integration scheme in multilevel motor drives for large vehicle propulsion," IEEE Trans. Veh. Technol., vol. 56, no. 4, pp. 1506–1515, Jul. 2007.
- [14] J. I. Leon, S. Vazquez, A. J. Watson, L. G. Franquelo, P. W. Wheeler, and J. M. Carrasco, "Feed-forward space vector modulation for single-phase multilevel cascaded converters with any dc voltage ratio," IEEE Trans. Ind. Electron., vol. 56, no. 2, pp. 315–325, Feb. 2009.
- [15] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 858–867, Aug. 2002.
- [16] R. Gupta, A. Ghosh, and A. Joshi, "Switching characterization of cascaded multilevel-inverter-controlled systems," IEEE Trans. Ind. Electron., vol. 55, no. 3, pp. 1047–1058, Mar. 2008.
- [17] J. Zhang, Y. Zou, X. Zhang, and K. Ding, "Study on a modified multilevel cascade inverter with hybrid modulation," in Proc. IEEE Power Electron Drive Syst., Oct. 2001, pp. 379–383.
- [18] V. G. Agelidis, A. I. Balouktsis, and C. Cossar, "On attaining the multiple solutions of selective harmonic elimination PWM threelevel waveforms through function minimization," IEEE Trans. Ind. Electron., vol. 55, no. 3, pp. 996–1004, Mar. 2008.
- [19] J. A. Pontt, J. R. Rodriguez, A. Liendo, P. Newman, J. Holtz, and J. M. San Martin, "Network-friendly low-switching-frequency multipulse high-power three-level PWM rectifier," IEEE Trans. Ind. Electron., vol. 56, no. 4, pp. 1254–1262, Apr. 2009.
- [20] M. K. Kazimierczuk, "Switching losses with linear MOSFET output capacitance," in Pulse-Width Modulated DC–DC Power Converters, 1st ed. West Sussex, U.K.: Wiley, 2008, ch. 2, pp. 37– 38, sec. 2.9.